A family of universal modules of the ADC/DAC

Measuring voltage converters

L-502-P-G-D-I
L-502-P-G
L-502-P-G-D
L-502-X-G
L-502-X-G-D
L-502-X-X
L-502-X-X-D

User manual

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L-CARD

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DAQ SYSTEMS DESIGN, MANUFACTURING & DISTRIBUTION

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Revision history of this document

Date	Document revision	Contents of the change
06.2012	1.0.1	Preliminary data
07.2012	1.0.2	Preliminary data
11.2012	1.0.3	The information on connection L-502 is added, as well as Chapter 6 an item 4.2.3.1, item 4.2.4.1, item 4.2.5, item 4.3, item ... is added by 4.4.
01.2014	1.0.4	Edited table 4-1, supplemented paragraphs. 1.3, 2.4, 2.5. 4.2.4
05.2014	1.0.5	A comment is added to the item 5.1.2, page 51
06.2014	1.0.6	Different names of signals are fixed: SYNC_IN, SYNC_OUT is changed to START_IN, START_OUT, accordingly.
05.2015	1.0.7	Added item 3.3.5, item . 5.5.1
03.2016	1.0.8	Added Chapter 7
02.2017	1.0.9	Paragraph added 3.3.4.1
07.2017	1.0.10	A warning is added to item. 3.3.5.2
10.2017	1.1.0	Added industrial design versions. The characteristics according to the results of preparation of the family of *L-CARD voltage measuring converters* for certification as Means of Measurement are brought into correspondence. Added to item 3.3.8. Paragraph added 4.5

When reading this document electronically, to facilitate navigation, use the electronic tree of the table of contents (for example, Acrobat Reader), as well as hyperlinks within the document.

Contents

Chapter 1. General description.

L-Card data acquisition system **L-502** based on the **PCI Express** interface of modern computer motherboards. **L-502 –** this system of the proprietary development of the "L-Card" LLC, it is made on the basis of high-tech production of the company, it provides its own technical support and maintenance.

The most important characteristics of L-502:

- ADC: 16 bits, conversion frequency up to 2 MHz, with switching to 16 differential channels or 32 channels with common ground. Subranges: ±10 V", "±5 V", "±2 V", "±1 V", ±0.5 V, ±0.2 V.
- DAC (optional): 16 bits, 2 channels, output ± 5 V, asynchronous or synchronous mode with a conversion frequency of up to 1 MHz for each channel.
- Digital input: up to 18 digital inputs of general purpose, asynchronous or synchronous data collection mode with a frequency of up to 2 million words per second.
- Digital output: up to 16 digital outputs of general purpose, with separate control of the output resolution of the high and low byte, asynchronous or synchronous data output mode with a frequency of up to 1 million words per second.
- Processor Blackfin 530 MHz, 32 MB RAM, JTAG input (optional) allows you to use the ready "advanced" signal processing and control functions inside the **L-502** or independently engage in low-level programming of these functions.
- Galvanic isolation (optional) provides isolation of digital and analog signal inputs/ outputs to all circuits of the computer.

The above "optional" is reflected in the **L-502** module designation system on fig. 1-1.

The system can consist of one or more modules (boards) **L-502**, synchronized from each other, from an internal or external synchronization source.

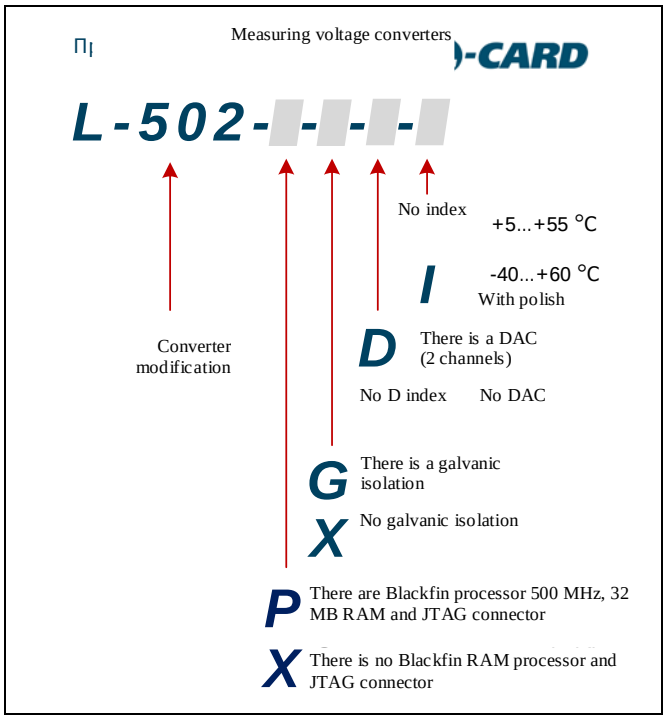


Fig. 1-1. Symbol system for L-502 module

1.1. Order information

Available modifications for L-502 for the order:

L-502-P-G-D-I

L-502-P-G, L-502-P-G-D

L-502-X-G, L-502-X-G-D

L-502-X-X. L-502-X-X-D

When choosing the modification of the L-502 module for the order, it should be noted that when you contact the L-Card sales department, the previously purchased version of the L-502 module can be modified only in the direction of installing the DAC. In other words, only the following modifications of the L-502 modules are technically recognized:

L-502-P-G → L-502-P-G-D

L-502-X-G → L-502-X-G-D

L-502-X-X → L-502-X-X-D

This work on the installation of a DAC can be carried out exclusively in the L-Card, while the original warranty period of 1.5 years for the product L-502 is retained.

1.1.1. Order kit

1. Module L-502 (in accordance with the ordered modification)
2. Cable part of DB-37F connector;
3. Cover for DP-37 connector
4. Jumper for configuration of outputs (3 pieces are pre-installed on the board + 2 pieces in the kit).
5. The synchronization cable *is supplied separately*. The cable is used to connect two L-502 modules. In the general case, for the connection of N pcs. of L-502 modules on one motherboard, you will need (N-1) pcs. of synchronization cables.

1.2. Consumer properties of L-502 in comparison with L-780(M), L-783(M), L-791

The new family of **L-502** in its overall technical characteristics is the development of the line **L-780 (M)**, **L-783 (M)**, **L-791** at a higher technological level**.** There is considerable compatibility of **L-502** in the type and purpose of the contacts of signal connectors, but, unfortunately, there is no software compatibility with them. The **L-502** module is more versatile in its capabilities as it practically covers the range of tasks that was solved earlier within the framework of the 700th family, in addition, it offers fundamentally new opportunities. A comparison of the technical characteristics of the **L-502** module with its predecessors of the 700th family is shown in table 1-1. The following conventions are adopted in the table, which are consistent with the versions of modifications L-502 in accordance with fig. 1-1:

- [P] – only for L-502-P-▒-▒ (with processor)
- [~~P~~] – only for L-502-X-▒-▒ (without processor)

- [G] – only for L-502-▒-G-▒ (with galvanic isolation)
- [D] – only for L-502-▒-▒-D (with DAC)

Table 1-1. Comparison with L-502 c L-780(M), L-783(M) and L-791

Characteristics	L-502	L-780(M)	L-783(M)	L-791
Bit depth:				
- ADC	16[1]	14	12	14
- DAC	16 [D]	12	12	12
- Dig. input	18	16	16	16
- Dig. output	16	16	16	16
Max. speed of o/i, in synchronous mode, n. count./s [2]				
- ADC	2000	400	3000	400
- DAC (for each channel)	1000 [D]	100	100	100
- Digital input	2000	No synchronous mode		400
- Digital output	1000	No synchronous mode		
ADC channels	16 differential/ 32 with common ground			
ADC subranges, V	±10, ±5, ±2, ±1, ±0,5, ±0,2	±5, ±1,25, ±0,3, ±0,08	±5, ±2,5, ±1,25, ±0,6	±10, ±5, ±2,5, ±1,25, ±0,6, ±0,3, ±0,15, ±0,07
ADC common-mode signal range, V	±1	±5	±5	±10
DAC range, V (output current, mA)	±5 (10) [D]	±5 (1)	±5 (1)	±5 (1)
The word width of the module data, bit	32	16	16	32
Multiple-frequency capability of data collection	Yes [P]	No	No	Yes
Index[3] data format	Yes	No	No	No
Internal data calibration	Yes [P]. Only for ADC [~~Р~~]	Only for ADC	Only for ADC	No
Ability to set ADC channel resolution/ timing	Yes	No	No	No
Processor (core clock)	ADSP-BF523 (530 MHz) [P]	ADSP-2185(M)		No
		29,5 MHz	40 MHz	
Processor's external RAM	32 MB [P]	No	No	No

[1] From the L-502, ADC data, expanded to 24 bits as a result of arithmetic processing, is transferred to the computer.
[2] A reference is the full word of the data of the ADC, DAC or input/ output with the bit width adopted in this product.
[3] When the data word format contains information about the channel number

Characteristics	L-502	L-780(M)	L-783(M)	L-791
The amount of user area of Flash-memory	1 MB	32 bytes	32 bytes	64 Kbyte
JTAG port to adjust the embedded software	Yes [P]	No	No	No
The possibility of custom low-level programming	Yes	Yes	Yes	No
Independent software access to the memory of the signal processor	Yes [P]	Yes	Yes	No
DMA in PCI BUS MASTER mode	Yes	No	No	Yes
Interface	PCIe x1	PCI 32 bit, slot 5V		
Synchronization: - External data collection start - External frequency of ADC conversion - From the next module - Analogous	 Yes Yes Yes Yes	 Yes No No Yes	 Yes No No Yes	 Yes No No No
The technology of the basic interface element	FPGA Altera Cyclone IV	PLX Tech. PLX9050/9030	PLX Tech. PLX9050/9030	FPGA Altera Acex1K
Indication on the panel	Yes	No	No	No
The possibility of remote firmware update FPGA	Yes	No	No	Yes
Program activation of pull-up resistors of digital inputs	Yes	No	No	No
Independent resolution of the active state of the digital output of the low and high byte	Yes	No	No	No

Full list of L-502 characteristics – Chapter 5 on page 49.

Already today, the architecture of the L-502 is not limited to just this one project by L-Card LLC. The new E-502 with USB and Internet interfaces has a continuity of architecture with L-502: Only the interface with the PC with the same functionality as the L-502 was subjected to processing, except for small functional differences. The E-502 and L-502 software also has continuity (common library functions of the upper software level of the PC, identical to the software at the Blackfin level).

1.3. Appearance and main structural elements

Depending on the version of the module (item 2.4, p.17), there are differences in the location of the inter-module sync connector and the output enable connector. Unlike the previous versions, in version 3, an angular synchronization connector is used, which allows connecting the synchronization cable when the L-502 module is already inserted and fixed in the system unit along with the installed adjacent PCI-Express modules.

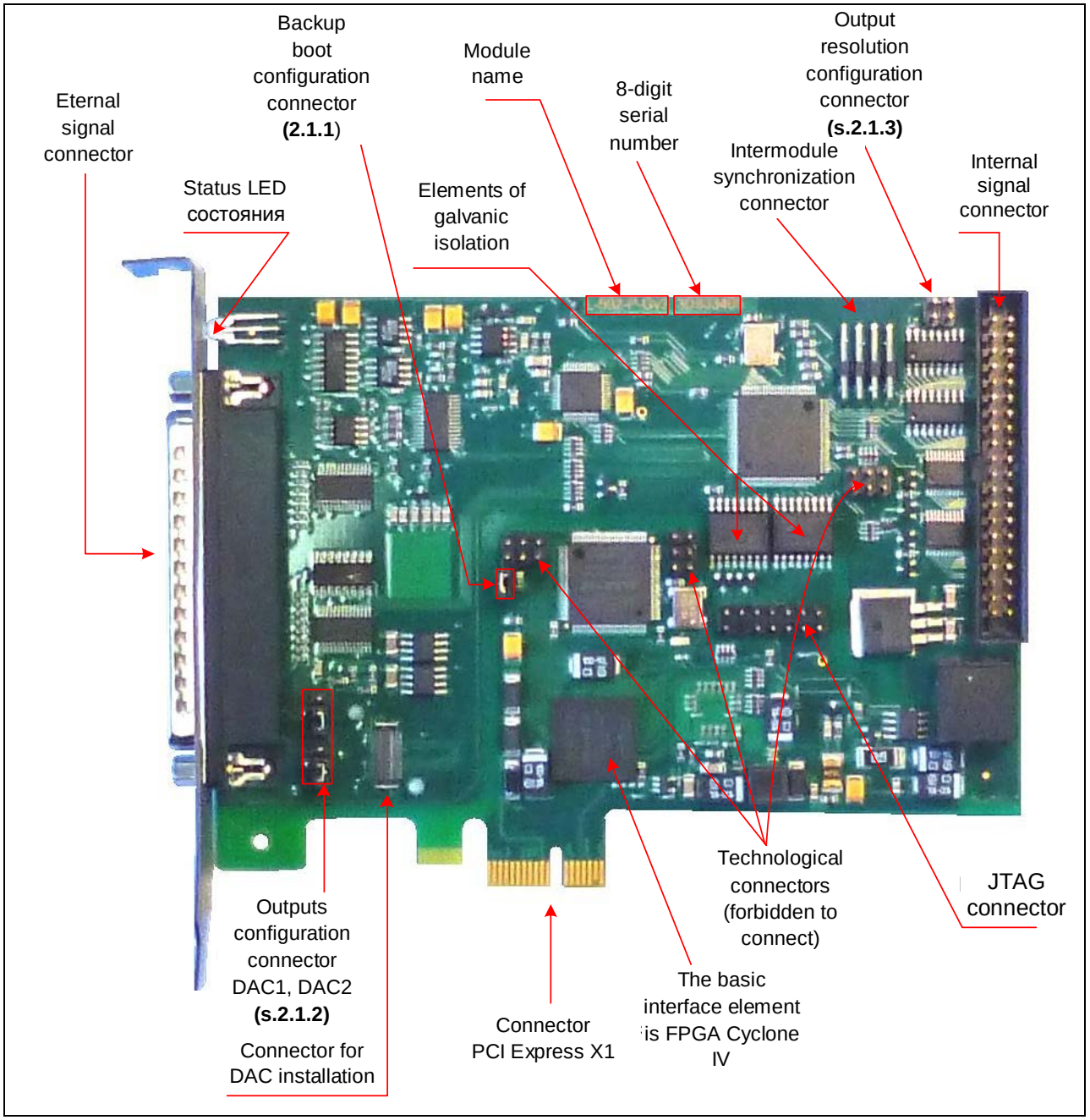


Fig.1-2. L-502 version 3 (face layout)

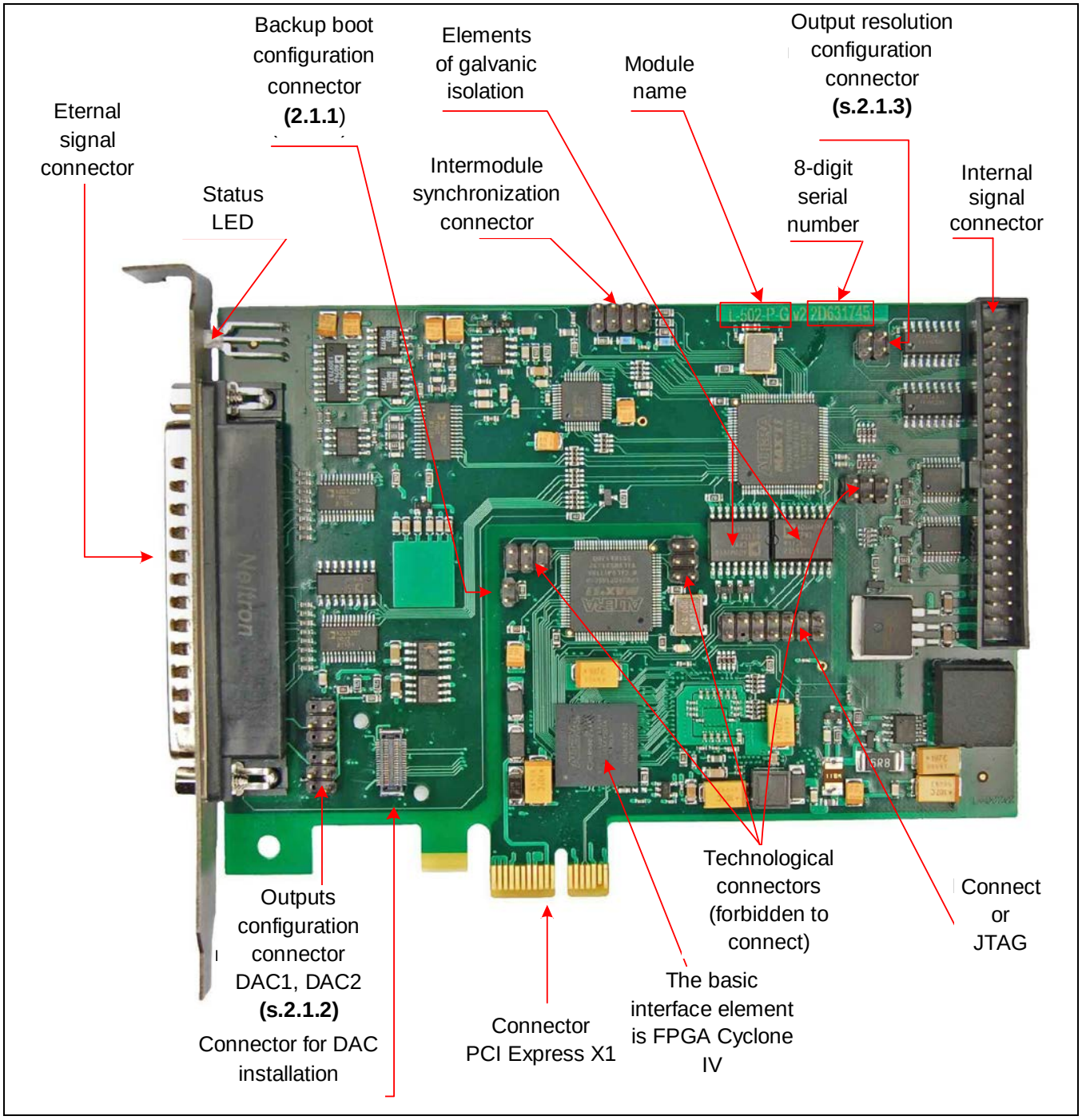


Fig. 1-3. L-502 version 1 or 2 (face layout)

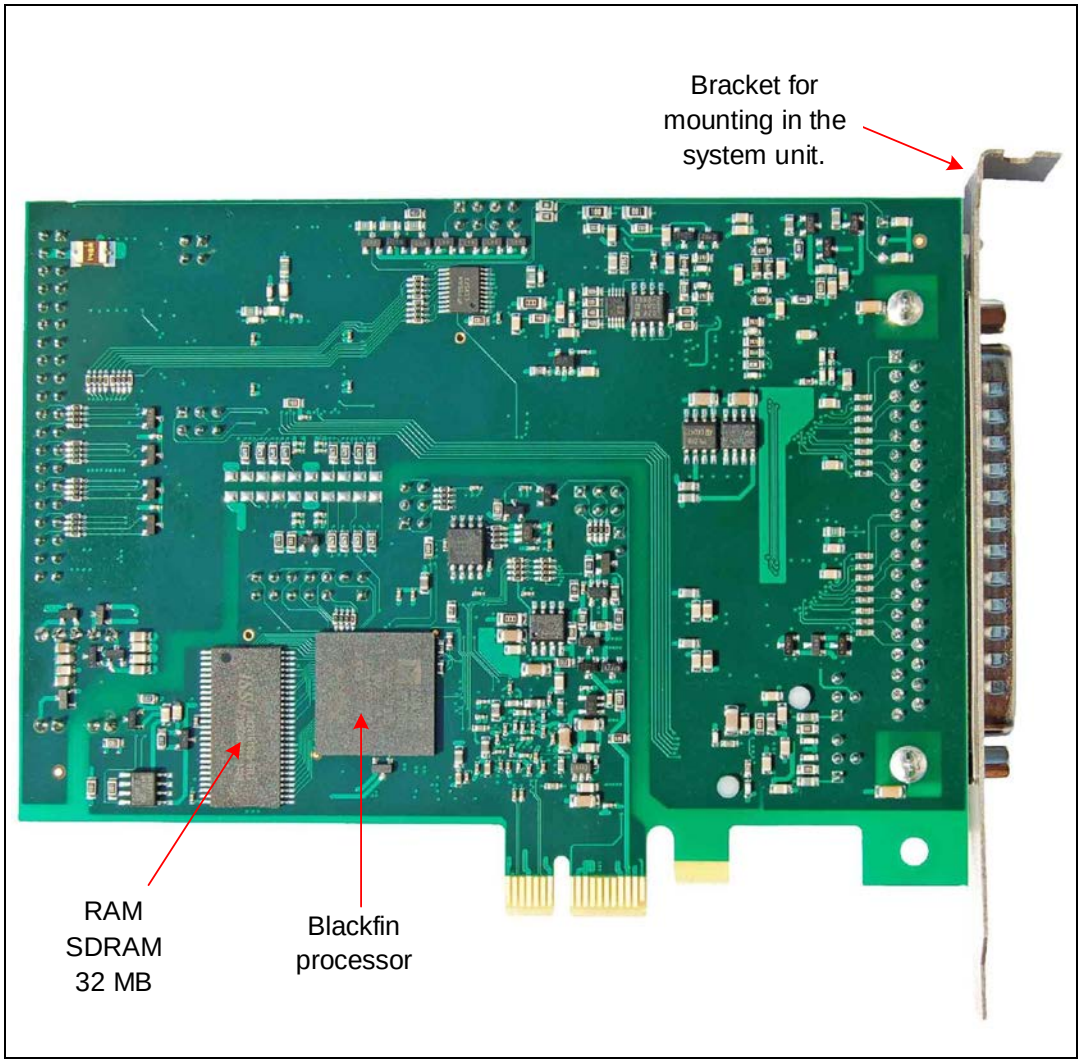


Fig.1-4. L-502 (back layout)

1.4. Documentation structure for L-502

A complete guide to the L-502 is divided into four separate books:

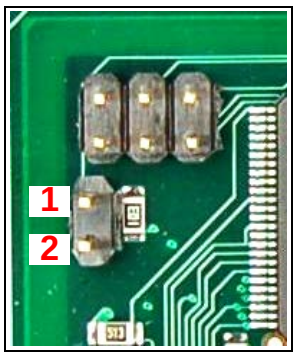
- *L-502. User Manual*
- *L-502. Programmer Manual*
- *L-502. Connexion samples*
- *L-502. Low-level description*

Chapter 2. Installation and configuration.

2.1. Configuration L-502.

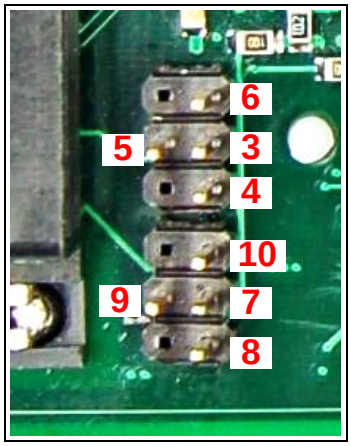
Here, the hardware settings of the L-502 are considered, which must be done before the L-502 module is installed in the computer. These settings are made by jumper, which you need to put (or not) on the corresponding pair of contacts, indicated below in the tables with conditional numbers.

2.1.1. Backup boot configuration

	Jumper for 1-2	FPGA is loaded with the main firmware from the Flash-memory. This loading mode is considered the main mode, and the L-502 always comes with a jumper set to contacts 1-2.
	No jumper	FPGA is loaded with a backup copy of the firmware from Flash-memory. This loading mode is considered auxiliary and the user can apply it if, for some reason, the main flash memory firmware has been corrupted and, as a result, the L-502 device has ceased to be detected by the operating system. See Note.

Note: Putting or removing the backup jumper should be done with the computer system's completely de-energized computer (the usual shutdown of the computer - the software or the button at the front of the system unit - is not enough, since the system unit has the "standby" power)

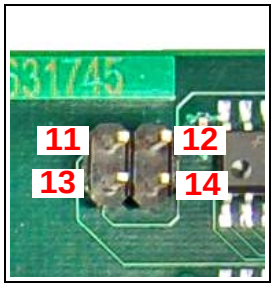
2.1.2. The configuration of the outputs DAC1 and DAC2



No jumper on 3,4,5,6	The contact "DAC1" is not connected to the external signal connector, see item 4.2.1, p. 33
Jumper on 3-4	The contact "DAC1" on the connector is connected to the DAC - channel 1
Jumper on 3-5	The contact "DAC1" on the connector is connected to +15V
Jumper on 3-6	The contact "DAC1" on the connector is connected to AGND
No jumper on 7,8,9,10	The contact "DAC2" is not connected on the connector
Jumper on 7-8	The contact "DAC2" on the connector is connected to the DAC - channel 2
Jumper on 7-9	The contact "DAC2" on the connector is connected to -15V.
Jumper on 7-10	The contact "DAC2" on the connector is connected to the DGND *digital ground* circuit.

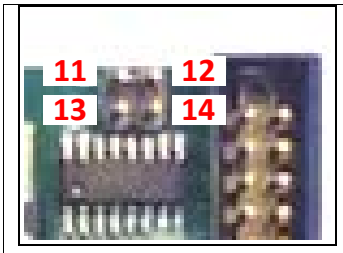
2.1.3. Configuring the resolution of the active state of the digital outputs

For version 1 or 2 :



For version 3:

Jumper on 11-12	Forced output enable of the low-order byte, see 4.2.3, p.36.
No jumper on 11-12	The resolution of the low byte output depends on the program setting.
Jumper on 13-14	Forced output enable of high byte.
No jumper on 13-14	The output enable of the high byte depends on the program configuration.

2.2. Installing the L-502 in your computer

The L-502 module can be installed in any PCI Express card slot of any size (x1, x2, x4, x8, x12, x16 and x32) from 1.0 to 3.0.

Before installing the L-502 in the computer, set the configuration jumper to the desired position, i. 2.1.

To install, and also to remove L-502 is allowed only when the computer's system unit is de-energized. "Hot connection" is not supported!

It is recommended to install L-502 in the system block with good air circulation in the interior.

It is recommended to avoid electrostatic discharges during the installation of L-502 in the computer. When handling the L-502, keep the module behind the metal panel.

It is not recommended to install the L-502 in an adjacent slot next to the heating radiator of an adjacent module, for example, in the vicinity of a powerful graphics card.

The two 6-threaded screws on the L-502 bracket must be tightened securely, make sure of this before installing the L-502.

The design of the L-502 is in strict accordance with the requirements of the PCI Express specification. But in the real case, it is also important: the quality of the computer chassis, the errors in installing the motherboard in the computer, the design features of the particular motherboard, the design features of the card in the adjacent slot. Due to a combination of these factors when installing L-502, you may encounter contacting the radiators of the motherboard (and other structural elements) with the internal electrically conductive elements L-502. It should be specially noted:

! Do not touch the L-502 conductive elements with any other electrically conductive elements of the motherboard or adjacent PCI/ PCI-E cards.

! It is not allowed to operate the L-502 with an unsupported bracket. The standard mounting screws for the card brackets (or plugs) are usually included in the computer case kit.

2.3. Function of the status LED on the front panel.

In the usual case, the LED on the front panel indicates the following statuses of the module:

LED status	Description
Red light	L-502 is on and in the synchronous I/O standby mode.

Green light	L-502 is in the synchronous I/O mode.
No lights	Power is off.

If more than one L-502 module is used in the computer's system unit, the task is to identify the module with which the program is currently running. To solve this problem, the software function of controlling the red glow of the LED is provided. Naturally, the same problem can be solved by software reading the serial number of the module, however, a comparison with the number punched on the board will require the opening of the system unit, which is inconvenient for operation.

2.4. Serial number. L-502 version number. Module identification in a multi-module configuration

The unique eight-digit product serial number item 1.3, page 11 serves to identify the module instance throughout the life cycle. The L-502 serial number is program-accessible.

The first digit of the serial number corresponds to the version number of the product L-502. The product version is changed to improve the design and technological characteristics during the production "life cycle" of the product. All versions of L-502 are programmed and functionally identical.

The task of module identification in a multi-module configuration arises because PCI Express (as well as PCI) -interface historically has never had a software binding to the physical position of the module in the slot line, and this binding occurs in operating systems when the system is initialized. If the composition of the equipment has not changed (and all the equipment remains operative), then there is a hope that the assignment of resources in the system during the initialization should occur from one computer to another. But in order to reliably compare a particular instance of the module and its assigned address *in a multi-module user program, it is necessary to bind to the serial number of the L-502 module.*

2.5. Software installation

To install the necessary drivers and libraries for Windows OS, you must download and run the installer "L-Card L502 / E502 SDK" http://www.lcard.ru/download/lpcie_setup.exe.

For information on installing the driver and libraries under Linux OS, see the Programmer Guide, http://www.lcard.ru/download/x502api_en.pdf.

Chapter 3. The device and principle of operation L-502.

3.1. Conventions

3.1.1. Convention on numbering

In all products of the L-Card, the numbering of all physical objects (for example, channel numbers) in the description of the principle of action and design is always made from one!

This agreement is completely unrelated to the encoding method in programming, where the numbers of these physical objects can be encoded from scratch or otherwise, in the context of the corresponding library function or programming language.

3.1.2. The assumption on the concept of "frequency"

In the documentation for L-502, the frequency of discrete signals (for examples, synchronization signals) is expressed in Hertz, rather than in periods per second, as is customary in the classical sense of frequency for a non-sinusoidal process.

3.1.3. The agreement on the terms "card", "board" and "module"

Literary PCI or PCI-E is translated as a card (in this case, even a L-card ☺). But many call it a board. Following the terms, in this manual we will adhere to the more strict name of this constructive unit, adopted in the ESKD - module. In particular, we will start from this point by using the term "multimodule synchronization".

3.2. Introduction (L-502 concept)

For the users who have already used L-780(M), L-783(M), L-761, L-791, the new device L-502 looks more like the development of this product line (L-7xx) at the new technical level. On the other hand, it can not be asserted that L-502 is an analog of one of these products or that L-502 is the mechanical sum of all the best characteristics of these products. Most likely, the L-502 project is the result of an analysis of the user needs in the market segment of the above products and the result of an engineering compromise at a modern technical level, where the most popular characteristics in this product line were first taken into account for most applications in order to obtain the best price-quality ratio.

L-502 has 6 modifications (fig. 1-1, item 1.1) which are based on the same multilayer printed board. Modification is achieved by different variants of the factory assembly. If you previously purchased an L-502 without a DAC, then the L-Card accepts orders for the installation of a DAC. The remaining options for subsequent changes of the L-502 modifications are not considered technically feasible.

The presence of the ADSP-BF523 signal processor with RAM (modification L-502-P-▒-▒) is considered justified for those users who want to get a maximum of on-board signal processing capabilities on-board, as well as advanced users to have their own low-level processor programming, possibly using a JTAG emulator.

The presence of galvanic isolation (modification L-502-▒-G-▒) is considered necessary if the sources of L-502 input signals and the load circuit of the output signals are not isolated from the ground and, at the same time, directly (electrically short) are not connected to the case of the system unit. The galvanic isolation in L-502 provides isolation of all circuits on the contacts of the internal and external signal connectors and the inter-module synchronization connector (fig. 1-3) relative to all circuits of the computer. The signal chains are not isolated between each other.

The presence of a 2-channel DAC (modification L-502-▒-▒-D) is necessary if in your task it is necessary to reproduce the output analog voltage levels or temporary voltage functions.

ADC 16 bits with a conversion frequency of up to 2 MHz with 16/32-channel circuit switching (up to 16 differential channels, up to 32 with a common ground) with voltage subbands ± 10 V, ± 5 V, ± 2 V, ± 1 V , ± 0.5 V, ± 0.2 V has an analogue path improved with regard to L-7xx for the following parameters:

- The resolution of the ADC is increased and the signal-to-noise ratio is improved due to the increase in the ADC bit depth, the quality of the analog path, and also at low data acquisition frequencies due to the built-in hardware averaging of the sample data within the same channel scan cycle.
- The interchannel passage for the same test conditions is reduced together with L-7xx: the same impedances of signal sources and channel switching frequency. In particular, the advantage of L-502 on lower sub-ranges of voltages of ± 0.5 V, ± 0.2 V is gigantic with regard to L-7xx for the same application conditions.
- The range is ± 10 V compared to ± 5 V in L-783 (M).

Along with the obvious progress in the characteristics of the ADC in L-502, there are trade-offs in the following characteristics with regard to L-7xx:

- Maximum ADC conversion frequency is limited by 2 MHz (in L-783(M) – 3 MHz).
- Limited to ± 1 V operating range of the input signal at the inputs Y and GND32 (for details, see 4.4).

Instrumental DAC 16 bits 2 channels ± 5 V compared to DAC 12 bits in L-7xx has a much better resolution, a larger working output current, normalized high-speed transients associated with the transition from one sample to another, which allows using this DAC in applications, the quality of the functional generator required from the DAC[4]. Synchronous (streaming) up to 1 MHz per channel or asynchronous mode on the selected DAC channel is possible, including mixed synchronous-asynchronous mode on different channels.

Digital input, up to 18 lines, synchronous mode up to 2 MHz or asynchronous. In synchronous mode, the stream from digital lines is synchronous with the ADC stream, but separate and independent of the settings of the ADC data collection frame (the frequency of data collection by digital lines is set separately and does not depend on the ADC frame settings). Programmable pull-up resistors to a high logic level on digital inputs.

Digital input, 16 lines. Synchronous as synchronous output up to 1 MHz, and asynchronous is possible. With synchronous output, the frequency is matched to the frequency of the DAC output. The output enable allocated for the low and high byte increases the flexibility of using digital lines,

[4] Strictly speaking, for qualitative sound applications to the DAC, even more stringent requirements are imposed in comparison with the requirements for the function generators.

for example, configuration is possible: 8-bit 2-way data bus + up to 10 data bits per input + up to 8 data bits per output. This allows the implementation of bus diagrams controlling complex digital devices (item 4.2.3.1, p. 38).

Note the limitations of the asynchronous output for external synchronization (n.3.3.4.1).

The ADC, DAC, digital input and output streams are synchronized with respect to the same $\mathbf{f_{ref}}$ reference frequency, which can be assigned programmatically: 1.5 MHz or 2 MHz.

Hardware-based in L-502, the physical conversion frequency of the ADC and synchronous digital input is always equal to $\mathbf{f_{ref}}$, and the physical refresh rate of each DAC channel and digital output is $\mathbf{f_{ref}}/2$. Getting all the fractional frequences of the data input $\mathbf{f_{ref}}/n$ and $\mathbf{f_{ref}}/2m$ output fractional frequencies (where m and n are natural numbers) occurs at the hardware processing level in the FPGA and/or in the Blackfin processor.

L-502 has a mechanism of inter-module (n.3.1.3) synchronization to form a single synchronous input-output system. Physically, the maximum possible number of L-502 synchronized modules is equal to the number of consecutive free PCI-e slots (of any size) in which L-502 modules are to be installed and the adjacent modules are connected by synchronization cables (the cables are not included in the main kit, they are bought separately). Programmatically, the first L-502 module in the generated synchronization chain is assigned to the master, the others to the slaves. Intermodular synchronization can be arranged for L-502 modules of any modifications, including between L-502 different modifications. It is important to note that if at least one L-502, used in the multi-module synchronization scheme, does not have a galvanic isolation, then all other L-502s lose their galvanic isolation in this scheme (item 4.2.4.1, p.39).

The L-502 has a 32-bit data word format, in which, besides the actual data for input or output, there is also a physical channel number. This hardware binding of the physical channel number ensures that the channel number is mistaken even if the top-level program for some reason lost an arbitrary amount of data.

The PCI Express interface, compared to the PCI interface, has significant user benefits associated with reliability: low-level network protocol PCI Express has a built-in error control and correction mechanism, invisible at the program level. At the same time, the PCI Express device in the BIOS of the computer is seen as a PCI-device, which basically allows to use the L-502 in all operating systems, starting with DOS!

The BUS MASTER mode used in the L-502 allows you to transfer streaming data to the input and output without the processor on the computer (the data is transferred between the RAM of the computer and L-502 only with the resources of the bridge, the chipset of the computer), while the L-502 module itself is a setup unit (master) of the process of data transfer. This is a cardinal advantage with respect to L-783 (M) in terms of unloading the processor in the computer by streaming data transfer operations. And for a multi-module BUS MASTER system is vital!

For advanced users: HOST DMA access mode to the internal memory of the signal processor ADSP-BF523 allows you to apply an independent access channel to the Blackfin internal memory. This creates a huge convenience - "transparency" with low-level Blackfin programming - to see what happens in Blackfin memory on an independent channel. To some extent, HOST DMA can replace JTAG. By the right convenience of the technology of the independent access channel to the memory of the signal processor was evaluated by users even in products E-440 / E14-440 from L-CARD!

3.3. Operation principle

In the section 3.2 the concept of the L-502 project was summarized, where the main principles of the module operation were listed. This section contains further details.

3.3.1. Reference frequency

f_{ref} – a signal reference frequency, from which the conversion processes are synchronized to the ADC, DAC, digital input and digital output. The L-502 uses a common reference frequency that synchronizes the start-up of the ADC, DAC, digital input and digital output to an accuracy of an integer division of this frequency. In L-502, the reference frequency source can be internal (2.0 or 1.5 MHz) or external (with a frequency of not more than 2.0 MHz). In particular, the reference frequency from the adjacent L-502 module can be used to form a synchronous multi-module system.

3.3.2. ADC channel.

The analog data input channel is a channel with dynamic switching of up to 32 input physical analog channels of the L-502 module to the input of a single internal ADC module. The process of switching channels itself is hardware, according to a pre-configured control table. The input process itself is conditionally divided into periodically alternating frame periods and interframe delay with pre-configured durations of these periods (interframe delay, in particular, can be set to zero). Duration of frame, interframe delay, ADC output sample timing - all these times can be configured, but they are always a multiple of $t_{ref} = 1/f_{ref}$ - the period of the synchronization reference frequency.

$t_{sw} = n_{sw} / f_{ref}$ – the ADC channel commutation period within the frame, equal to the sampling period of the ADC readouts, where n_{sw} can be specified by an integer from 1 to 2097152

The preset number of samples in the frame and the size of the control table $n_к$ can be set from 1 to 256. In each cell of the control table, the physical number of the ADC polling channel is prescribed. Within the frame, the control table will be read completely: from the 1st to the n_{th} cell and the read sequence of physical channels will be used in the hardware control mechanism of the channel switch.

The cell number of the control table is called the logical channel number. Accordingly, logical channels can be up to 256, and physical - up to 32. For example, it gives the opportunity to obtain a different frequency of polling different physical channels within the frame.

Frame time: $t_k = n_к * t_{sw} = n_к * n_{sw} / f_{ref}$

If necessary, between intermittently following frames, a non-zero interframe delay t_d with a duration n_d of synchronization frequency periods can be inserted:

$t_d = n_d * t_{ref} = n_d / f_{ref}$, where n_d can be set with an integer from 0 to 2097151

The frame period is equal to the sum of the frame length and the interframe delay:

$t_{ch} = t_k + t_d = n_к * n_{sw} / f_{ref} + n_d / f_{ref}$

In other words, the frame period t_{ch} is equal to the period of data collection from the same logical channel of the control table.

During interframe delay, the sample of control words does not advance, and the analog channel switch is always set in accordance with the first cell of the control table.

Frequency of collection from one logical channel of the control table

$f_{ch} = 1/ t_{ch} = f_{ref} /(n_к * n_{sw} + n_d)$,

where $\mathbf{f_{ref}}$ can be 2.0 or 1.5 MHz for an internal synchronization or ≤2.0 MHz for an external, $\mathbf{n_к}$ = {1,2,…, 256}, $\mathbf{n_{sw}}$ ={1,2,…,2097152}, $\mathbf{n_d}$ ={0,1,…,2097151}.

The above-mentioned frame structure of the ADC data is shown in fig. 3-1. Here, for example, a 3-channel ADC mode operation ($\mathbf{n_к}$ = 3) is taken with a non-zero interframe delay $\mathbf{t_d}$.

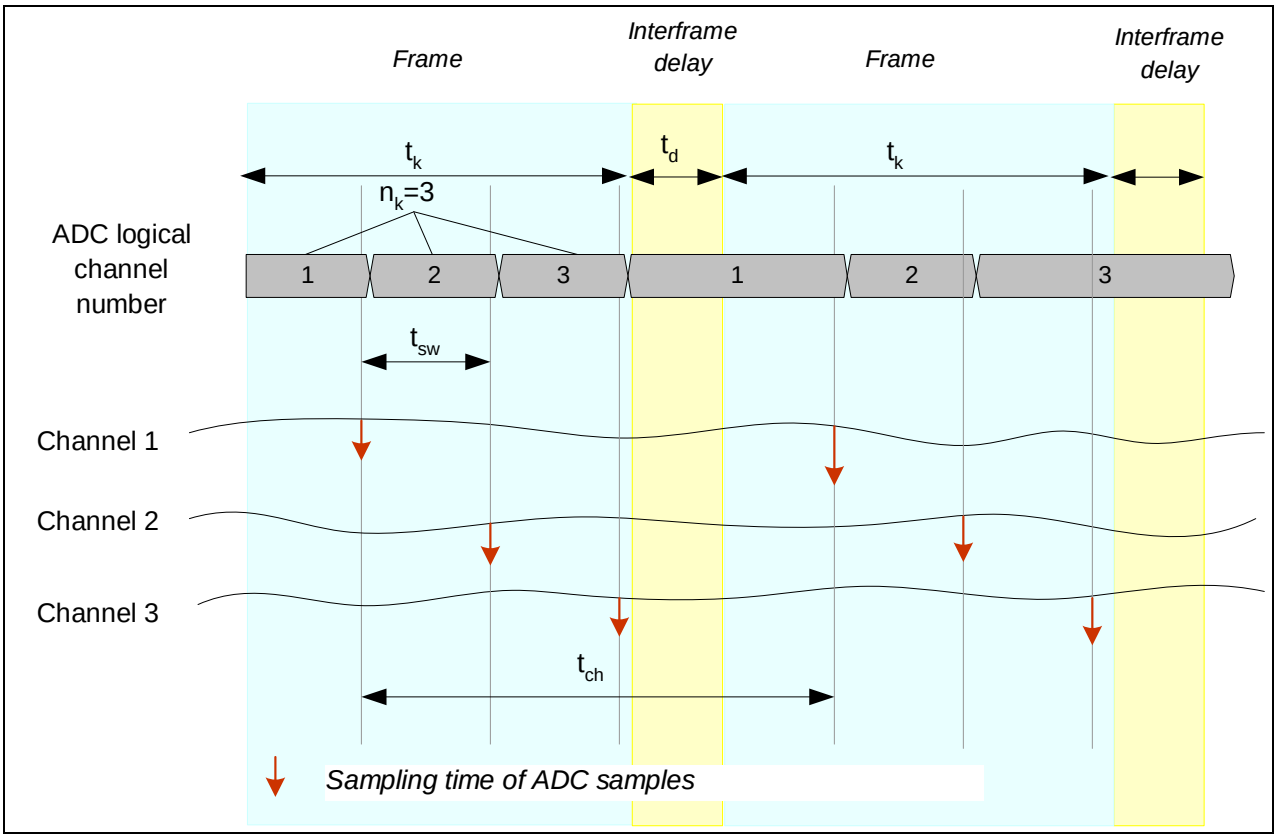


Fig. 3-1. Illustration of the personnel principle for acquiring ADC data

3.3.3. Digital input channel.

Synchronous digital input occurs with a period of $\mathbf{t_{ref}} * \mathbf{n_{din}}$,

where $\mathbf{n_{din}}$ ={1,2,…,2097152} is a configurable frequency division factor for synchronous digital input

3.3.4. Digital output and DAC channels

Synchronous digital output, as well as updating both channels of the DAC, occurs with a period of 2* $\mathbf{t_{ref}}$. If the data buffer for the output and the DAC is empty, then the last value is held at the outputs.

3.3.4.1. Restrictions on the current implementation of asynchronous output during external synchronization.

Asynchronous output to digital lines and to DAC in the operating mode will always work when configured for internal synchronization. But asynchronous output to digital lines and to the DAC will not function in the standby mode for external synchronization of the start of data acquisition or waiting for more than 1 μs of the external clock of the ADC conversion.

3.3.5. General principle for synchronization in L-502.

A simplified block diagram is presented on fig. 3-2 to explain the general arrangement of the synchronization system in L-502. L-502 synchronization system consists of two parts: primary and secondary synchronization circuits.

3.3.5.1. Primary synchronization.

The primary synchronization circuit *(I)* according to the settings selects the corresponding external or internal source of the reference frequency, as well as the external or internal source of the start signal. Using the selected signals, circuit ***I*** generates an internal reference signal $\mathbf{f_{ref}}$ as a sequence of synchronization pulses with a period $\mathbf{t_{ref}}$. Moreover, the beginning of this sequence is strictly bound by this scheme to the external or internal *start event*, and all I/O equipment is synchronized (and simultaneously starts) from this sequence: nodes of the ADC (including the logic of the control table), DAC and digital I/O. These nodes contain the corresponding frequency dividers $\mathbf{f_{ref}}$.

We list all possible options for user settings related to the *selection of sources of reference frequency signals*:

- The internal generator 2.0/1.5 MHz of this module L-502 (the "default" setting)
- The reference frequency from the DI_SYN1 input (on the front or on the drop)
- The reference frequency from the DI_SYN2 input (on the front or on the drop)
- The reference frequency is from the CONV_IN input from the neighboring L-502, which acts as the master.

We list all possible options for user settings for *selecting sources of the start event of the L-502* I/O system:

- Program start from PC (default setting)
- On the signal from the input DI_SYN1 (on the front or on the drop)
- On the signal from the input DI_SYN2 (on the front or on the drop)
- By the signal from the input START_IN from the neighboring L-502, which acts as the master.

Each L-502 module always translates via its CONV_OUT and START_OUT outputs, respectively, its internal reference and start signals for one L-502 slave module, if it is connected to these outputs via a *synchronization cable* and is located in the neighboring PCIe slot of the PC system unit.

The L-502 module can simultaneously be the master for the neighboring L-502 located on one side of this PCI-E slot and slave for the other neighboring L-502 on the opposite side. Thus, synchronization of several L-502, connected by a chain, is supported in an amount limited by the number of PCI-E-s of one PC motherboard.

The primary synchronization circuit provides synchronization of the frequency and phase of the ADC, DAC and cycle cycles of the digital input and output system. It is understood that in a

multi-module synchronization system, the user will be able to intelligently set the control tables of different modules, as well as the division of the reference frequency for the required input-output processes.

Note that for the slave L-502 there is a frequency limitation on the input CONV_IN - no more than 1.5 MHz. Thus, two or more L-502 slave modules can be synchronized only at a reference frequency of 1.5 MHz from the master.

Stopping the primary synchronization scheme is done only programmatically and asynchronously.

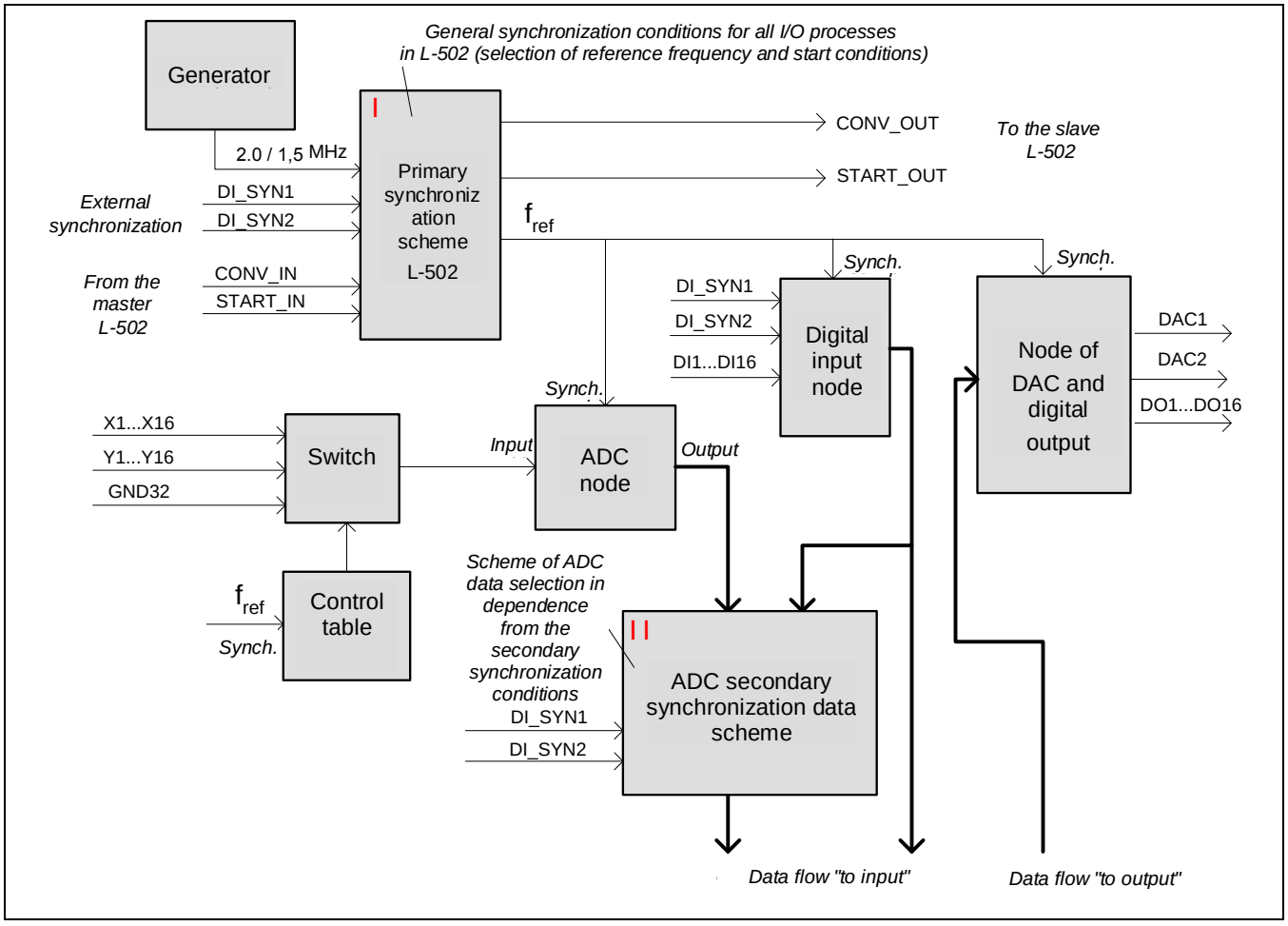


Fig. 3-2. L-502 synchronization system structure

3.3.5.2. Secondary synchronization.

The functionality of the secondary synchronization is embedded in the project, but is not currently implemented. You can find out about the availability of this functionality in the sales department of L-Card.

The secondary synchronization circuit *(II)* is the ADC data selection circuit depending on the secondary synchronization conditions, operating exclusively against the background of the previously started clock signal from the output of the primary synchronization circuit (***I***), i.e. against the background of the started data stream of the ADC.

The following ADC data resolution synchronization modes are supported:

- No synchronization (transparency mode)
- Synchronization from an analog signal in the selected ADC channel
- Digital synchronization with the selected signal from the inputs DI1 ... DI16, or DI_SYN1, or DI_SYN2

The following modes of sensitivity to the fluctuations of the synchronization signal are supported:

- Enable of ADC data *on the edge (drop)* of an analog or digital signal
- Enable of ADC data at *a level* "above the threshold" or "below the threshold" (for analog synchronization) or *at the logic level* "1" (for digital synchronization)

The following ADC data inhibit modes are supported:

- Software prohibition (stop) with the possibility of re-authorization (if the previously set enable condition is repeated) without restarting the primary synchronization scheme
- Automatic prohibition (stop) after entering the specified number of frames (from 1 to 2^{32}-1 frames) with the possibility of re-authorization (if the previously set resolution condition is repeated) without restarting the primary synchronization scheme

3.3.6. Setting the ratio between the time of setting the signal and the resolution for each channel of the ADC is a unique possibility of the L-502!

Above was the principle of the frame-by-line input of ADC data, which was applied in all L-CARD ADCs with the input channel switch, up to synchronization frequency, frame size and interframe delay. But with L-502 this principle is developed for better adaptation to the output physical properties of the signal source. Further we will discuss it more precisely.

If L-502 is used at the highest possible data acquisition frequency from each channel, then set $\mathbf{n_{sw}} = 1$, which means that the sampling period of one measurement channel is $\mathbf{t_{sw}} = \mathbf{t_{ref}}$, during which only one ADC sample is converted. For example, for $\mathbf{f_{ref}}$=2 MHz time$\mathbf{t_{sw}} = \mathbf{t_{ref}} = 0{,}5$ µs is a fairly short switching period of the channel switch, which imposes restrictions on the output impedance of the signal source (and the wires from it): the impedance should be sufficiently small (not more than 50 Ohm) and not have a large reactive component, so that the duration of the transient process caused by circuit switching does not exceed 0.5 µs. In other words, the signal source should be no more than 50 Ohm and have a short or coordinated cable. For those who used the L-783, these requirements and these conditions of use roughly correspond to the conditions of application of the L-783 in the multichannel mode with the maximum ADC conversion frequency of the 3 MHz, but with the difference that the L-502 ADC's resolution is 16 bits, not 12, and the electronic switch in L-502 is much more "quiet" (i.e. it injects a significantly smaller parasitic charge into the signal chain at the time of commutation, and therefore causes a significantly smaller shock excitation for a possible transient process in the signal circuit).

But if you want to use L-502 at a data acquisition rate for each channel less than the maximum, and you can reduce the switching frequency, then in L-502 with internal synchronization there is no reduction in the frequency of ADC startup, and $\mathbf{n_{sw}} > 1$ is set, for example, as it is shown on fig. 3-1. But, in the sense of $\mathbf{n_{sw}}$ – this is the number of cycles of ADC conversion for one

switching period. L-502 has, by default, that for $\mathbf{n_{sw}} > 1$ all ADC readouts are flipped, except for the last one, during the switching period - this creates the greatest time for setting the signal after switching (due to "idle" ADC conversion cycles), therefore the least stringent requirements are imposed to the impedance of the signal source. On fig. 3-3, with $\mathbf{n_{sw}}$ =3, such conditions are set "by default" for the logical channel 1: the first two counts are always discarded, and the third one is used. But the real tasks of using multichannel ADCs do not assume that the impedances of the signal sources are the same, and for channels with connected low-impedance sources it would be good not to discard at least some of the ADC samples, but to use them for averaging the data, thereby increasing the enable when measuring this channel. This possibility is provided in L-502 due to the fact that in every cell of the control table, besides the physical channel number, there is also the averaging factor $\mathbf{n_{av}}$, by default, $\mathbf{n_{av}}$= 1. Averaging factor $\mathbf{n_{av}}$ ={1,2,…,128} means: "how many counts of the ADC from the end of the switching cycle of this channel will be used to averaging the data". Accordingly, $\mathbf{n_{su}} = \mathbf{n_{sw}} - \mathbf{n_{av}}$ means "how many ADC counts from the beginning of the switching cycle of the given channel will be discarded", or "how many periods $\mathbf{t_{ref}}$ will be used to set the signal at the ADC input after switching".

For example, on fig. 3-3 for navigational channel 2, $\mathbf{n_{av}}$ = 2 is installed in the control table, which means that for $\mathbf{n_{sw}}$=3 the result of the last two conversion periods in one switching phase will be used for averaging, and one first period is added to the time of signal establishment after switching. For logical channel 3, all three samples of the ADC are used for averaging, and therefore the minimum time is assigned here to establish a signal after switching.

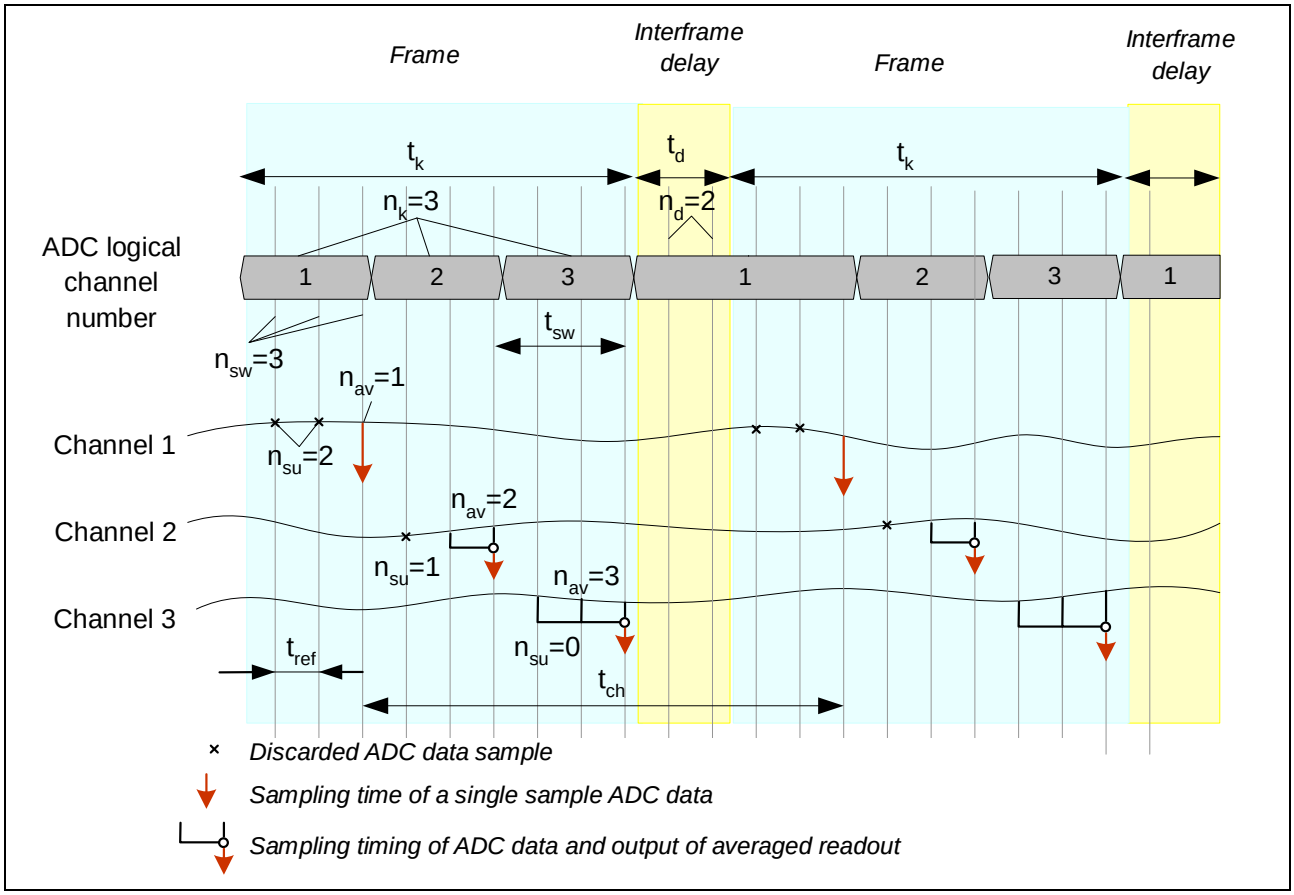


Fig. 3-3. The principle of obtaining ADC data (in detail)

From fig. 3-3 it also follows that the set non-zero interframe delay actually increases the settling time for the first logical channel. This can be used, for example, by associating the first logical channel with the physical channel to which the signal source is connected by the largest impedance.

It can be argued that by setting optimal $\mathbf{n_{su}}$ / $\mathbf{n_{av}}$ settings for each channel, we are trying to optimize the *timing of the signal conditioning* associated with the inter-channel passage and the *resolution of the ADC*.

It is important to note that in the L-502, the ADC averaging algorithm described here (by the simple average method) is considered as an inseparable part of the analog-to-digital converter itself, although physically the averaging procedure is performed by means of FPGA using 24-bit integer arithmetic.

Such an averaging operation increases the real resolution of the ADC by suppressing the random components of the signal of different nature, improves the signal/noise by suppressing the high-frequency components of the spectrum above the Nyquist frequency of 0.5*$\mathbf{f_{ch}}$ for a given physical channel associated with one (or more) logical channel. Note in passing that digital filtering by the Blackfin processor (or high-level software) has a fundamentally different active filtering area, because it is below the Nyquist frequency.

Once again, we emphasize that "default" settings of L-502 have $\mathbf{n_{av}}$=1, and there is no averaging process "by default".

3.3.7. Relative switching delays in ADC channels.

This information will be important only for that class of multi-channel data acquisition tasks where the magnitude of the relative signal delay between the ADC channels is important for measuring relative phase delays. For this class of problems, the theoretical calculated latency values in the ADC channels are taken into account in the delay equalization algorithm based on one or another method of signal interpolation.

For ADC mode without averaging ($\mathbf{n_{av}}$=1), the relative switching delay between adjacent ADC channels within one frame (in the order of polling the control table) is equal to $\mathbf{t_{sw}}$, and between the last channel of the previous frame and the first channel of the next one is $\mathbf{t_{sw}}$ + $\mathbf{t_d}$.

If the averaging mode is used ($\mathbf{n_{av}}$>1), where $\mathbf{n_{av}}$ are selected equal for all ADC channels, the absolute delay for each channel will decrease by the same amount 0.5*$\mathbf{n_{av}}$*$\mathbf{t_{ref}}$. Therefore, the relative delay will remain equal to $\mathbf{t_{sw}}$ between neighboring channels of one frame and equal $\mathbf{t_{sw}}$ + $\mathbf{t_d}$ between the nearest channels of neighboring frames separated by interframe delay.

If the averaging mode is used ($\mathbf{n_{av}}$>1), where $\mathbf{n_{av}}$ are assigned in the control table different for i- and j-th logical ADC channel, the absolute signal delay on the i- channel will decrease by 0.5$\mathbf{n_{av}}$(i)*$\mathbf{t_{ref}}$, and the relative delay j channel towards the previous i- (within one frame) becomes $\mathbf{t_{sw}}$ + 0,5* $\mathbf{t_{ref}}$ ($\mathbf{n_{av}}$(i)- $\mathbf{n_{av}}$(j)), or becomes equal to $\mathbf{t_{sw}}$ + $\mathbf{t_d}$ + 0,5* $\mathbf{t_{ref}}$ ($\mathbf{n_{av}}$(i)- $\mathbf{n_{av}}$(j)) between the nearest i-th and next j-th channels of neighboring frames separated by interframe delay (if more precisely, for the last channel in the frame always i = $\mathbf{n_k}$, and for first, always j = 1).

3.3.8. Relative delays of the ADC, DAC and I/O channels.

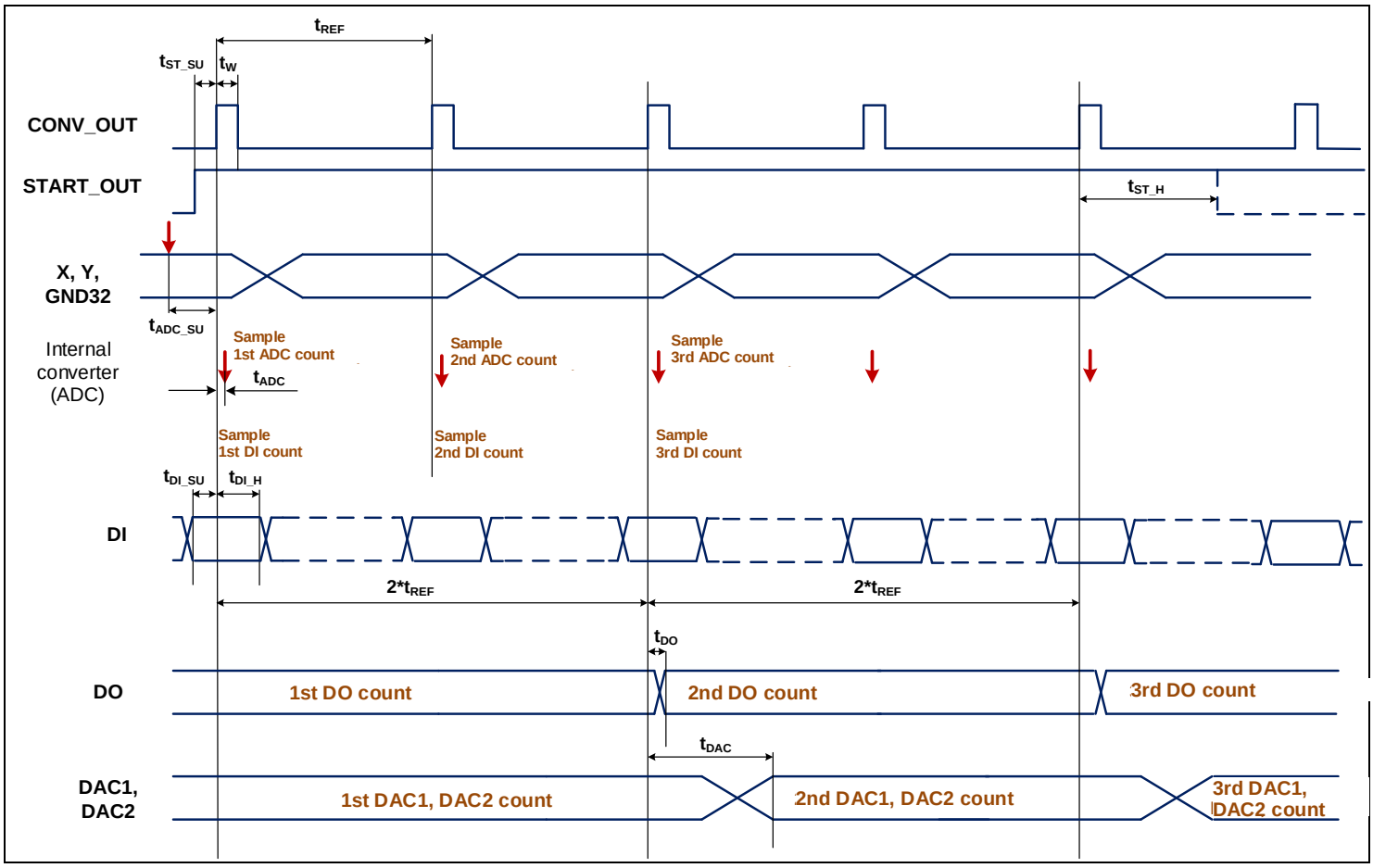


Fig.3-4. Synchronous I/O diagram

In the above-mentioned synchronous I/O diagram, the output signal CONV_OUT is used as a reference clock signal, with respect to which all I/O delays are described. Temporal parameters of the diagram are described in the table below. The delays in the ADC channel are given for the operating mode without averaging the data and without allocating additional cycles of the ADC for setting the signal

Description	**Desig-nation**	**Timing sample**		
		Minimum	**Typical**	**Maximum**
Reference frequency period	t_{REF}		500 ns (2 MHz) 667 ns (1.5 MHz)	
Duration of the signal pulse CONV_OUT	t_W		50 ns	
Group delay time of analog path of ADC channel in L-502	t_{ADC_SU}		15-70 ns	
The delay time from the front CONV_OUT to the sampling time of the ADC chip	t_{ADC}		0 ns	

Description	Desig-nation	Timing sample		
		Minimum	Typical	Maximum
The time to set the state "1" to START_OUT before the front CONV_OUT (start of data collection)	t_{ST_SU}	45 ns		
Hold time of state "1" to START_OUT after the front CONV_OUT (termination of data collection)	t_{ST_H}	150 ns		
The time to set the data at the DI input	t_{DI_SU}		5 ns	
Data hold time at the DI input	t_{DI_H}		-1 ns	
DO delay time relative to the front CONV_OUT	t_{DO}		6 ns	
The group delay time of the signal at the output of the DAC relative to the front CONV_OUT	t_{DAC}		0,7 µs	

3.4. Operation principle and function circuit

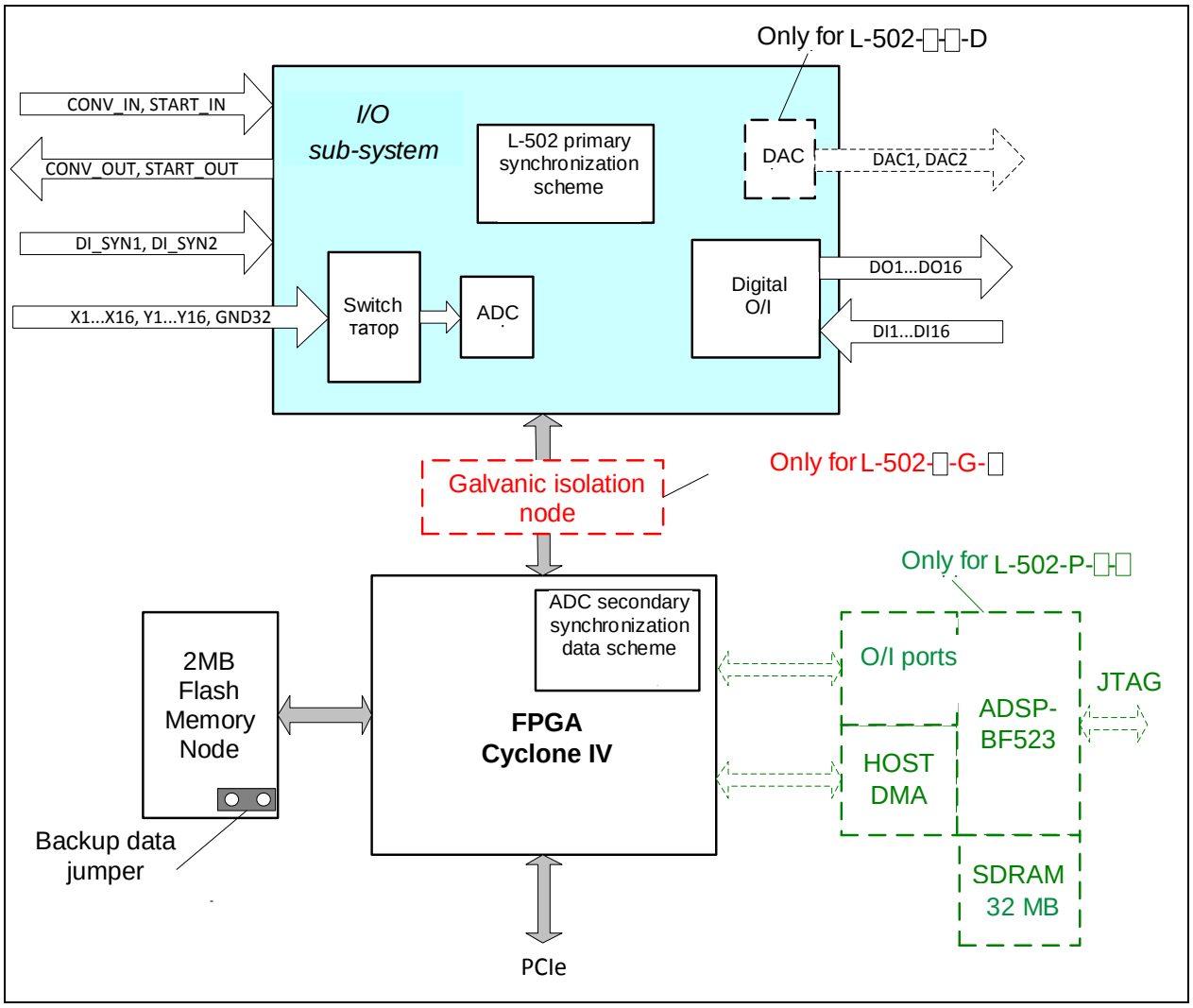


Fig. 3-5. Block diagram

FPGA is the basic logical element in the L-502, in which all the interface functions, the hardware logic of ADC calibration, and the logic of the *secondary synchronization* are concentrated (3.3.5)

Flash-memory with a capacity of 2 MB is designed to store the main and backup firmware FPGA, calibration factors, serial number. Half the amount of Flash memory is provided for user tasks.

The L-502 I/O subsystem includes nodes for the channel switch, ADC, DAC (L-502-▒-▒-D), digital I/O, and *primary synchronization* circuit (3.3.5).

The galvanic isolation unit (L-502-▒-G-▒) isolates all circuits of the I/O subsystem from circuits connected electrically to any circuits of the computer.

The ADSP-BF523 signal processor (L-502-P-▒-▒) is designed for additional data processing and control. If the processor is enabled, the entire data stream and the I/O subsystem are transferred through the processor's I/O ports. For example, it is possible to create a control loop through a

signal processor. The interface of the processor with the computer is through the HOST port of the DMA processor.

The signal processor has 32 MB SDRAM (L-502-P-▒-▒).

When the computer's power is turned on, before the BIOS of the computer starts initializing the devices, the L-502 will download the firmware to the FPGA from Flash memory (fig. 3-5), and the L-502 internal power supply system will be fully turned on. In this case, the option of loading the main/backup firmware will depend on the status of the backup boot jumper (sec. 2.1.1).

After loading the FPGA, the L-502 becomes a PCI Express device, which will be assigned the appropriate system resources when the OS is initialized.

Chapter 4. Connection of signals.

This chapter provides information on the L-502 connectors, the assignment of their contacts, and the main characteristics of the L-502 inputs and outputs related to the correct connection.

4.1. GND, DGND, AGND circuits.

L-502 has the following the following conventions for earth circuits (or "common wire" circuits for an interface):

GND is the ground circuit of the computer's system unit, electrically connected to the computer chassis, with the computer's mains plug ground, the GND circuit of the computer's motherboard, with the GND PCI Express circuit.

AGND is a "common wire" circuit of analog circuits: ADC inputs and DAC outputs.

DGND is a circuit of the "common wire" of digital circuits: digital inputs and outputs.

! In any modification of the L-502, the AGND and DGND circuits have a common connection point inside the L-502

In L-502-▒-X-▒ (without galvanic isolation) the GND circuit has an internal connection point with DGND, which in turn is connected to AGND.

In L-502-▒-G-▒ (with galvanic isolation), DGND-AGND circuits are isolated from GND and all other circuits of the computer, and the DGND and AGND circuits have a connection point inside the L-502.

4.2. L-502 connectors description.

4.2.1. L-502 external signal connector.

The external signal connector is a 37-pin 2-row type DRB-37M plug that extends outward when the L-502 module is installed inside the PC unit. The bracket L-502 is directly fixed to the DRB-37M connector with 6-point screws.

The conductive contact of the connector (screen) is always electrically connected to the computer case (GND circuit).

4.2.2. Connecting the cable shield.

On the casing of the cable part of the DB-37F signal connector it is possible to directly seal the screen of the signal cable for any modification of the L-502, however, as shown by the L-502 practice, **the best signal-to-noise ratio is obtained by connecting the cable shield to the AGND signal connector** (there are no connections to the connector housing).

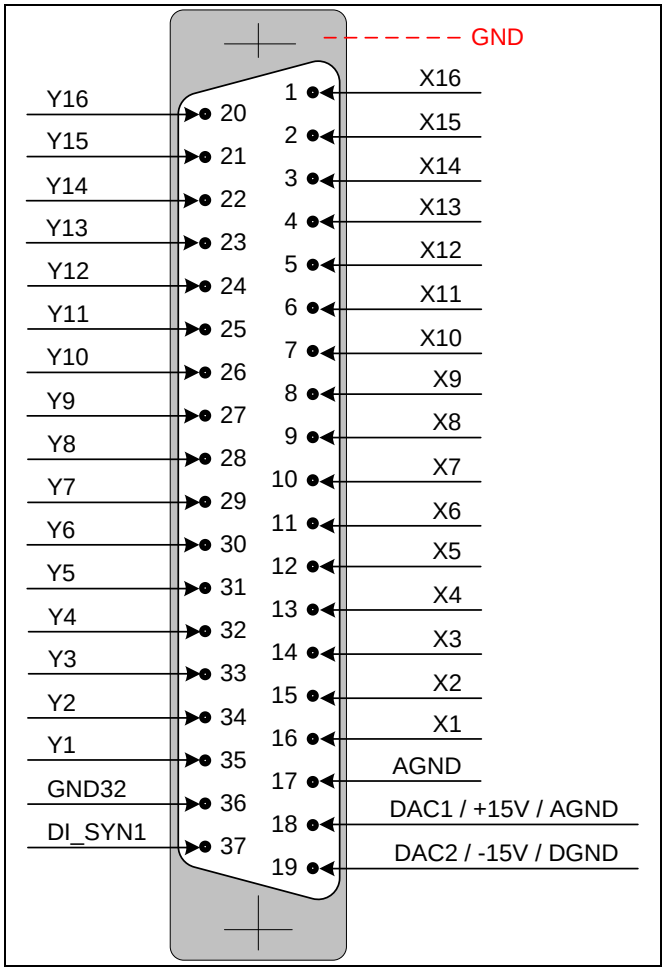


Fig. 4-1: Eternal signal connector

Table 4-1: Eternal signal connector

Signal name	Common point[5]	Direc-tion	Description
X<1…16>	AGND	Input	• Non-inverting channel voltage input 1 ... 16 for differential and "common ground" mode: • Operation voltage range: **±10 V (**see the details in section 4.4 p. 44). • Unused inputs X <1 ... 16> are recommended to be connected to AGND or the corresponding physical channel not to be interrogated programmatically.
Y<1…16>	AGND	Input	• Inverting channel voltage input 1 ... 16 for differential mode. • Input channels 17 ... 32 for the mode "with common ground". • Operation voltage range: **±10 V (**see the details in section 4.4 p. 44). • Unused inputs X <1 ... 16> are recommended to be connected to AGND or the corresponding physical channel not to be interrogated

[5] The common wire circuit for the specified signal input or output

Signal name	Common point[5]	Direc-tion	Description
			programmatically.
DAC1 / +15 V / AGND / not connected (see section 2.1.2)	AGND	Output	For modifications, the L-502-▒-▒-D can be configured with a jumper as the output of the 1st DAC channel (voltage output in the range -5 ... + 5 V). For any modifications, the L-502 can be configured with a jumper as + 15V output of an external device, or as an additional AGND contact, or as an unconnected pin contact. (see section 2.1.2)
DAC2 / -15 V / DGND / not connected (see section 2.1.2)	AGND	Output	For modifications, the L-502-▒-▒-D can be configured with a jumper as the output of the 2nd DAC channel (voltage output in the range -5 ... + 5 V). For any modifications, the L-502 can be configured with a jumper as an -15V output of an external device or as an additional DGND contact, or as an unplugged connector pin (see section 2.1.2)
AGND	—	—	Analog ground
GND32	AGND	Input	• In the "with common ground" mode: common inverting channel input 1 ... 32. • For all modes must be connected to AGND (in differential mode - to increase noise immunity). In the "common ground" mode, it is recommended to connect to the AGND on the signal source side. • Operation voltage range ±1 V (see the details in section 4.4 p. 44).
DI_SYN1	DGND	Input	Synchronization input 1, which can also act as an additional input to the digital input. Compatible with the output logic level of TTL/CMOS- cells with a supply voltage of +2.5 V to +5 V. The input has an extended range of maximum permissible voltages (± 10 V relative to GND). The minimum rate of rise of the signal drop at the input DI_SYN1 is not specified, since there is a Schmitt trigger on this input. There is a software option to turn the 1k pull-up resistor to a high logic level at this input. The DI_SYN1 input does not bypass the external TTL source, even when the power is off.

Notes to table 4-1:

- The maximum permissible voltages and currents at the contacts of the connectors are indicated in section 4.3, on p. 42.

4.2.3. Internal signal L-502 connector.

The internal signal connector means a 40-pin 2-row BH-40 type plug intended for connecting a flat cable inside the system unit. It is possible to use the finished AC-7xx-m or AC-7xx-f cable with the use of an additional adjacent crate slot in the PC system unit.

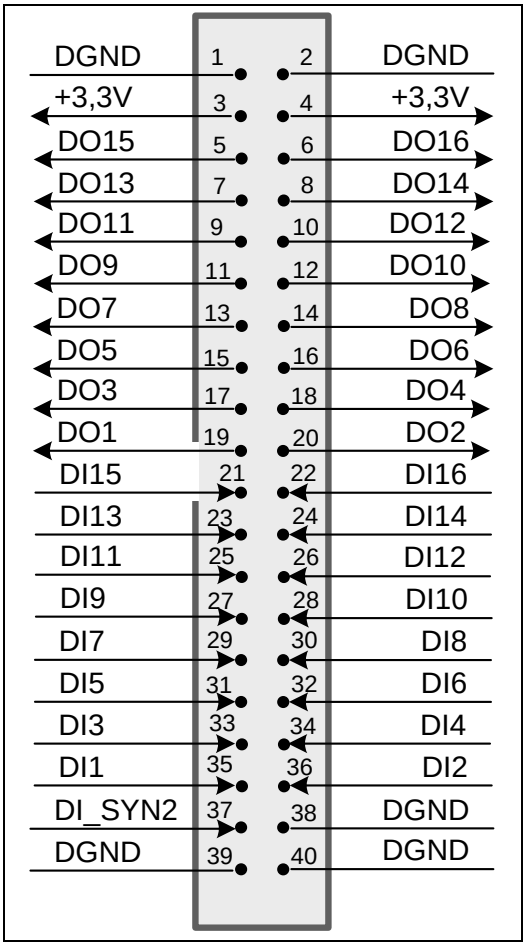


Fig. 4-2: Internal signal connector

Table 4-2: Internal signal connector

Signal name	Common point	Direction	State after connection	Description
DI<16…1>	DGND	Input	Input	16-bit digital input, where DI1 is the low bit, DI16 is the high bit of the 16-bit word. It is possible to programmatically turn the 2.2 kOhm pull-up resistors to a high logic level independently on the lines of the low and high byte. The DI_SYN2 input does not bypass the external TTL source even when the power is off.
DO<16…1>	DGND	Output	Z-state	16-bit digital output, where DO16 – high bit, DO1 – low bit of the 16-bit word. Lines DO1 ... DO8 refer to the low byte, and lines DO9 ... DO16 - to the high one. Program control Z- state is independent for the high and low bytes. It is possible to force the active state of the outputs of each byte when the power is turned on by installing jumper, section 2.1.3.
DGND	—	—	—	A common-wire circuit for digital inputs and outputs.
DI_SYN2	DGND	Input-output	Input	Sync input 2, which can also act as an additional input to the digital input. Compatible with the output logic level of TTL/CMOS- cells with a supply voltage of +2.5 V to +5 V. The input has an extended range of maximum permissible voltages (± 10 V relative to GND). Especially does not specify the minimum rate of increase of the signal drop at the input DI_SYN2, since there is a Schmitt trigger on this input. There is a software option to turn the 1k pull-up resistor to a high logic level at this input. DI inputs do not bypass the external TTL source even when the power is off.
+3.3 V	DGND	Output	Output +3.3 V	Output +3.3 V supply external digital nodes. Attention! In versions 1 and 2 of L-502 (serial numbers start with the digit "1" or "2"), the short circuit of the +3.3V output is inadmissible (it leads to failure of the L-502! In version 3, a short circuit of +3.3 V is permissible.

For the maximum permissible voltages and currents at the contacts of the connectors, see the section 4.3, on p. 42

4.2.3.1. What gives an independent resolution to the outputs of the high and low byte?

One of the important practical examples is a system of 3 buses with a width of 8 bits each, as shown in the figure below. The first bus is the input one, the second is the output bus, the third is bi-directional.

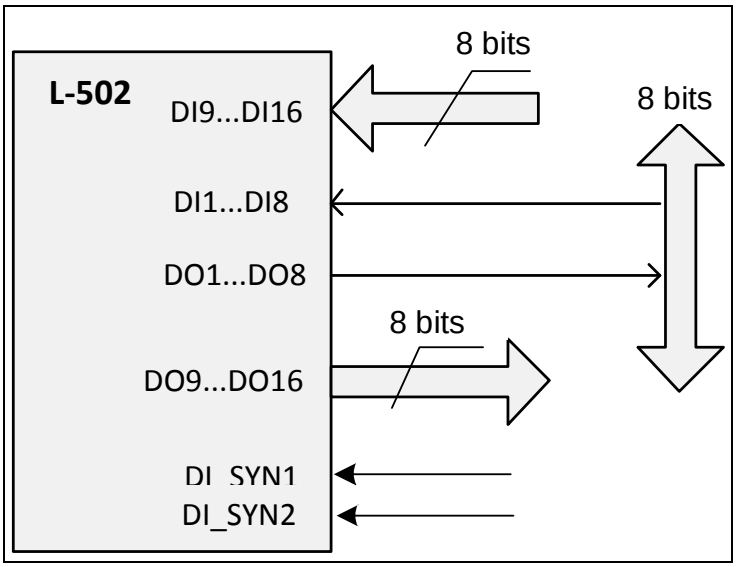


Fig. 4-3: Example of a grouped connection of digital lines: three buses of 8 bits each.

With the addition of two additional universal inputs DI_SYN1, DI_SYN2, we get an almost important case of implementing interfaces with different devices that have an 8-bit bidirectional data bus, input and output control lines.

4.2.4. Internal connector of intermodule synchronization.

The pinout for the synchronization connector for all versions of L-502 is identical, but in version 3, an angled connector is used.

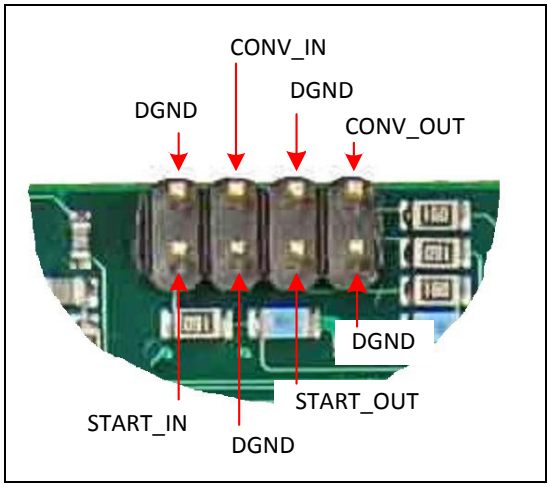


Fig. 4-4: Intermodule synchronization connector (L-502 version 1 and 2).

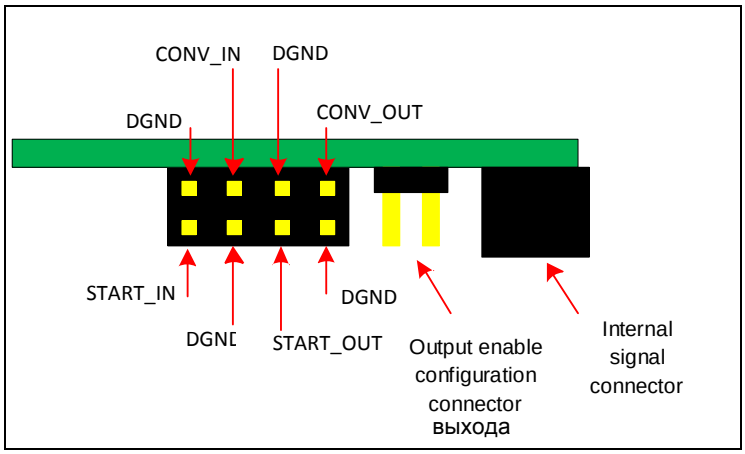


Fig. 4-5: Intermodule synchronization connector (L-502 version 3).

Table 4-3: Intermodule synchronization connector

Signal name	Common point	Direc-tion	State after connection	Description
CONV_IN	DGND	Input	Input	The input of the synchronization pulse of the ADC-DAC conversion and input-output (from the neighboring module L-502)
START_IN	DGND	Input	Input	Input of start signal of ADC-DAC and input-output (from neighboring module L-502). Active logical signal level is high.
CONV_OUT	DGND	Output	Output	Output of conversion signal of ADC-DAC and input-output (to neighboring module L-502).
START_OUT	DGND	Output	Output	Output of start signal of ADC-DAC and input-output (to neighboring module L-502). Active logical signal level is high.
DGND	-	-	-	Common wire circuit for sync connector

All digital signals on the synchronization connector correspond to the LVCMOS voltage level standard for + 3.3V supply voltage. The internal resistance of the inputs START_IN, CONV_IN is 300 Ω. The internal resistance of the outputs CONV_OUT and START_OUT is 50 Ω.

For the maximum permissible voltages and currents at the contacts of the connectors, see the section 4.3, on p. 42

4.2.4.1. Connections with intermodule synchronization.

These connections are designed for short connections of L-502 modules located in adjacent PCIe-slots with two twisted pairs.

The connection of modules located on different computers is not supported.

With the connection shown in the figure below, module # 1 is the master, and the others are slaves. The software of such a system should ensure the start of data collection of the master module after the slave starts and pre-programmed these modules to the appropriate synchronization modes.

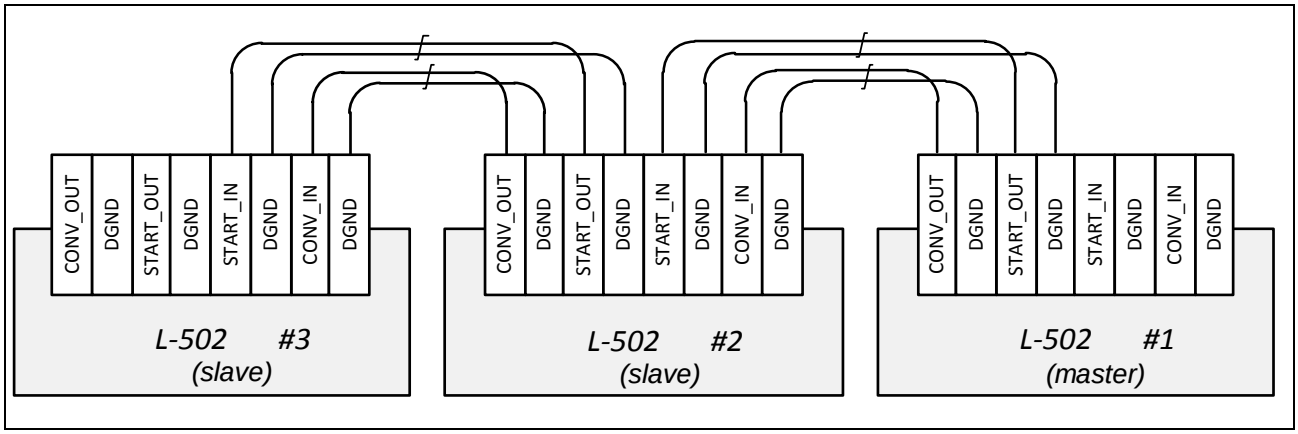


Fig. 4-6: Multi-module synchronization scheme

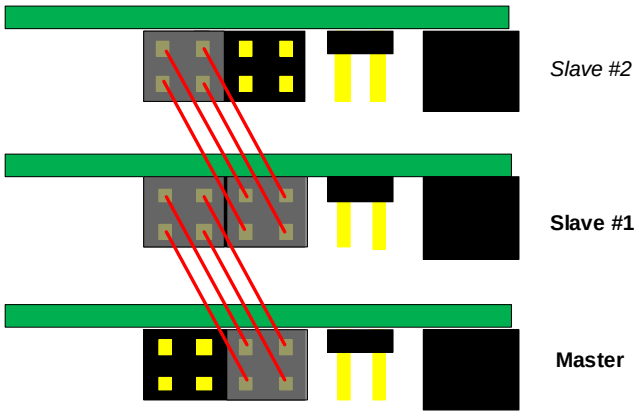


Fig. 4-7: The scheme of multi-module synchronization of three L-502 version 3 (top view of the computer's motherboard)

The synchronization cable for a pair of L-502 modules, which, if necessary, must be ordered separately, is designed to connect two L-502 modules. For connecting N pcs. of L-502 modules on one motherboard you will need (N-1) pcs. of synchronization cables.

If, at least, one L-502 in this connection scheme does not have galvanic isolation, then the entire system of these modules loses the galvanic isolation of the signal circuits from the ground and the computer case.

The four-wire synchronization cable L-502-SYNC connects one pair of L-502 modules. The pinout of the cable is made according to the "one-to-one" scheme. For orientation during installation, use the key ▽ on the casing of the cable connector. At the same time, on each side of the cable, when installed according to the scheme fig. 4-7, the key must be oriented in the same direction.

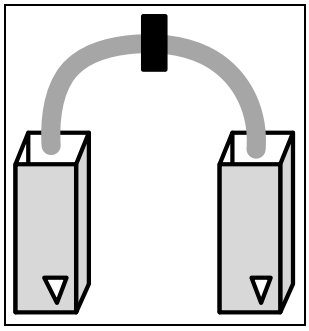


Fig. 4-8: Intermodule synchronization cable L-502-SYNC

The L-502-SYNC cable is clad with a black ferrite ring that improves electromagnetic compatibility. The length of the cable L-502-SYNC is designed for connection L-502, located only in adjacent PCI-Express slots.

If you intend to use the L-502-SYNC cable together with the old versions of 1 or 2 L-502 modules, then the cable connector housing should be shortened (this modification will be made by the L-Card at your request).

4.2.5. JTAG connector.

To debug your own Blackfin software on the L-502 board, you should use one of the JTAG-emulators from Analog Devices: ADZS-USB-ICE, ADZS-HPUSB-ICE or ADZS-ICE-100B with the USB-interface. They differ significantly with USB transfer rate and price. You can get information on these devices on the manufacturer's website www.analog.com .

The board has a JTAG connector, fig. 4-9, compatible with the above JTAG- emulators.

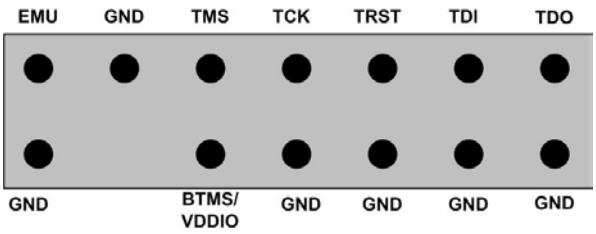


Fig. 4-9. JTAG

The operation of attaching and detaching the JTAG-emulator connector should be done in the de-energized state of both devices.

! If the JTAG emulator and L-502 are to be used in different computers, then the computer grounding circuits (enclosures) must be pre-connected!

Do not connect the JTAG connector to other devices which are not specified in this chapter.

4.3. The maximum allowable conditions at the inputs and outputs of signal lines.

Under the maximum permissible conditions are meant such currents and voltages that do not lead to failure or irreversible degradation of the characteristics of the L-502. At the same time, the maximum permissible conditions may not provide the performance characteristics of the product.

! Long-term operation of equipment at maximum permissible levels is not allowed

Table 4-4 The maximum permissible modes are described for the L-502 module installed in the computer's system unit

Circuit/ Signal	**Maximum permissible modes description**
Inputs X1÷X16, Y1÷Y16, GND32	±15 V relative to AGND
Outputs DAC1, DAC2	± 20 mA when the total load power is not exceeded, see section 4.6
Outputs +15 V, -15 V	No more than 30 mA in load circuits when the total load power is not exceeded, see section 4.6 SC is not permitted.
Inputs DI_SYN1, DI_SYN2	± 10 V relative to the DGND circuit with an internal input resistance of, at least, 1 kΩ.
Digital inputs DI1÷ DI16	From -0.4 to +6.5 V relative to the DGND circuit
DO digital outputs	From -0.4 to +3.6 V relative to the DGND circuit, the current is not more than ± 20 mA. When the power is on, the total load power should not exceed the calculated value, according to section 4.6.
Inputs CONV_IN, START_IN	From -0.5 to +4.3 V relative to the DGND circuit

Table 4-5Maximum permissible through current by GND, AGND, DGND

Maximum permissible through-current by the circuits of one L-502 module: AGND-DGND[6] GND-DGND (L-502 without galvanic isolation) GND-AGND (L-502 without galvanic isolation)	 100 mA 100 mA 100 mA
Maximum permissible through currents along AGND-AGND, AGND-DGND, DGND-DGND circuits of different L-502 modules connected by a synchronization cable	50 mA
Test voltage of galvanic isolation	500 V, 50 Hz during a minute

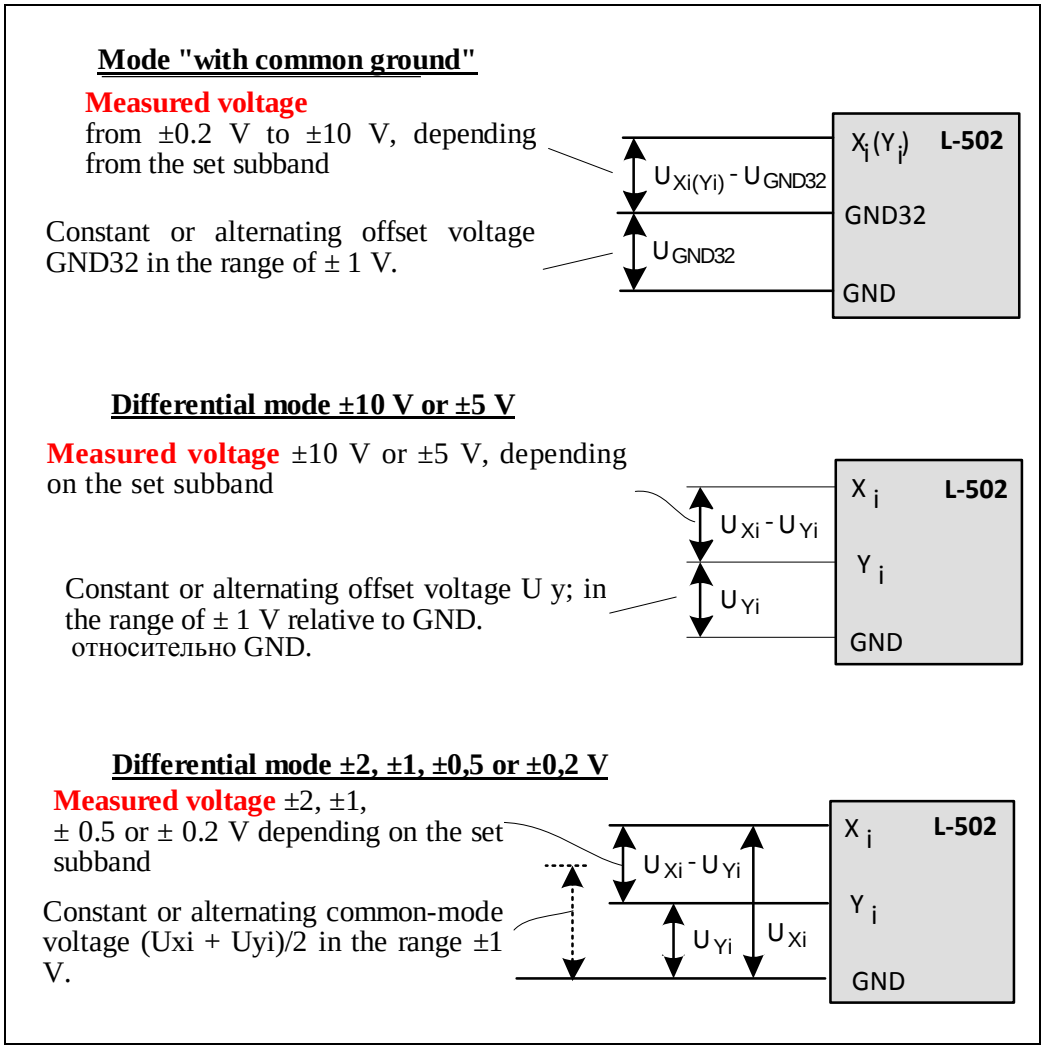
[6] The notion of circuits GND, AGND, DGND is introduced in section 4.1

The maximum permissible voltage rise rate between galvanically isolated circuits in L-502-▒-G-▒	10 kV / μs

The maximum permissible circuit modes of the JTAG connector are not considered, since the JTAG designated area is strictly limited to specific types of JTAG emulators and the specified connection procedure, according to section 4.2.5, p. 41.

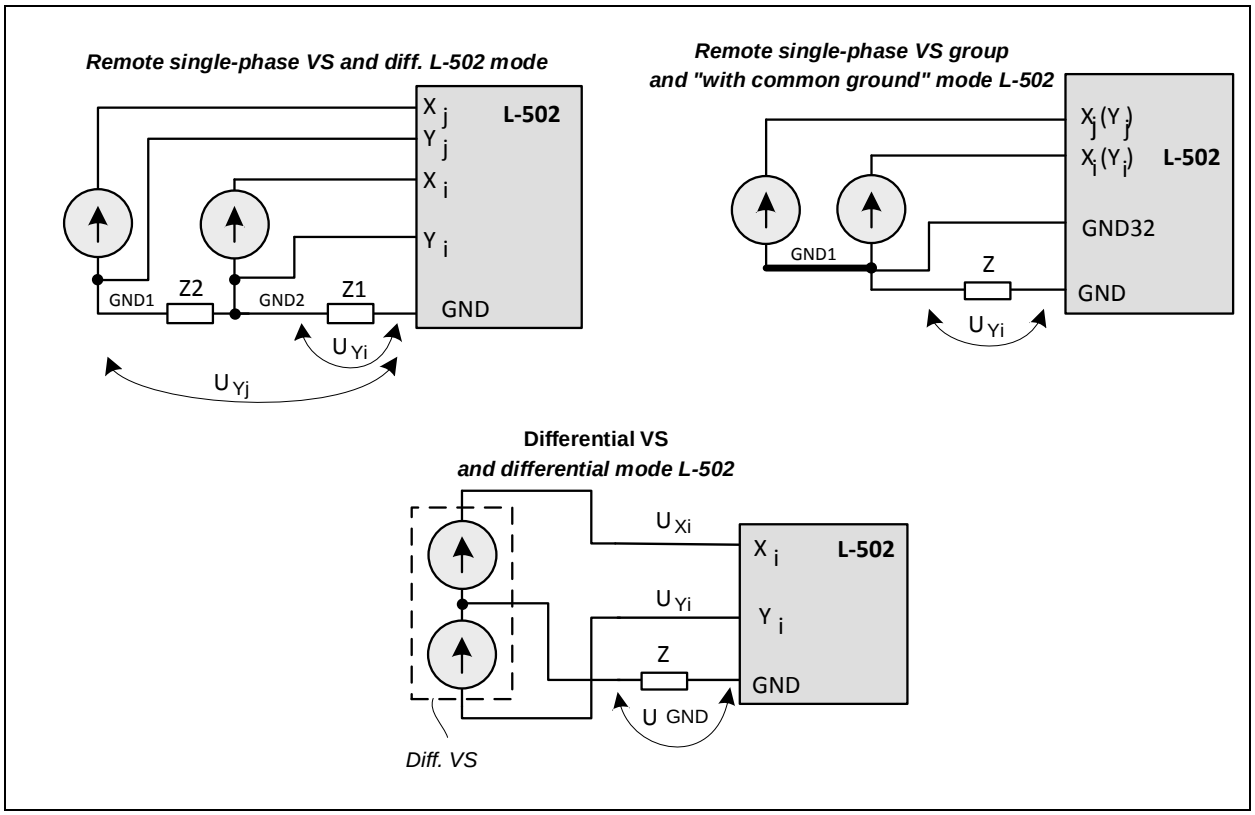
4.4. ADC input operation voltage range

Note that in the differential mode on the subbands ± 10, ± 5 V, the L-502 has unbalanced input signal ranges of the inputs X and Y with regard to the analog ground circuit AGND, and in the "common ground" mode, the L-502 on the same subbands has asymmetric input signal ranges of the inputs X (Y) and GND32 with regard to the AGND circuit.



The figure below shows examples of connecting voltage sources (VS) to the ADC inputs.

Z, Z1, Z2 - the intrinsic resistances of the wires (through which the through currents can flow with the connection of different devices) or other external electrical causes inducing the parasitic offset voltage U_{Yi}, U_{Yj}.U_{GND} are indicated. In the first two circuits, the voltage U_{Yi}, U_{Yj} should not exceed ± 1 V in order to ensure the operating mode, and in the latter scheme the common mode voltage $(U_{Xi} + U_{Yi})/2$ must be within ± 1 V.



Examples of connecting the ADC input are collected in the item 6.1 on page 59.

4.5. Necessary conditions for correct connection and correct settings of the input of the ADC L-502.

Simplified examples of connection of the ADC input are given in section 6.1, however,

! ... If you do not take into account the electrical properties of the signal sources, wires (cables) when using L-502 ADC connections, use the default L-502 program settings, then, most likely, you will get a poor result. Why? What do you need to consider? – If you answer below these questions, links to the Internet resources of the site en.lcard.ru will be used.

4.5.1. The physical causes of possible problems

Physical cause #1. The wide bandwidth of the ADC transmission in L-502 (of the order of 10 MHz) can be not only a great advantage of the L-502 ADC (in the ability of the ADC to qualitatively digitize the high-speed dynamic processes), but it can be a big problem if:

- the signal source has an unlimitedly wide frequency band (much wider than the width of the frequencies of the useful signal)
- unscreened connection is applied (or the signal source itself has a significant area of the unscreened surface), in a situation where electromagnetic fields in the frequency

band up to 10 MHz are always present in the real situation, and also in the situation of the user's failure to apply a differential connection (and adjustment to the differential mode), and therefore use the valuable property of a differential input – effectively suppressing common-mode interference.

Physical cause #2. The high frequency of the 2 MHz channel switch (when tuned to multichannel mode) with L-502 default settings may not only be a great advantage of the L-502 ADC (in the high-speed ADC input interrogation), but it can also be a problem as it takes a short setting time for the measuring circuit (less than 500 ns after the switch's own charge is injected into the measurement circuit). This cause is fundamental for all ADC with input commutator, manifested as a switching disturbance.

4.5.2. Conditions for correct connection and settings L-502.

1. If you need to use no more than 16 ADC channels, always select the differential connection mode and the L-502 settings.
2. With a differential connection, the X and Y circuits of each channel always lead in pairs (twisted pair, shielded pair).
3. The L-502 signal circuit must be shielded. On the screen connection, see 4.2.2.
4. For differential connection, when using a pair cable, to maximize common-mode rejection of the L-502, the output impedances from the remote source along the X and Y circuits should be balanced, (connection example - p. 6.1.10).
5. The AGND L-502 circuit must be connected to the common circuit of the signal source (if there are several signal sources to the common junction of the common signal source wires).
6. If you need to configure the L-502 for multichannel operation, you first need to optimize the signal-to-noise ratio of the ADC in a single-channel operation mode with a maximum data acquisition frequency of 2 MHz, in which in the signal spectrum you will see all the frequencies of the interference (possibly from "mirror frequencies", if interference above 1 MHz), which means that you have a tool in your hands to find the sources and causes of these interferences (before going to multi-channel mode and averaging mode, which will be much more difficult to understand with sources of interference).
7. **When using ("default") in the multi-channel operation mode of the maximum switching frequency (2 MHz), the output impedance** of the L-502 ***signal circuit*** **must be from 0 to 50 Ω (in the frequency band up to 10 MHz), and this voltage source must be linked to connector L-502 by wires of zero length.** This is achieved either by directly connecting the output of the signal source itself (50 Ω) or by connecting its load resistor (up to 50 Ω) directly to the cable part of the L-502 signal connector (when connecting an agreed 50-ohm line or a current shunt to 50 ohms of the external current measurement circuit) .
8. **When using a multichannel mode of non-zero length of wires to *the voltage source and (or) with an output resistance of the signal circuit of more than 50 ohms, the program setting of the signal conditioning time* n_{su} > 1 (s. 3.3.6) should be applied.**

9. **In multi-channel mode, the optimal settling time n_{su} (s. 3.3.6) should be selected depending on the output impedance of the signal source, the length and the coherence of the cable.**It is suggested to choose the optimal n_{su} for this channel by the criterion of obtaining a small inter-channel signal transmission from the previous polling channel.
10. **To improve the signal-to-noise ratio and increase the resolution in the measurement path, it is recommended to use the maximum possible averaging factor n_{av}> 1 (s. 3.3.6)** for the required channel polling frequency and the necessary *signal conditioning time* n_{su} .
11. Do not exceed the operating voltage ranges at the inputs X, Y, GND32 (s. 4.4)
12. Use the L-502 "common ground" operation mode only in case of closely located low-resistance sources. Optimizing the n_{su} **and** n_{av} settings for the "common ground" mode is required. Do not make "common ground" connections through the cable, if there are no low-resistance pull-up resistors on the L-502 side.
13. While connecting L-502 "with common ground", the GND32 circuit must be in the same group of cable wires (in particular, within the same screen) as other circuits X and Y operating in the "common ground" scheme.
14. While using 16 to 31 channels, it is advisable to combine L-502 "differential" and "common ground" connections and settings to obtain more channels operating in differential mode. In this case, the wires X and Y (differential circuit) and the wires X, Y, GND32 ("common ground" circuits) should form different groups in the cable in a common AGND circuit situation for these groups.
15. When using L-502 without galvanic isolation, do not allow continuous currents on the screens and common wires of the signal circuits. Do not allow continuous currents between common-wire circuits of digital and analog signal circuits. Take into account the internal scheme of land connection in L-502 (s. 4.1)

4.6. Calculation of the total load power of L-502 output circuits

If you intend to use L-502 output circuits to connect any external loads, then the total load power should not exceed the power specified in the specification (see section 5.7 on p. 56). The load power should be estimated according to the procedure described below.

The total load power P *taken from the L-502 power system is:*

$$P = \sum P_{DO} + \sum P_{DAC} + P_{+15} + P_{-15} + P_{3,3}$$

where P_{DO} *is the total load power taken from digital DO outputs in the "1" state (only for loads connected to the GND circuit);*

P_{DAC} *— power load removed from the DAC outputs;*

P_{+15} *— power load, taken from the output of +15 V;*

P_{-15} *— power load, taken from the output of -15 V;*

$P_{+3,3}$ *— power load, taken from the output of +3.3 V;*

In turn, the power summands P_{DO} *of the corresponding i-th outputs must be calculated either through the known load current* I_{DO}^{i} *by the formula* $P_{DO}^{i} = 3{,}3 * I_{DO}^{i}$*, or through the known load resistance* R_{DO}^{i} *at the i-th output* $P_{DO}^{i} = \frac{10{,}9}{R_{DO}^{i}}$

The power summands P_{DAC} *of the corresponding j-th outputs must be calculated either through the known load current* I_{DAC}^{j} *by the formula* $P_{DO}^{j} = 5{,}0 * I_{DAC}^{j}$*, or through the known load resistance* R_{DAC}^{j} *at the j-th output* $P_{DAC}^{j} = \frac{25}{R_{DO}^{j}}$

The power P_{+15} *and* P_{-15} *should also be calculated either through known load currents* $I_{+15} + I_{-15}$ *by formulas* $P_{+15} = 5{,}0 * I_{+15}$, $P_{-15} = 5{,}0 * I_{-15}$ *or through a known load resistance* R_{+15}*, according to* R_{-15} *formulas* $P_{+15} = \frac{25}{R_{+15}}$, $P_{-15} = \frac{25}{R_{-15}}$

All terms in the power formulas are positive, dimension: power — Watt, current — Ampere, resistance — Ohm

Chapter 5. Specifications.

The following specifications indicate the main parameters of the L-502 for its intended - operating mode.

For the maximum permissible voltages and currents at the contacts of the connectors, see section 4.3, on p. 42

5.1. ADC.

Parameter	Value
Number of channels	16 differential or 32 with common ground (single-phase)
DC Voltage Measurement Range Voltage measurement subranges (the input signal is applied between Xi and Yi for 16-channel mode, between Xi (Yi) and GND32 for 32-channel mode)	±10 V ±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V, ±0.2 V when *observing the operating conditions of the measurement (see below)*
Operating conditions of measurement at the ADC inputs (s. 4.4, p. 44)*:* - Voltages at the input Yi with regard to AGND for the differential measurement mode on the subbands "± 10 V", "± 5 V" - The average value of the voltage at the inputs X and Y for the differential mode on the measurement subranges "± 2 V", "± 1 V", "± 0.5 V", "± 0.2 V" - Voltages at the GND32 input relative to AGND for the "common ground" mode and all measurement subbands	$\lvert U_X \rvert \leq \pm 1$ V $\lvert (U_X + U_Y)/2 \rvert \leq \pm 1$ V $\lvert U_{GND32} \rvert \leq \pm 1$ V
Analog-to-digital converter bit depth	16 bits
ADC data width after arithmetic processing (data correction, data averaging)	24 bits
Limits of the permissible reduced basic error of DC voltage measurements, %, in subbands: – 10; 5 and 2 V – 1 V – 0.5 V – 0.2 V	 ±0.05 ±0.07 ±0.1 ±0.2
Own input current (via X, Y or GND32 circuits) in single-channel mode, no more than	0.4 µA
Charge injection into the input circuit of the ADC (X, Y or GND32) for one switching	2 pC
Possibility of data correction (use of calibration coefficients)	Yes

Common-mode rejection ratio 50 Hz with 1 V amplitude in differential mode on sub-band:	
±10 V	77 dB
±5 V	83 dB
±2 V	90 dB
±1 V	92 dB
±0.5 V	92 dB
±0.2 V	92 dB
Resistance to overloads by input measuring signal of DC voltage	±15 V
Limits of the permissible relative fundamental error of the ADC conversion frequency	±0.005 %
AC voltage measurement range	From 0.2 mV to 7 V
Limits of the permissible relative basic error of measuring the AC voltage	According to section

5.1.1. Limits of the permissible relative basic error of measuring the AC voltage

Frequency range of input signal, kHz	**Limits of the permissible relative basic error of measuring the AC voltage, %**
from 0.01 to 50 incl.	$\pm[0{,}15 + 0{,}02 \times (\frac{X_{AC}}{X} - 1)]$
more than 50 to 100 incl.	$\pm[0{,}3 + 0{,}02 \times (\frac{X_{AC}}{X} - 1)]$
more than 100 to 300 incl.	$\pm[1 + 0{,}03 \times (\frac{X_{AC}}{X} - 1)]$
more than 300 to 999	$\pm[5 + 0{,}05 \times (\frac{X_{AC}}{X} - 1)]$

Notes:
1 The error in measuring the AC voltage is normalized in the differential connection scheme E-502 at the ADC conversion frequency of 2000 kHz, for signals whose peak values do not exceed the value of the set measurement subband.
2 X_{AC} is the AC voltage measurement limit, $\boxed{X_{AC} = \frac{X_K}{\sqrt{2}}}$ where X_K is the value of the set voltage subband.
3 X_K is the final value of the set voltage subband.
4 X is the value of the measured voltage.

5.1.2. ADC own input noise.

Below are the typical noise levels without taking into account the factors of temperature and long-term zero drift for 1-channel mode with a shorted ADC input.

Data entry rate, Kword/s from one ADC channel	**Averaging factor**	**ADC subrange, V**					
		±10	±5	±2	±1	±0.5	±0.2
		Typical value of the noise level, applied to the ADC input, µV					
2000	1	309	157	50	37	22	18
400	5	127	56	28	16	12	8
50	20	62	27	13	8	6	4
10	128	40	25	12	7	5	4

5.1.3. ADC inter-channel passing.

Signal source resistance (in the channel where the interchannel passage is measured)	**Channel polling time,** µs (with averaging factor equal to 1**) or channel setup time, µs**					
	0.5	1.0	2.0	4.0	8.0	16.0
	Interchannel traversal, dB (the signal from the previous channel in the order of interrogation)					
0-50 Ohm	**-65**	**-78**	**-82**	**-82**	**-82**	**-82**
1 kOhm	-35	-63	-73	-82	-82	-82
10 kOhm	-5	-11	-22	-43	-74	-82

5.2. DAC.

Parameter	Value
Number of channels	2
Output frequency in synchronous mode	1 Mcount/s per channel
Output frequency in asynchronous mode	The actual speed depends on many factors of the software and hardware environment.
DAC bit depth, bit	16
Output modes	Synchronous (streaming), asynchronous
Output signal range	±5 V
Operating range of output currents	±10 mA
Limits of the allowed reduced basic error of reproducing DC voltage	±0,3 %
Maximum allowable output current[1]	±20 mA
AC voltage playback range	From 1 mV to 3.5 V
AC voltage playback error	According to section 5.2.1

5.2.1. AC voltage playback error

Output voltage frequency, KHz	Limits of the permissible relative basic error of AC playback voltage, %
From 0.01 to 50 inclusive	$\pm[0{,}15 + 0{,}02 \times (\frac{X_{AC}}{X} - 1)]$
From 50 to 100 inclusive	$\pm[0{,}5 + 0{,}02 \times (\frac{X_{AC}}{X} - 1)]$
Notes: 1 X_{AC} – the final value of the range of AC voltage playback, X_{AC} = 3.5 V. 2 X is the value of the voltage to be reproduced.	

[1] If the total load power is not exceeded, see s. 4.6 Calculation of the total load power of L-502 output circuits

5.3. Digital inputs.

Parameter, characteristics	Value, description
Total number of digital inputs (DI1-DI16, DI_SYN1, DI_SYN2) Of these, the number of digital inputs with synchronization function (DI_SYN1, DI_SYN2)	18 2
Data entry modes	Synchronous, asynchronous
Program control of pull-up resistors activation: - for inputs DI1-DI16 - for inputs DI_SYN1, DI_SYN2	 Regardless of the high and low byte Regardless of each input
Maximum speed in synchronous mode	2 Mwords/s
Maximum speed in asynchronous mode.	The actual speed depends on many factors of the software and hardware environment.
Maximum permissible input voltage range: - at the inputs DI1-DI16 - at the inputs DI_SYN1, DI_SYN2	 –0.5…+6.5 V –10…+10 V
Recommended operating voltage range	0 …+5.5 V
Operating voltage range	-0.2...+0.6 V ("logical zero") +2.4...+5.0 V ("logical item").
High-impedance state with power off	Yes
Maximum input current with power off	10 µA
Own input current in operating mode with software-activated pull-up resistors	10 µA
Pull-up resistor resistance	2.2 kOhm with regard to +3.3 V
Recommended edge duration: - at the input DI1-DI16 - DI_SYN1, DI_SYN2	 0…50 ns Not limited
The input hysteresis voltage DI_SYN1, DI_SYN2, typical value	400 mV

5.4. Digital outputs.

Parameter	Value
Number of digital outputs of general purpose	16
Control of the third state of outputs	Byte
Data entry modes	Synchronous, asynchronous
Maximum speed in synchronous mode	1 KWords/s
Maximum speed in asynchronous mode	the actual speed depends on many factors of the software and hardware environment.
Maximum permissible current[2] in the load circuit	20 mA
Recommended current in the load circuit	max. 8 mA
Voltage range at digital outputs	0...+0.4 V ("logical zero") max. 2.4 V ("logical unit"). Output logic elements with a supply voltage of 3.3 V
Output resistance, typical value	110 Ohm
Maximum leakage current in operating mode in high-impedance state	±1 µA
High-impedance state with power off	No

5.5. Synchronization in L-502.

5.5.1. Synchronization characteristics

Parameter	Value
The reference frequency of the process of synchronization of data collection and output of ADC, DAC, digital input and output: • For a single module • For a multiple module synchronization	1.5/2.0 MHz 1.5/2.0 MHz 1,5 MHz
Limits of the permissible relative fundamental error of the reference frequency	±0.005

[2] If the total load power is not exceeded, see s. 4.6 Calculation of the total load power of L-502 output circuits

5.5.2. Intermodule synchronization interface

Parameter	Value
Topology of multimodule connections over synchronization lines	Sequence
Maximum number of synchronized L-502 modules in a serial synchronization scheme	Equal to the number of PCI-E slots in the PC motherboard
Maximum cable length of the intermodule synchronization	40 mm (only for an adjacent module PCI-E)
Number of intermodule synchronization lines	4 twisted pairs (2 inputs from the master and 2 outputs to the slave)

5.6. Characteristics of standard interfaces.

Parameter, characteristics	Value, description
Interface with a computer	
Standard for an interface with a computer	PCIe x1
The bit depth of the L-502 data word on the PCIe	32 bits
DMA support in the BUS MASTER mode on the PCle	Yes
Interfaces of the signal processor ADSP-BF523 (L-502-P)	
Interface with a computer	HOST DMA 16 bits
Main interface of input-output for ADC, DAC, digital I/O	SPORT0, >120 Mbit/s, duplex
Main control interface	SPI
SDRAM interface	32 MB; 16 bit; 132.5 MHz
Debugging interface	JTAG
Compatibility with JTAG emulators Analog Devices	ADZS-ICE-100B, ADZS-USB-ICE, ADZS-HPUSB-ICE.

5.7. Power supply system and galvanic isolation.

Parameter, characteristics	Value, description
L-502 modifications, which have galvanic isolation	L-502-P-G, L-502-P-G-D, L-502-X-G, L-502-X-G-D
The condition of galvanic isolation in a system of several L-502 connected via a synchronization interface	If in all connected L-502 there is galvanic isolation
Galvanic isolation border	Between all circuits that come to the contacts of signal connectors, and PC circuits. The metal case DRB-37M is not galvanically isolated from the PC.
Galvanic isolation border in a system of several L-502 connected via a synchronization interface	Between all circuits that come to the contacts of all signal connectors L-502, and PC circuits. The metal housings DRB-37M are not galvanically isolated from the PC. Between themselves all the signal circuits in the system will not be galvanically isolated
Test voltage of galvanic isolation	500 V during 1 min.
The maximum permissible voltage rise rate between galvanically isolated circuits in L-502-▒-G-▒	10 kV / µs
Total load power taken from all outputs L-502: For L-502-▒-▒-D (with DAC) For L-502-▒-▒ (without DAC)	The method for estimating the load power is given in p. 4.6, p. 48 0.4 W 0.8 W
External analog power supply outputs	+15 V, -15V. The maximum load current is up to 30 mA, provided that the total load power is not exceeded. SC is prohibited. Outputs are switched on by jumpers, (see p. 2.1.2), this possibility is dependent on whether the corresponding outputs of the DAC are used
External digital circuits supply output	+3.3 V. The operating current of the load is up to 50 mA permanently, up to 100 mA for a short time. Attention! In versions 1 and 2 of L-502 products (serial numbers start with the digit "1" or "2", short circuit of the output + 3.3 V is not allowed (leads to failure of L-502)! In version 3, short circuit of the output is permissible.
Maximum current consumed from PCI Express unit through circuits: “+12 V” “+3.3 V” “+3.3 VAUX”	 0.4 A 0.35 A for L-502-X-▒-▒ 0.85 A for L-502-P-▒-▒ 0.02 A

Maximum power consumed from PCI Express unit	6 W (for L-502-X-▒-▒) 7.6 W (for L-502-P-▒-▒)
Maximum permissible through-current by the circuits of one L-502 module: AGND-DGND[3] GND-DGND (L-502 without galvanic isolation) GND-AGND (L-502 without galvanic isolation)	 100 mA 100 mA 100 mA
Maximum permissible through currents along AGND-AGND, AGND-DGND, DGND-DGND circuits of different L-502 modules connected by a synchronization cable	50 mA

[3] The notion of circuits GND, AGND, DGND is introduced in section 4.1

5.8. Construction specification.

Parameter	Value
Construct	PCI Express CARD x1 of standard height, with bracket, in length - less than half the size (HALF LENGTH), according to *PCI Express Card Electromechanical Specification rev.2.0*. Requires one PCI Express crate slot.
Overall dimensions of the printed circuit board - length x height	136 x 101 mm

5.9. Environmental conditions.

5.9.1. Normal conditions

Parameter	Value
Normal operating conditions: – environment temperature, °C – relative humidity, % – air-pressure, kPa	 20±5 from 30 to 80 from 84 to 106

5.9.2. Operating conditions

Parameter	Value
For stability under climatic influences, the converters, in addition to the versions with the letter index I, correspond to GOST 22261, group 3 with an extended range of operating temperatures: – environment temperature, °C – relative humidity at an ambient temperature of 25 °C, % – air-pressure, kPa	 from +5 to +55 up to 90 from 70 to 106.7
For stability under climatic influences, converters of designs with the letter index I correspond to GOST 22261, group 4 with an extended range of operating temperatures: – environment temperature, °C – relative humidity at an ambient temperature of 30°C, % – air-pressure, kPa	 from -40 to +60 up to 90 from 60 to 106.7

Chapter 6. Connexion samples.

! These connection examples should be considered together with the recommendations for connecting and configuring the L-502 (n.4.5).

The short form of information provided in this chapter does not cover all the features of the connection for your particular case. If necessary, please contact: en@lcard.ru or in the conference on the site en.lcard.ru

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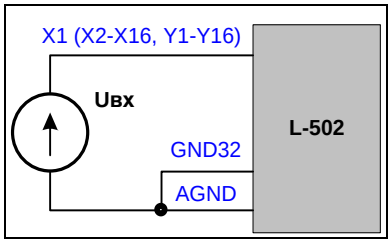
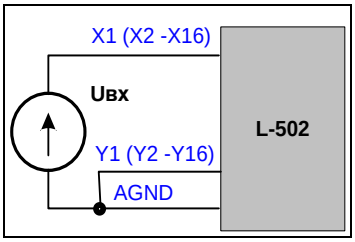
6.1. ADC entry point connection

6.1.1. Connecting to the ADC entry point of single-phase voltage source

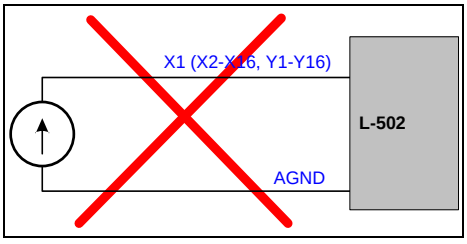
6.1.1.1. Up to 32 channels. Mode "with common ground"

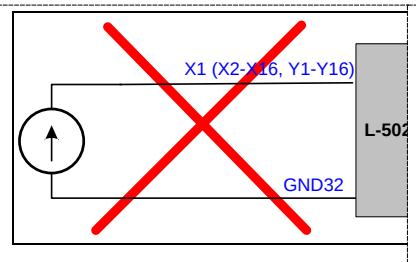


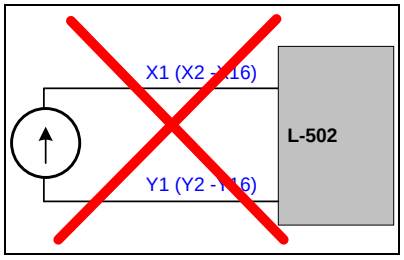
6.1.1.2. Up to 16 channels. "Differential" mode

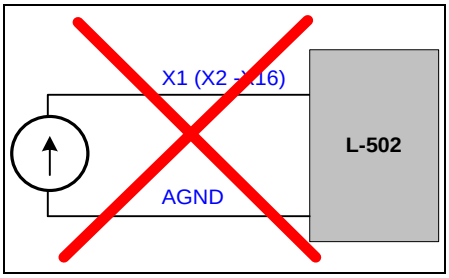


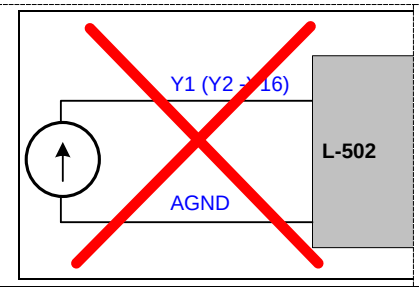
Forbidden to connect in this way!:



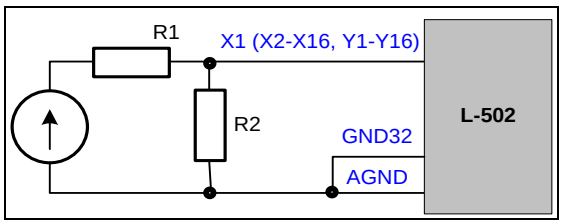




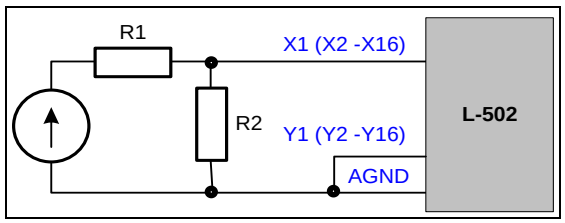




6.1.1.3. Voltage divisor. Mode "with common ground"



6.1.1.4. Voltage divisor. "Differential" mode

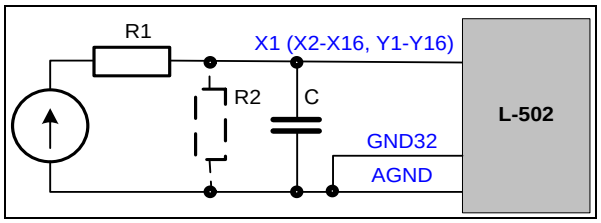


The voltage transfer ratio is R2/(R1+R2).

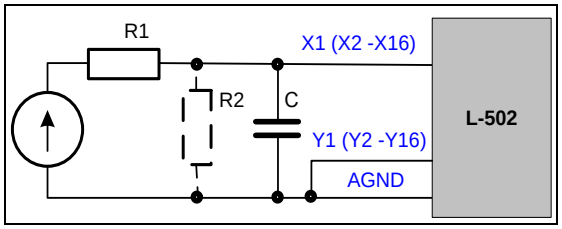
It is necessary that R1 or R2 should not be more than 50 ohms if the switching frequency is maximal.

R2 should be located close to the L-502 entry point.

6.1.1.5. Integrating circuit. Mode "with common ground"



6.1.1.6. Integrating circuit. "Differential" mode



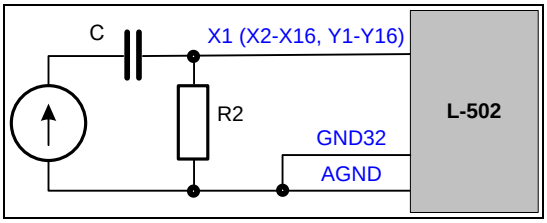
The transmission coefficient of the voltage in the frequency band is R2/(R1+R2).

If multichannel mode, it is necessary that $1/F_{ADC} >> R1*R2*(C+10^{-10})/(R1+R2)$, or if R2 is not present, then $1/F_{ADC} >> R1*(C+10^{-10})/R1$, where F_{ADC} is the ADC conversion frequency.

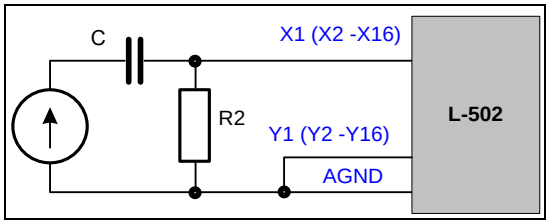
It is necessary that R2 should not be more than 50 ohms if the switching frequency is maximal.

R2, C should be located close to the L-502 entry point.

6.1.1.7. Closed entry. Mode "with common earth"



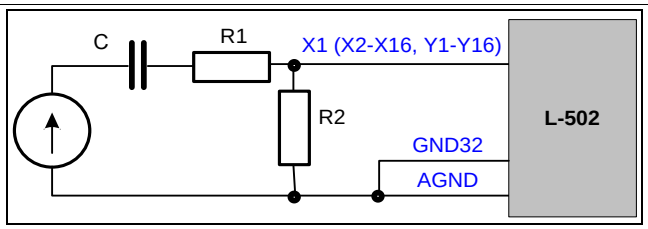
6.1.1.8. Closed entry. Mode "differential"



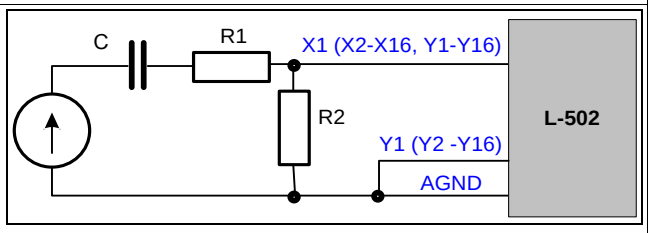
The connection is recommended for single-channel mode.

R should be located close to the L-502 entry.

6.1.1.9. Closed entry with divider. Mode "with common ground"



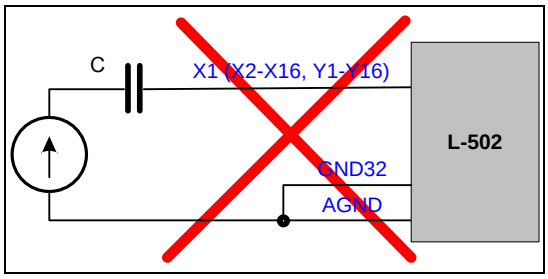
6.1.1.10. Closed entry with divider. "Differential" mode

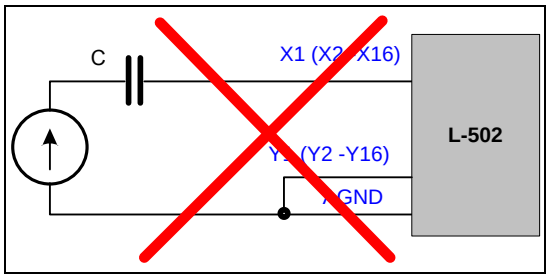


In multi-channel mode, the connection is correct only for R2 << R1 and R2 ≤ 50 Ω.

R2 should be located close to the L-502 entry point.

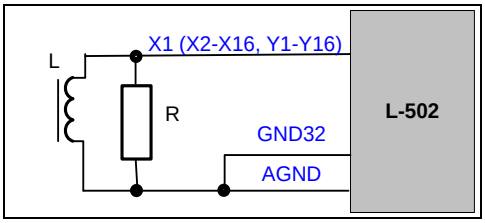
The transmission coefficient of the voltage in the passband is R2/(R1+R2).



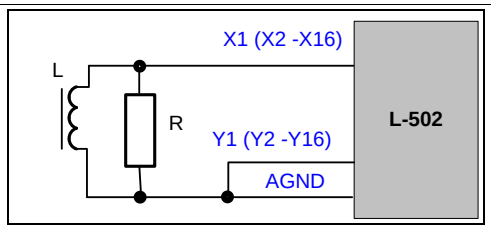


Can not be connected like this!

6.1.1.11. Inductive pickup. Mode "with common ground"



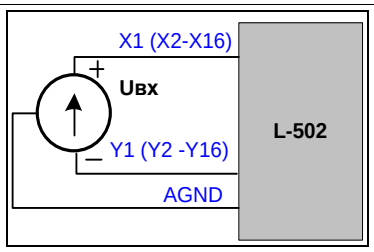
6.1.1.12. Inductive pickup. "Differential" mode



Resistor R performs the function of a damper to suppress the oscillation process in the L-C circuit, where C is the equivalent total capacitance applied in parallel to L. The ADC entry capacitance is estimated to be 25 pF. Resistor R should be located close to L-502 input.

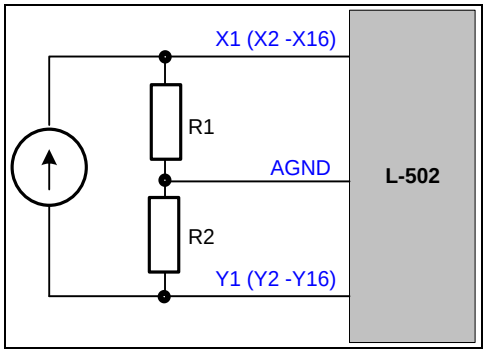
6.1.2. Connection to ADC input with up to 16 differential voltage sources

6.1.2.1. General case



Only for voltage subranges of L-502: ± 2 V, ± 1 V, ± 0.5 V, ± 0.2 V.

6.1.2.2. Differential connection of an isolated voltage source

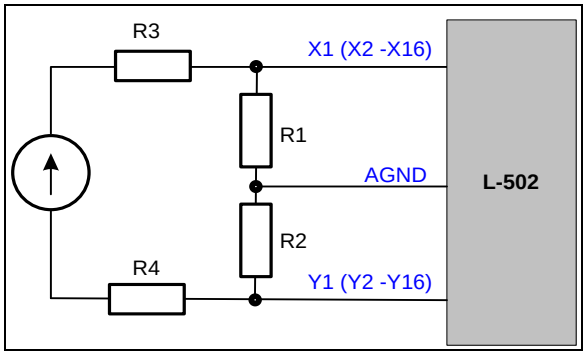


The following condition should be met:
(R1 = R2) ≤ 50 Ω, if the switching frequency is maximal.

Allocate R1, R2 close to L-502 entry.

Only for voltage subbands:
± 2 V, ± 1 V, ± 0.5 V, ± 0.2 V.

6.1.2.3. Differential connection of an isolated voltage source with divider

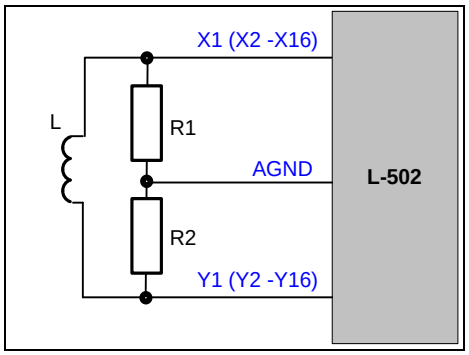


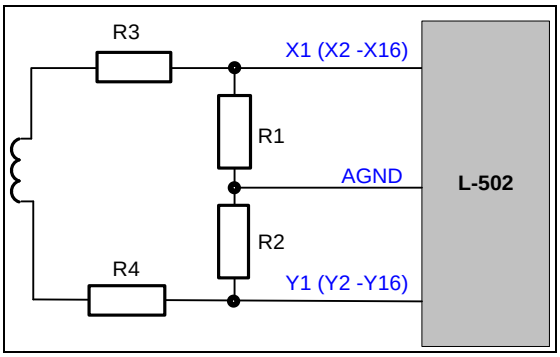
It is necessary: R1 ≤ 50 Ω, if the switching frequency is maximal, R1 = R2, R3 = R4..

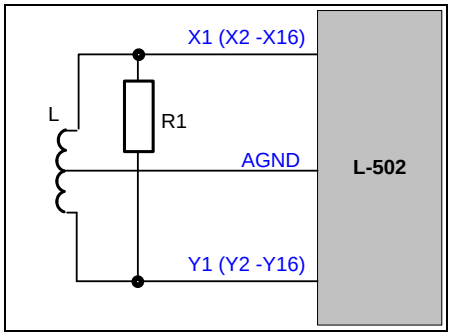
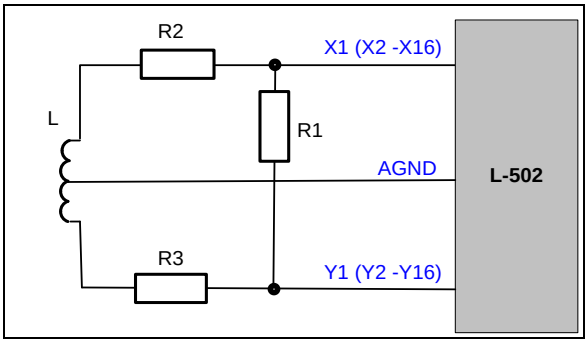
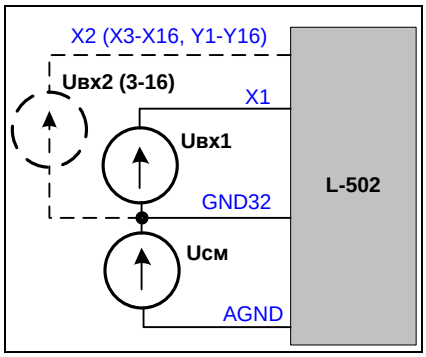
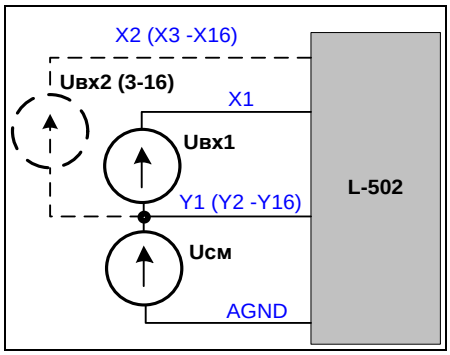
Allocate R1, R2 close to L-502 input. The voltage transfer ratio is (R1+R2)/(R1+R2+R3+R4)

Only for voltage subbands:
±2 V, ±1 V, ±0.5 V, ±0.2 V

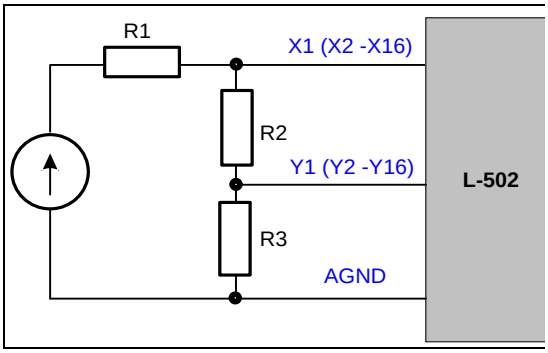
6.1.2.4. Special case: differential connection of the inductive sensor:





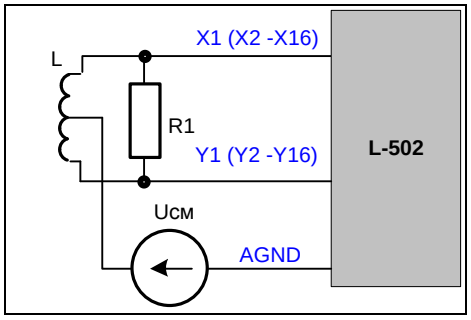
Only for voltage subbands: ±2 V, ±1 V, ±0.5 V, ±0.2 V	*Only for voltage subbands:* ±2 V, ±1 V, ±0.5 V, ±0.2 V
6.1.2.5. Differential winding connection with midpoint	***6.1.2.6. Differential winding connection with midpoint through the divider***
 Locate R1 close to L-502 entry point *Only for voltage subranges of L-502:* ±2 V, ±1 V, ±0.5 V, ±0.2 V	 Locate R1 close to L-502 input. *Only for voltage subranges of L-502:* ±2 V, ±1 V, ±0.5 V, ±0.2 V
6.1.3. Connection to the ADC input for the case where the common wire of the signal sources has a offset potential **Ucm of max. ± 1 V** relative to the AGND circuit.	
6.1.3.1. Connection up to 32 channels. Mode "with common ground"	***6.1.3.2. Connection up to 16 channels. "Differential" mode***
 See limitations in section 4.4, p. 44!	 See limitations in section 4.4, p. 44!

6.1.4. Measurement of the voltage drop on the circuit section in the differential mode (up to 16- channels)



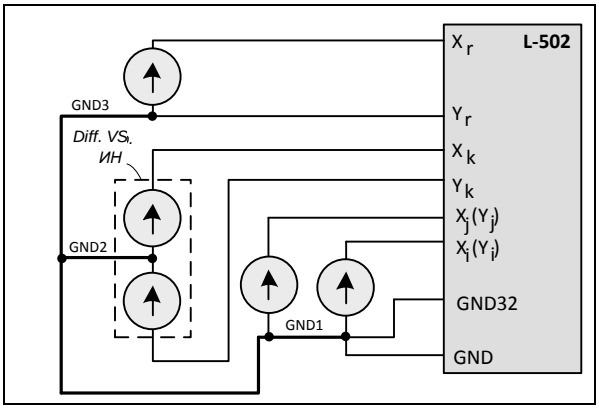
This connection allows you to measure the voltage drop *across resistor R2*. **For a single-channel mode**, R1, R2, R3 can also be impedances of a capacitive or inductive nature, but with the condition that the circuits X and Y used are not broken by the direct current of the circuit. **In multichannel mode**, the equivalent impedance referred to the ADC input must be active. It is necessary that R2 should not be more than 50 ohms if the switching frequency is maximal. See limitations in section 4.4, p. 44!

6.1.5. Differential connection of the transformer (throttle) winding with midpoint and offset potential with respect to AGND



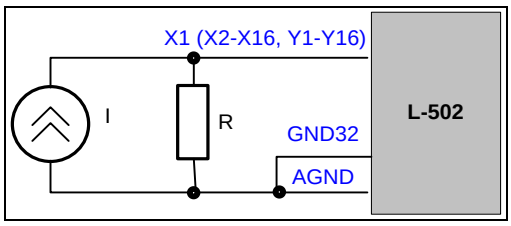
Limitations:
|Ucm| ≤ 1 V
Only for the voltage subbands L-502:
±2 V, ±1 V, ±0.5 V, ±0.2 V

6.1.6. Example of mixed connection of voltage sources "with common ground" and differential.

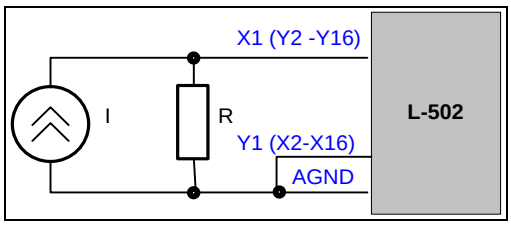


6.1.7. Connecting a power supply to the ADC input

6.1.7.1. Mode "with common ground"

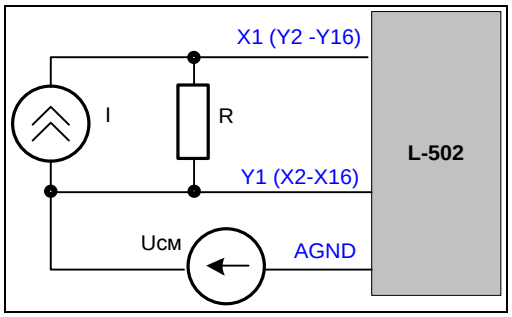


6.1.7.2. Differential mode

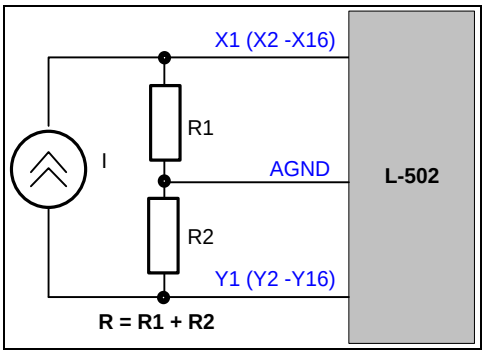


Fixed ADC ± U subband must correspond to $U=I_{MAX}*R$, and the current source must have a voltage margin of at least U. Resistor R should always be located close to the ADC input. In any case, the resistor R must be less than 50 Ω in the multi-channel mode at the maximum switching frequency.

6.1.7.3. Differential mode, offset potential due to current source in regard to AGND



6.1.7.4. Differential mode, isolated current source



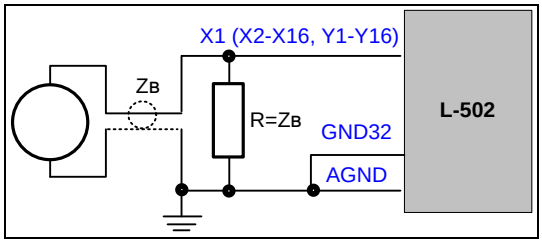
Only for the voltage subbands L-502: ±2 V, ±1 V, ±0.5 V, ±0.2 V

Fixed ADC ± U measurement subband must correspond to $U=I_{MAX}*R$, while the current source must have a voltage margin of, at least, U. Resistor R should always be located close to the ADC input. Resistors R, R1, R2 must be less than 50 Ω in multichannel mode at the maximum switching frequency. **|Ucm| ≤ 1 В**

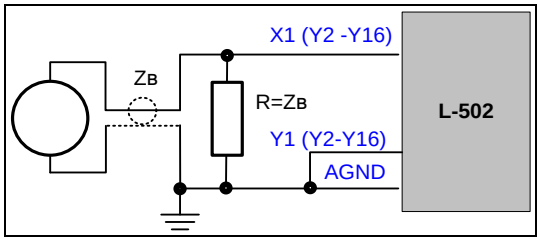
6.1.8. Consistent connection of remote current sources or voltage through a long line with a wave resistance of Zw with load on the side of the receiver.

(If the signal source has an output impedance, unequal to Zw, then these cases correspond to one-way matching of the long line on the side of the signal receiver)

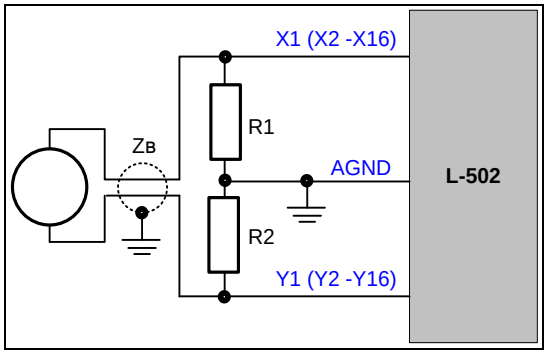
6.1.8.1. Mode "with common ground"



6.1.8.2. Differential mode



6.1.9. Differential connection of an isolated current source or voltage



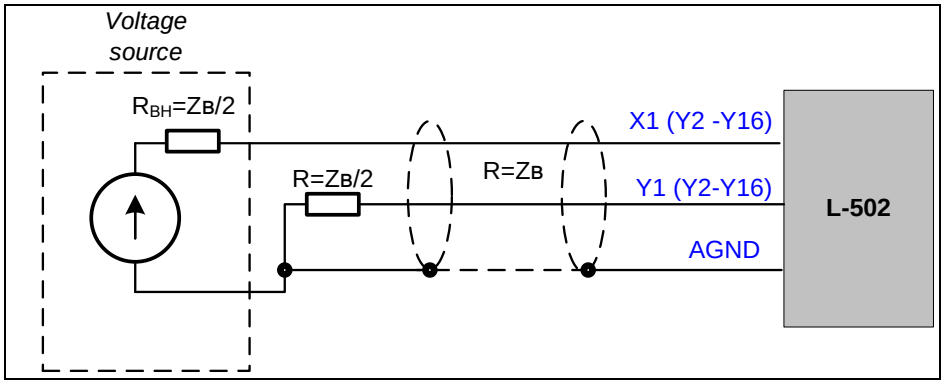
R1=R2

R1+R2 = Zw

The circuit is valid only for the following voltage subranges L-502:

±2 V, ±1 V, ±0.5 V, ±0.2 V

6.1.10. The coordinated connection of a remote voltage source through a pair of long line with a wave resistance Zw with matching on the signal source side

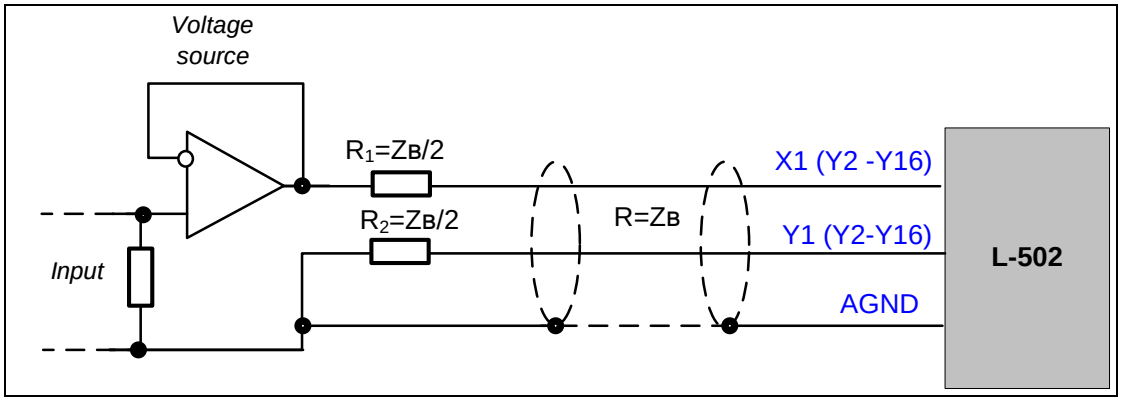


R_{BH} – internal (output) impedance of the signal source.

R – balancing resistor on the signal source side.

The cable must be paired (shielded twisted pairs) with wave resistance of wire pairs Zw.

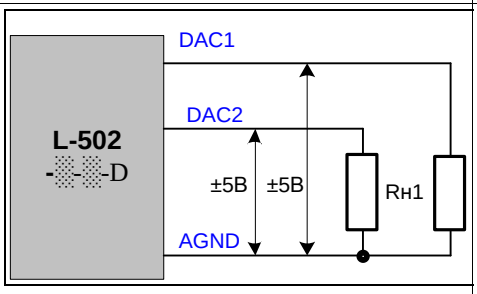
Below is a practical case where a broadband operational amplifier acts as a remote voltage source (providing a low-impedance voltage output in the frequency band up to 10 MHz).



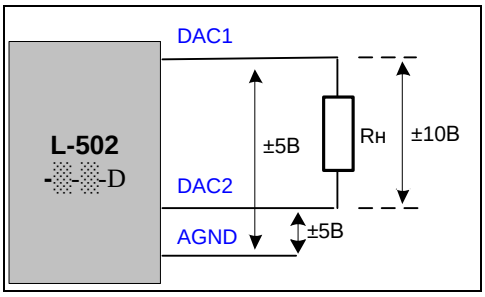
6.2. Connecting the DAC outputs.

To realize the DAC function in L-502-▒-▒-D, the outputs DAC1 and DAC2 must be preconfigured with jumper, see section 2.1.2 on p. 15

6.2.1. 2-channel output ±5 V



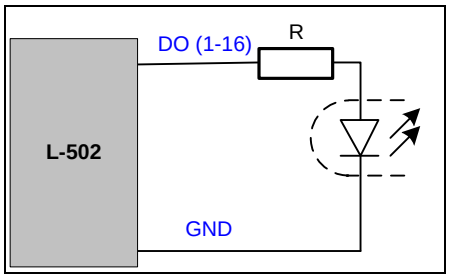
6.2.2. Single-channel differential output ±10 V



The differential output ±10 V is realized as a difference voltage between the outputs DAC1 and DAC2

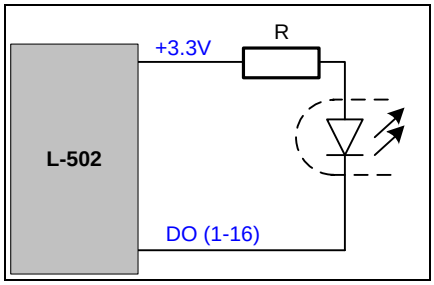
6.3. Connecting the digital inputs and outputs.

6.3.1. Connecting the LED or the optron input. Option 1



The LED is lit when the DO output is at the "logical unit".

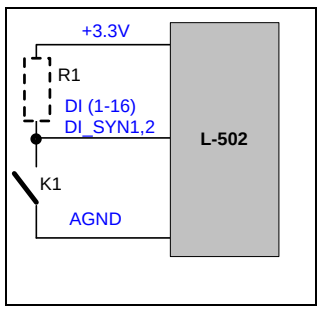
6.3.2. Connecting the LED or the optron input. Option 2



The LED is lit when the DO output is at the "logical zero".

6.3.3. Connecting a contact to a digital input

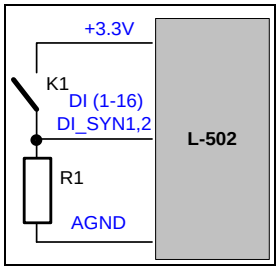
6.3.3.1. Option 1



A logical unit corresponds to an open contact. The recommended resistor R1 nominal is from 3 to 5 kOhm.

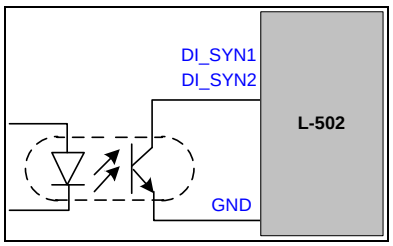
R1 is not required if the internal pull-up resistor is programmed on the corresponding input.

6.3.3.2. Option 2



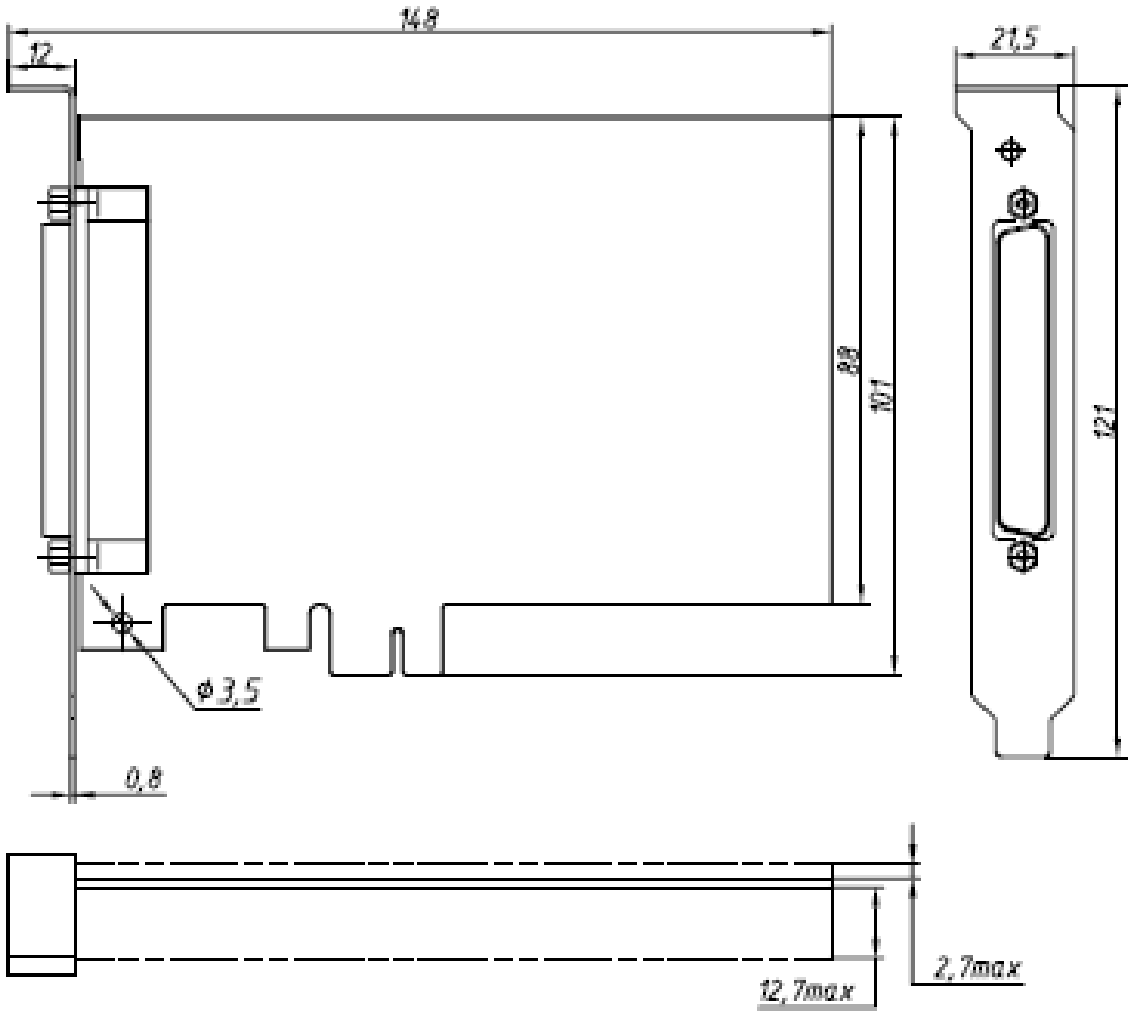
The open contact corresponds to a logical zero. The recommended resistor R1 nominal is from 3 to 5 kOhm. In this case, the internal pull-up resistor should be turned off.

6.3.3.3. Connect the optron output to the synchronization input



The digital inputs DI_SYN1,2, which can be used as synchronization inputs, are adapted to directly connect the optron output. The internal pull-up resistor of the DI_SYN1,2 input must be software-enabled.

Chapter 7. Dimensional drawing



The dimensions are in millimeters.

Bibliography.

[1] L-502. Programmer guide. - M.: L-Card, 2013

[2] Low-level programmer manual for the L-502 board. - M .: L-Card, 2013

[3] A. V. Garmanov. - "Connection of measuring devices. Electrical compatibility and noise immunity". - M.: L-Card, 2003

[4] Terminology for measuring systems – technical support section on the L-Card website: www.lcard.ru/lexicon

[5] **Error! Hyperlink reference not valid.**

List of tables.

List of figures