A family of universal modules of the ADC, DAC

Measuring voltage converters

E20-10
E20-10-1
E20-10-D
E20-10-D-1
E20-10-D-I
E20-10-D-1-I

User manual

Revision 2.01.00
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DAQ SYSTEMS DESIGN, MANUFACTURING & DISTRIBUTION

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Revision history of this document

Manual revision	Date	Notes to the updates
1.00.02 – 1.00.07	05-2006 - 05-2007	Guidelines on **E20-10** revision A release of which was completed in late 2007.
2.00.01	04-2008	The manual is significantly amended, updated due to addition of numerous details on **E20-10** revision B.
2.00.02	04-2008	Table in p. **7.3** is updated, p. **3.3.4** is added, **table 5-5** is updated, error is corrected in **table 6-3**
2.00.03	09-2008	FPGA (p. **3.3.4**) firmware upgrade details are updated.
2.00.04	10-2008	Explanatory figure is added in p. **4.4**.
2.00.05	10-2008	FPGA (p. **3.3.4**) firmware upgrade details are updated.
2.00.06	04-2009	**E20-10** (p. **3.3.2**)design versions designation system is changed and amended
2.00.07	12-2009	Paragraph **6.5.4.3** has new version
2.00.08	06-2010	Paragraph updated **7.1.3**
2.00.09	07-2010	Paragraph **6.3** edited
2.00.10	06-2011	P.**5.2.2** edited. Paragraph **6.5.1** added
2.00.11	03-2012	Manor changes in documentation
2.00.12	09-2012	**ADC frame is oversized up to 8192 samples!** ***Characteristic is added to*** **Table 7.1 : *Zero offset when ADC input is unconnected***
2.00.13	11-2012	Details are added to p. **3.3.4**
2.00.14	02-2013	**Details on revision B.01 are entered. (**p. **2.1**)
2.00.15	03-2013	Paragraph **2.1** edited
2.00.16	01-2014	Paragraph **6.5.1** edited
2.00.17	02-2014	**table 6-7**, p. **7.4**, p. **6.5.1** are updated
2.00.18	12-2014	Details on new firmware 2.00.10, p. **3.3.4** are added
2.01.00	10-2017	Industrial design versions are added The characteristics according to the results preparation of *L-CARD Voltage measuring converter* series for certification as Means of Measurement

The latest revision of this document is always being recorded on the CD-ROM included in the delivery package (p.**3.3**). Besides, you can find the latest revision in the *library of files* on our website http://en.lcard.ru/download.

Contents

1. What this document is about

This document is a *User Manual* written in a[1] user-friendly manner as far as possible. It describes the technical (hardware) properties of **E20-10**, explains the operation rules and principles of functioning, contains specifications and contents of delivery.

This document does not cover any programming or software issues. These issues are given in programmer's manual [1].

So, You need two documents to operate with **E20-10**: user manual and programmer's manual.

1.1. On revisions **A**, **B** and **B.01** of module **E20-10**.

Rapidly developing present element base and technologies and long-term experience in serial production of **E20-10**, many user stories are causes of significant redesigning of project **E20-10**: to add a significant number of additional useful functions and properties saving compatibility with previous functions as much as possible keeping the same value category for data acquisition devices. Revision B is assigned to new **E20-10** and its manufacturing has started with 2008. Revision A executed before the end of 2007 of **E20-10** module is taken out of production but, of course, is being supported by **L-Card,** and its description is given in this manual. **E20-10** of revision B– it is a technologically new device, so, next observe that any changes in **E20-10** revision A into revision B are impossible.

In 2013 L-Card issued new revision **B.01** different from older ones in significantly extended power voltage range, see p. 7.4, page 61.

Complete list of A, B and B.01 revision differences can be found in p. 2.1 of this manual.

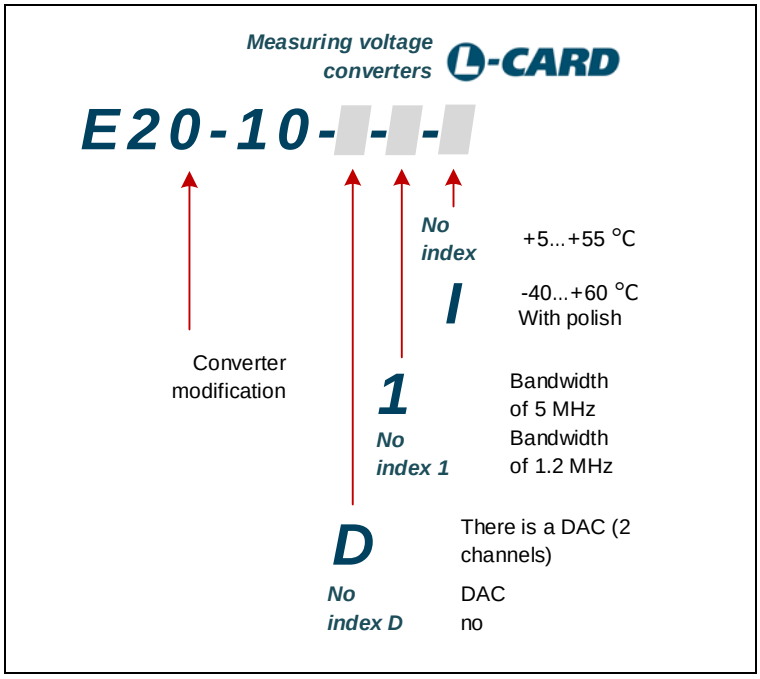
Unless otherwise specified, throughout the text of this manual when it comes to revision B the same information relates to revision B.01 as well.

In 2017 the certification of modules of L-CARD series including E20-10 modules as of industrial versions was started.

Characteristics of revision B.01 given in this manual comply with L-CARD-E20-10 characteristics.

[1] but not according to GOST

1.2. Designation system



1.3. Design versions

- **E20-10** (ADC frequency bandwidth of 1.2 MHz, 2-channel DAC is not available).
- **E20-10-D** (ADC frequency bandwidth of 1.2 MHz, 2-channel DAC is available).
- **E20-10-1** (ADC frequency bandwidth of 5 MHz, 2-channel DAC is not available).
- **E20-10-D-1** (ADC frequency bandwidth of 5 MHz, 2-channel DAC is available).
- **E20-10-D-I** (ADC frequency bandwidth of 1.2 MHz 2-channel DAC is available, industrial design version).
- **E20-10-D-1-I** (ADC frequency bandwidth of 5 MHz 2-channel DAC is available, industrial design version).

Industrial versions (with alphabetic notation "I") designed to operate under temperature from -40 to +60 °C have cards sealed with varnishing that improves the product environmental resistance.

More detailed information on operational conditions see in Appendix 0.

1.4. How to read this manual?

Sketchy information on primary application properties of **E20-10** is given in Chapter 2. This chapter is targeted for wide range of stakeholders.

In Chapters 3, 0, 6 details relating to practical work itself with **E20-10** *are given*. The issues discussed herein will be of interest for specialists and operators.

When exploratory reading, Chapter 5 can be missed because it describes internal architecture of module **E20-10** which is essential when closer looking.

In Chapter 0 the specifications for **E20-10** *are given*. List if characteristics on **E20-10** given herein is intended for specialists.

In Chapter 8 practical information on problems solution under abnormal situations is given.

2. Primary application properties

E20-10 — is a module of high-speed analog-digital conversion with *USB 2.0* interface. The product primary application properties are summed up below in short.

- Continuous 16-bit data acquisition with frequency up to 10 MHz is provided by USB2.0 interface[2].
- 4-channel architecture with one *14-bit ADC,* switch, input buffer amplifiers, filters in each channel. *Due to input buffer amplifiers* the *dynamic switching interference effect is impossible*.
- Each of ADC 4 channels can set in software the following input signal sub-ranges individually per channel: ±3.0V, ±1.0V, ±0.3V.
- *Each channel has LPF (low pass filter)* 3-order with frequency cut-off of 1.25 MHz (optimal bandwidth for 4-channel ADC conversion mode and frequency is 10 MHz) improving signal-noise-rate. Other LPF frequency cut-offs are possible (p. **3.3.2**).
- *ADC conversion frequency* F_{ADC} can be set within the range *from 1.00 to 10.0 MHz.* ADC conversion frequency can be both as set in software, frequency spectrum in megahertz is determined from the formula $F_{ADC} = 30/\kappa$, where $\kappa = \{3,4, 5,..., 30\}$, and as external with any frequency of from 1.00 to 10.0 MHz (lower data acquisition frequency can be reached by interframe delay setting).
- Maximum data acquisition frequency per channel is F_{ADC}/n, where $n = \{1,2,3,4\}$ — number of sampled channels.
- In module control table the *frame* — random sequence *of channel sampling* with length of from 1 to 256 can be programmed. Size of sampled channels will be selected cyclically from the set size table and order of output data samples **E20-10** will comply with channels sequence.
- *Interframe ADC sampling delay can be programmed from 0 to 65535*[3] *of ADC conversion frequency periods* . Due to this the lower sampling frequencies can be implemented per channel.
- Multi-mode system has advanced synchronization modes for data acquisition and/or ADC conversion frequency. For example, by connecting modules **E20-10** according to one *setting device - many receivers diagram* the synchronous multi-module data acquisition system can be achieved!
- Architecture *externally completely downloaded: downloaded* FPGA, controller firmware can be updated. Due to this the user can update firmwares with latest versions by himself.
- *FIFO data internal buffer with size of 8 MV* buffers data saving their loss in case when computer operating system "thinks" [4] (to 400 ms at an acquisition frequency of 10 MHz to 4 s at an acquisition frequency of 1 MHz).
- *Digital input-output* is presented in form of 16 input and 16 output digital TTL-compatible lines. Digital outputs can be optional translated in *the third state*.
- *Two-channel 12-bit DAC* (option) allows to set constant voltage within ±5 V under asynchronous mode operation.
- External device power supply output ±12 V, 35 mA

[2] Under full-speed (USB1.1) mode the maximum available frequency makes 500 kHz
[3] In **E20-10** revision B
[4] for example, in Windows – in non-real-time (off-line) system

- *Power supply of E20-10 from external unregulated source is +8V...+40 V*[5] (power supply circuit from USB is not used). It can be network card of -220/=12 V (included in the delivery.). Under off-line conditions **E20-10** can be energized from external power supply source of from +9 to +27 V. Power consumption — max. 4.5 W[6]. **Revision B.01 for E20-10 module has extended supply voltage range from +8 to +40 V.**

In addition, revision B for**E20-10 module** in comparison with revision A has a number of improved parameters and optional capabilities listed below (p. **2.1**).

[5] for module revision B.01
[6] In **E20-10** revision B

2.1. Complete list of user differences of revisions A, B and B.01 for **E20-10** module

Since 2008 **L-Card** has decided to release **E20-10** of revision B with advanced useful quality.

All **E20-10** modules of 2006 and 2007 production years should be related to revision A (see label on the body bottom), since 2008 **L-Card** has started to produce **E20-10** of revision B.

In 2013 **L-Card** has started to release revision B.01 with extended power voltage range. Revisions B and B.01 are not differed in program. Revision B.01 specified on label on body bottom face, new power voltage range "+8.0...+40 V" is specified on body top cover.

E20-10 module has signed in 2017 as modification in L-CARD Measuring voltage converter series.

All consumer differences of **E20-10** of revisions A and B are given in Table:

Characteristic, parameter, function, property	**E20-10 revision A**	**E20-10 of revisions B and B.01, L-CARD-E20-10**
Data calibration procedure... (p. **5.2.5**)	is performed on computer (by implementing of the relevant library function)	is performed inside **E20-10** by FPGA hardware.
Interframe delay range (p. **5.2.1**)	0-255 ADC conversion frequency periods	0-65535 ADC conversion frequency periods
Power consumption (p. **7.4**)	to 5 W	to 4.5 W
Power supply voltage	+9.0...+27 V	+9.0...+27 V (revision B) +8.0...+40 V (revision B.01)
ADC input offset current software disconnecting capability (p.**6.5.4.1**)	no	yes
Intrinsic input current of ADC analog input (p.**7.1**)	-15...0 µA (typical value -7 µA)	10 nA (typical value), if input current is not specially on
Typical signal-to-noise ratio (p. **7.1**)	70 dB	73 dB
Minimum data acquisition rate at maximum interframe delay and ADC conversion frequency of 1 MHz (p. **7.1**)	7.8 kbyte/s	30 byte/s
Input resistance of analog input	min. 5 MOhm	10 MOhm ± 5%
Inter-channel interference, not more than (p. **7.1**): - at constant voltage - at frequency of 1 kHz - at frequency of 1 MHz	 -50 dB -70 dB -60 dB	 -70 dB -75 dB -65 dB
Operating current of output of +5V of external devices power supply	35 mA	35 mA (revision B) 100 mA (revision B.01)

Characteristic, parameter, function, property	E20-10 revision A	E20-10 of revisions B and B.01, L-CARD-E20-10
Synchronization start modes for data acquisition "according to level" of signal of selected physical channel (p.**5.2.2**)	no	yes
Marker mode of first frame – logic indicator of data continuous section (p.**5.2.3.2**)	no	yes
Capability to set additional permit conditions for ADC data recording in buffer memory **E20-10*:*** - "according to differential" signal in ADC selected channel, - blockage of set number of frames transmission from the beginning of data acquisition (p.**5.2.2**)	no	yes
Mode of hardware acquisition stopping according set number of collected data frames (p.**5.2.2**) On stop the data acquisition restart can be started, for example, per external sync-signal START. In practice this capability allows to implement start-stop operation for several data acquisition start modes	no	yes
In initiating of internal memory overflow 8 MV **E20-10**event recognizable in hardware (computer-caused spooling by USB high delay) (p.**5.2.4**)	data acquisition mandatory computer-sourced restart is required	restart is not required, because of the required minimum number of data frames will be automatically (hardware logic) deleted from buffer memory of **E20-10** to eliminate overflow, and program-accessible overflow indicator is activated.
ADC word size overflow indicator per ADC channel (p.**5.2.6**).	inserted in ADC data flow (in relevant mode initiation)	is not inserted in ADC data flow and raises the relevant program event
External minor construction features (page **15**)	BNC connectors (ADC inputs) have flanges with 4 screws	BNC connectors (ADC inputs) without flanges have one nut retaining
Internal major construction features	2-storied construction based on two boards	More reliable 1-storied single-board construction, in particular, easy-to-use **E20-10** without body as built-in ADC module in Your system [7].
Number of design versions (p. **3.3.2**)	2 (fixed)	4 6 (for L-CARD-E20-10)
Certificate of Means of Measurement	No	E20-10 - Not available L-CARD-E20-10 (under certification)

[7] In this case the references to product **E20-10** of **L-CARD LLC** are required in Your system end user documentation.

As shown in table above, revision B of **E20-10** *module has better useful quality in variety of significant parameters in comparison with revision A!*

3. General description

This chapter describes **E20-10** device application, informs about required and optional equipment, content of software package for CD-ROM as well as contains the start operation instructions.

3.1. Device application

E20-10 is small-bodied multifunctional measuring module connected to PC through USB 2.0-interface. The module is intended for rapid flow capture with ADC conversion frequency of to 10 MHz.

Basic functions of **E20-10**:

- 4-channel ADC of 10 MHz with channel multiplexing, with buffered input, with advanced functions of internal, external, multi-module synchronization
- digital asynchronous input-output
- 2-channel asynchronous DAC (option)

Fast **E20-10** module is complemented with some slower ADC USB-modules: **E-154**, **E14-140**, **E14-440** and is intended for creating multi-channel measuring analog data acquisition systems as well as for digital control and monitoring of external devices state.

3.2. Appearance

Revisions A and B of **E20-10** module have minor external differences (**fig. 3-1**, **fig. 3-2**). In addition, on factory label (on the body bottom) of E20-10 module of revision A the production years 2006 or 2007 are specified, and on label of revision B – 2008 or later. Moreover, on the label the design version of **E20-10** module is specified in compliance with agreed notation (p. **3.3.2**).

Fig. 3-1. **E20-10 revision A *appearance***

Fig. 3-2. **E20-10 revision B *appearance***

*Appearances of **E20-10** of revision B and B.01 are similar.*
Details on revision B.01 are specified on label on body bottom wall.
Power supply voltage range is specified on body top cover.

3.3. Module configuration

3.3.1. Standard supply package

- module **E20-10** *(1* pcs.)
- communication cable on USB 2.0 (1 pcs.) — *A-B type, length of 1.3...2.0 m*
- network card for **E20-10** power supply from alternate current network of 220 V, 50 Hz
- magnetic sweep cable of connector (1pcs.) — *DB-37M* with housing DP-37P — for digital signal cable terminating production
- magnetic sweep cable of connector (1pcs.) — *DJK-10A* — for extern power supply circuit cable terminating production, if required, to energize **E20-10** not from circuit of 220V through attached network card but from different source of +9...+27 V
- magnetic sweep cable of connector (1pcs.) — *MDN-9P* — for production of magnetic sweep cable to external device power supply outputs of ±12 V and to DAC outputs.
- CD-ROM with documents and software.

Attention! DAC is not included in standard supply package (p.**3.3.2**).

If required, use hub stations, power units for them and auxiliary USB-cables. When dealing with **E20-10** the user must buy this equipment by himself in third-party manufacturers. The same is related to not included in delivery package interconnecting wires, auxiliary cables, connectors and terminals to connect signal sources and arrange network interface communications.

3.3.2. Design versions

E20-10 is produced in the following design versions:

Design version	Description
E20-10	Basic design version — without DAC, bandwidth of 1.25 MHz per ADC channel
E20-10-D	2-channel DAC bandwidth of 1.25 MHz of each ADC channel. This version was named as "E20-10D" in old notation
E20-10-1	Without DAC, bandwidth of 5 MHz of each ADC channel (design version is available for revision B only)
E20-10-D-1	With 2-channel DAC, bandwidth of 5 MHz of each ADC channel (design version is available for revision B only)

Attention! Specify the required design version in ordering **E20-10**.

Design version is specified on factory label on the body bottom.

Another ADC channel bandwidths are available as agreed upon with **L-Card**.

3.3.3. Software delivery

3.3.3.1. Operational software

For historical reasons, *L-Card* ***LLC firm*** provide currently two libraries for the user to operate with module **E20-10**, as follows: *Lusbapi* and *LComp*. Both libraries are intended to operate under *Windows'98/2000/XP/Vista* environments. Both *Lusbapi,* and *LComp* provide complete functional support for module **E20-10**. *LComp* library benefit is wider support the product performed by ***L-Card LLC***. So, *Lusbapi* supports **USB** devices only, and *LComp* library provide additionally operation with **ISA** and **PCI** products of *L-Card* ***LLC***.

Attention! Both libraries *Lusbapi* and *LComp* have programming interfaces incompatible completely but they use the same universal **USB** driver named **Ldevusbu.sys**.

3.3.3.2. Library Lusbapi

The whole *Lusbapi* library package is located in accompanied to module branded CD-ROM in base directory \USB\Lusbapi. The same library can be downloaded from our website en.lcard.ru from the section "File Library". There, in subsection "Software for Windows" you should select the self-extracting archive lusbapi*XY*.exe, where *X.Y* denotes the software current version number. At the time of this manual writing, the latest *Lusbapi* library has version **3.2**, and its archive is named lusbapi34.exe.

The structure of arrangement on branded CD-ROM of all *Lusbapi* library components is given in table below (paths are specified relatively to base directory \USB\Lusbapi):

Directory	Intended purpose
\DLL\	***Lusbapi*** **library including all sources, import libraries, declaration modules and, etc.**
\DRV\	USB **driver of module and *inf*-file.**
\E20-10\DOC\	**Documentation Including programmer's manual on operation with *Lusbapi* library.**
\E20-10\Examples	**Designs on module programming examples across different development environments:** Borland C++ 5.02**,** Borland C++ Builder 5.0**,** Delphi 6.0 **and** MS Visual C++ 6.0**.**

To provide Your applications proper operation with module **E20-10** it is recommended to copy binary file of \DLL\Bin\Lusbapi.dll library to directory %SystemRoot%\system32, that can be implemented by using finished batch file \DLL\CopyLusbapi.bat. This operation is often applied because *Windows'98/2000/XP/Vista*, if required, searches automatically the required libraries in specified directory. On the other hand, Lusbapi.dll library can be conceptually located in directory of ultimate application or in one of the directories specified in environment variable PATH.

All user required components of *Lusbapi* library (include files, programming examples and, etc.) are moved to target computer by copying of required directories and files from delivered branded CD-ROM.

3.3.3.3. LComp library

LComp library is presented in form of installation tool LComp.exe, which is located on branded CD-ROM in directory \DLL\LComp. The same library can be downloaded from our

website en.lcard.ru from the section "File Library". There, in subsection "Software for Windows" you should select self-extracting archive lcomp.exe.

Installation tool LComp.exe is intended for proper arrangement of all components of *LComp* library on user's computer. Moreover, such required *LComp* components as sources, import libraries, declaration modules, programming examples, electronic documentation and, etc. will be located in directory assigned by the user in library installation.

3.3.3.4. Optional software

- Free program ***L-Graph II***. It is intended for operation on *Windows'XP* only. ***L-Graph II*** operates with module **E20-10** through *LComp* library. This program is higher-end version of ***L-Graph I***. For example, it offers the possibility to user *to view* and record data from ADC simultaneously. ***L-Graph II*** can be installed using installation tool \LGraph2\setup.exe from branded CD-ROM attached to the module. ***L-Graph II*** distribution can be also downloaded from our website en.lcard.ru from the section "File Library". There, from subsection "LGraph2 software package" you must select distribution lgraph2.zip.
- Commercial program of multi-channel recorder ***PowerGraph***. The program is intended to record, process and hold analog signals and allows to use personal computer as tape recorder. *Windows'98/2000/XP/Vista*. Developing, delivering and technical support – **"Interoptica-S** "*LLC* , www.powergraph.ru. Standard software package delivered with module **E20-10** includes demo version ***PowerGraph*** located in directory \P_graph on our branded CD-ROM.
- Commercial automation complex ***ACTest*** for experimental and process plants. This complex is intended to real-time view, record, store and process data. *Windows'98/2000/XP*. Developing, delivering and technical support – **"Automated systems laboratory"** *LLC*, www.actech.ru. Standard software package delivered with module **E20-10** includes demo version ***ACTest*** located in directory ACTest on our branded CD-ROM.

3.3.4. FPGA firmware versions

In **E20-10** FPGA firmware version and creation date are programm-accessible [1]. The current delivered FPGA firmware is integrated into delivered program library functions. Conceptually, you can update **E20-10** firmware by two ways: download upgraded software in "Files library" or order FPGA firmware new file in **L-Card** (en@lcard.ru) and use it in calling initialization function **E20-10**. The last way is technically appropriate only if exchanged FPGA firmwares are compatible on program library functions – this and rest user information about available firmwares of **E20-10** is given in table below.

You can find out about actual FPGA firmware of Your module **E20-10** using utility ModulesViewer which can be downloaded from website **L-Card** from section **Files library**.

Firmware version	Firmware description
1.00.06 dd. 15.01.07.	Final firmware **E20-10** rev.A.
2.00.03 dd. 10.04.08.	First firmware of serial **E20-10** rev.B. Users applying internal calibration in **E20-10** rev.B are recommended to update firmware to elder version where the effect to damage individual data samples in code approximating to ADC word size edge has been eliminated. Negative effects have not been found when internal calibration is off.
2.00.05 dd. 24.07.08.	Updated firmware of serial **E20-10** rev.B. In FPGA 2.00.05 firmware the additional program start is not required under additional startup condition "on signal passing through given level in selected channel" and shutdown condition "on number of M recorded frames", due completing of the next shutdown condition fulfillment the additional data acquisition start will begin automatically upon completing of new start condition fulfillment. For another start conditions FPGA 2.00.05 firmware is similar to 2.00.03 firmware. Also refer to **table 5-5** notes to it. FPGA 2.00.03 and 2.00.05 firmwares are fully compatible on program library functions.
2.00.06 dd. 01.09.08r.	Updated firmware of serial **E20-10** rev.B. One-channel mode sensitive data acquisition fault has been eliminated**.**
1.00.07 dd. 29.10.08.	Updated firmware of serial **E20-10** rev.A. Data corruption in repetitive interleaving of external start and program shutdown has been eliminated (this relates to rev.A only). FPGA 1.00.07 firmware means simultaneous upgrading of AVR controller firmware.
2.00.07 dd. 05.09.12.	For E20-10 rev.B the embedded software upgrading enabling to boost **maximum possible frame size up to 8192 samples of ADC** has been developed! To upgrade it is required to alter AVR controller and upgrade library remotely (FPGA 2.00.07 firmware has been yet added in which). Compatibility with old software of upper level is existed.
2.00.08 dd. 20.11.12.	Firmware for E20-10 rev.B. In comparison with version 2.00.07, the fault on odd data interference in ADC buffer in additional data acquisition starting on signal START under data acquisition program shutdown mode has been eliminated.
2.00.10 dd. 15.12.14.	Firmware for E20-10 rev.B. Data acquisition restart on signal START fault has been eliminated.

4. Installation and customization

4.1. Module connecting to computer

Inspect package and product components for mechanical damages. Switch on the computer if it was off and download operating system *Windows'98/2000/XP/Vista*. These particular operating systems are enabled to support adequate operation of **USB** interface.

USB interface specification provides users with operational capabilities to work with peripheral devices under true mode ***Plug&Play***. This means that **USB** standard provides device*"hot"* connection to live computer, its automated recognition by operating system immediately upon connecting and next downloading of drivers relevant to this device. Moreover, **USB** device can be disconnected from computer at any time. In addition, the computer can be switched on if **USB** device has been previously connected.

Hardwared connecting of module **E20-10** to computer is as follows: apply external power to **E20-10** by connecting network card included in delivery package, connect **USB** module connector to computer **USP** port using cable included in delivery package. All specific aspects to connect signals are described in Ch.6, in particular, on connecting to USB, refer to p. **6.5.1.**

Note that when operating with drivers LComp you should download first the drivers **4.2.2** and connect **E20-10** once this is done.

4.2. USB drivers installation

Procedures on **USB** drivers installation from libraries *Lusbapi* and *LComp* are a bit different for **E20-10** module. These particular differences are described in the following two paragraphs.

4.2.1. USB drivers installation from Lusbapi

When very *first* connecting of **E20-10** module to computer using included standard **USB** cable the operating system should request driver files for *first-time* connected **USB** device. In this case, it is required to specify *inf*-file from *Lusbapi* library from our branded CD-ROM: \USB\Lusbapi\DRV\Lusbapi.inf. While doing so the operating system copies itself all files required for it to necessary slots and performs all necessary entries in its registry. *Windows* system should subsequently perform so called *enumeration procedure of* **USB** device, see description below in **p. 4.3** **"Recognition of** the module".

4.2.2. USB drivers installation from LComp

Prior to use module **E20-10** with application of *LComp* library it is required to perform installation tool LComp.exe located on branded CD-ROM in directory \DLL\LComp. In addition, this tool installs to user target computer all necessary files required for operating system during recognition module **E20-10** when it is firstly connected to computer **USB** port. Upon successful completion of program LComp.exe only you may connect module to computer using included standard **USB** cable. While doing so, *Windows* system shall perform numeration *procedure for* **USB** device, see description in the following paragraph of this manual.

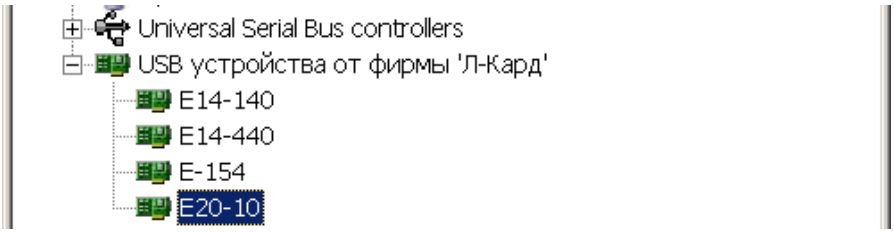
4.3. Recognition of the module

As was mentioned above, the operating system *Windows* shall perform numeration *procedure* for each connected **USB** device. Such procedure for **USB** devices is performed on-the-fly when they are connected to computer without any user interacting or client software.

During the execution of *numeration* **the module USB** indicator – LED, located near to **USB** connector **E20-10**, shall flash continuously, and upon completion it shall be red or green. This will mean that connected **USB** device is recognized properly by operating system and is ready for further operation. Indicator's color informs about **E20-10** connection speed to interface USB[8]:

- **red – full speed,**
- **green – high speed.**

You can further check connected module validity of recognition by operating system in *"Device Manager"* . There, in appeared section *"***L-Card** *USB devices"* device **E20-10** will be displayed, as it, for example, is shown in figure below:



In further working with module **E20-10** the operating system will already know the location of driver for this type of the device and will load it automatically during product connecting to the computer.

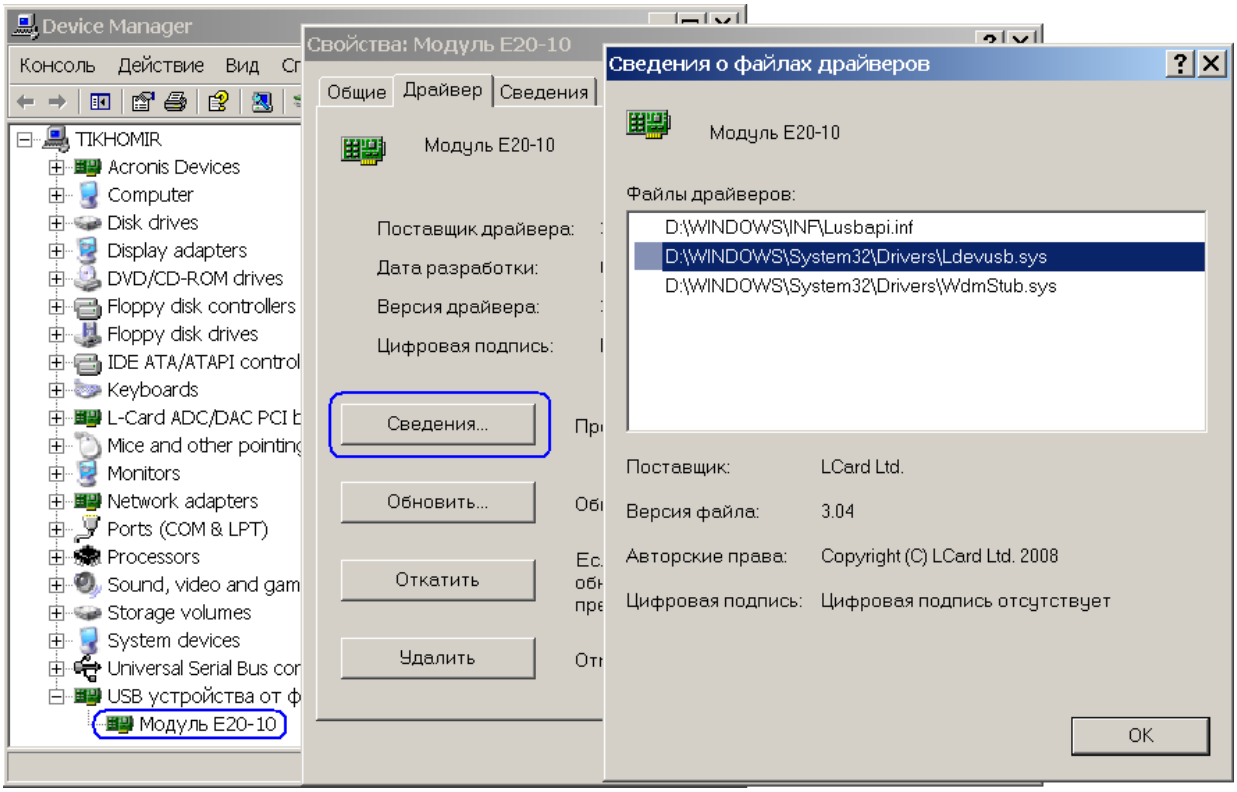
[8] In **E20-10** revision B the indicator is flashing when data transmitting on USB–it is a natural occurance.

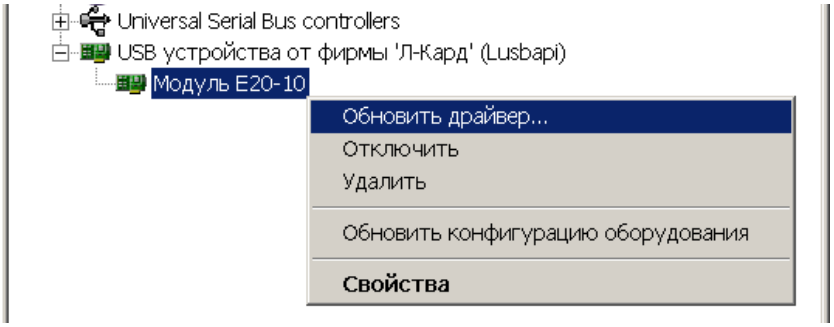
4.4. Differences in USB driver of Lusbapi library

From the version **3.2** in *Lusbapi* library the primary file of **USB** driver, now it is called **Ldevusbu.sys** instead of old **Ldevusb.sys**. So, those users who has already installed on computers **USB** drivers from *Lusbapi* library of version **3.1** or later shall be very attentive during moving to newer library, because he must change module **E20-10** to operate with new **USB** drivers. To do this the user must perform several standard actions using *"Device Manager"* .

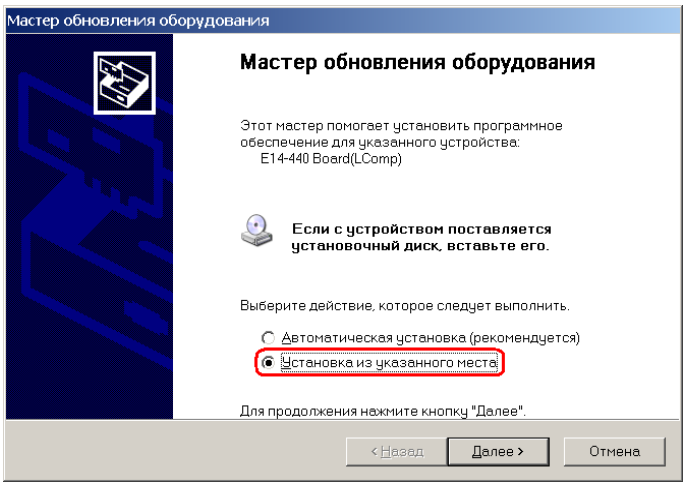
Firstly, you may verify that module **E20-10** connected to the computer operates with old **USB** driver **Ldevusb.sys**. To do this you should find in *"Device Manager"* the device of module **E20-10** type and consecutive call of panel with its features. Then, on this panel you should move to bookmark *"Driver"* on which click on button *" Driver Details…"* . In this case the panel with list of all drivers enabled for selected device will appear. In our case, driver **Ldevusb.sys** shall be in this list. This means, that to operate with module **E20-10** the USB drivers from *Lusbapi* library of version**3.1** or older are used.

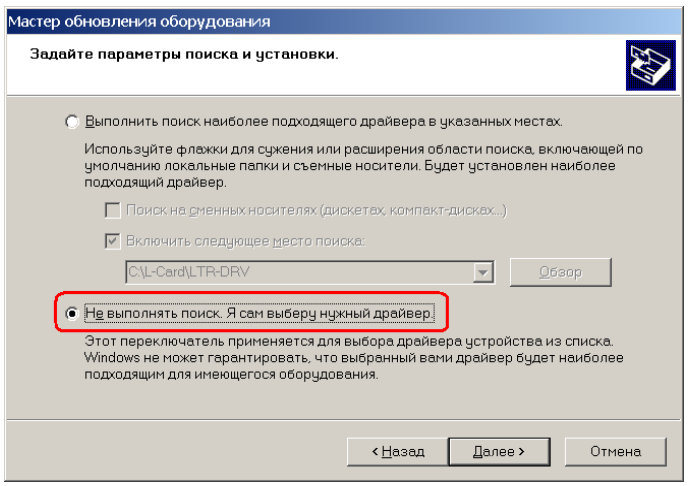
To move to new **USB** driver (from *Lusbapi* library of version **3.2** or newer) you should perform the following actions. Select in *"Device Manager"* the same module**E20-10** mentioned in previous paragraph and call pop-up menu using right clicking. The following picture must be as a result of these actions:



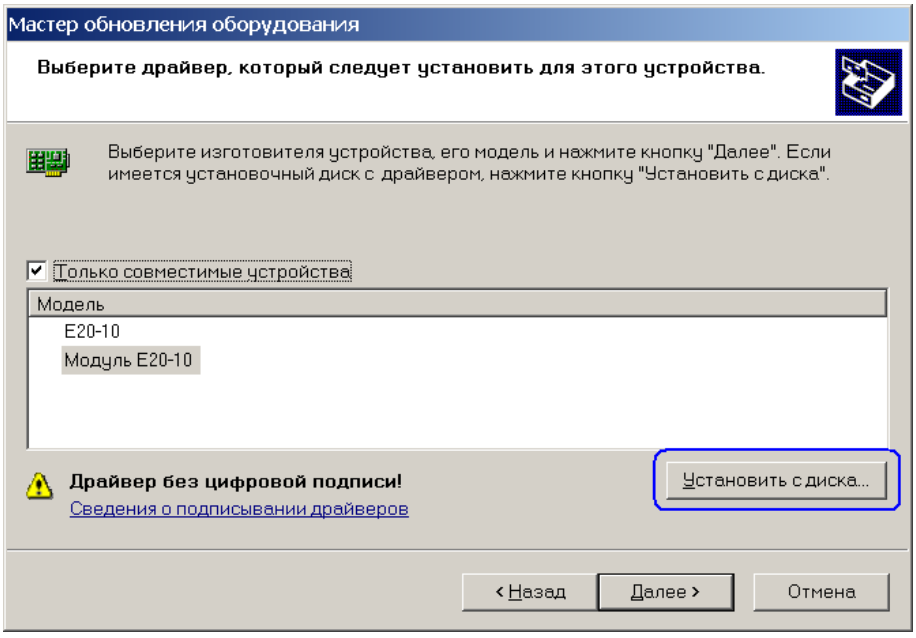


Then, you should activate the driver upgrade point using left clicking. It should be noted that depending on *Windows* configuration the information panels of type to alert about failure of driver digital signature and propose to find drivers in Internet may be displayed. Then, you should move to standard information panels *"Hardware Update Wizard"* on which you should specify selection variants given on figures below and click button *"Next"* :

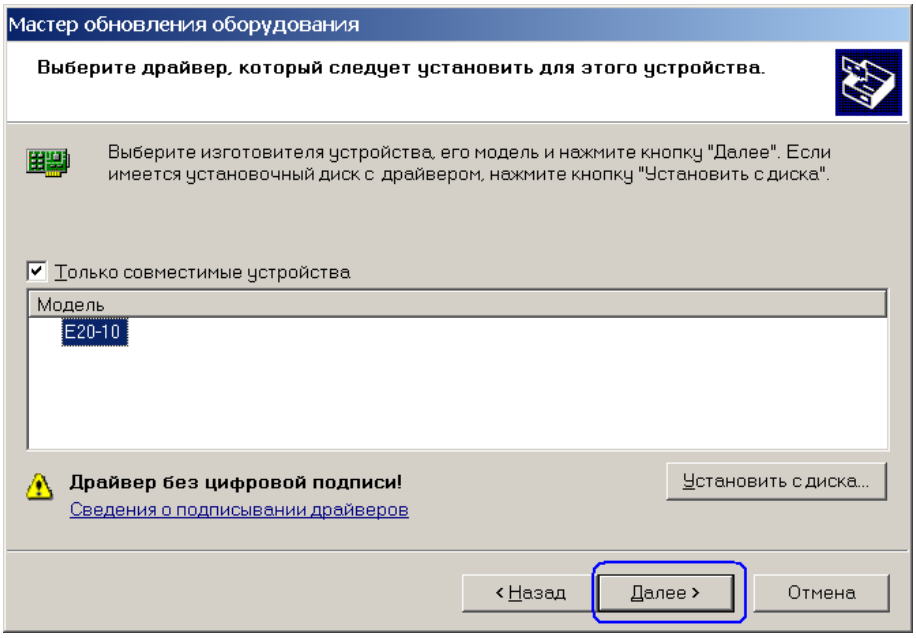




Then, the following panel will appear on which you should just click the button *"Have Disk…"* ().



In this case, in appeared dialogue box *"Install From Disk "* you should specify *inf*-file \USB\Lusbapi\DRV\Lusbapi.inf from our branded CD-ROM and click button*"OK"*. Upon completion, on return to previous panel you should click button *"Next"* :



Now, the only you need is to drive the nail home, in other words, you have to be reassured by *Windows* that drivers installation for module **E20-10** is completed successfully and the device is ready for further operation.

In general, to operate with **E20-10 USB** drivers both as of old (version**3.1** or older) as new (version**3.2** or newer) *Lusbapi* libraries can be simultaneously installed on computer. The thing is **USB** driver from exactly which library would be selected by operating system during module connecting to computer. You may clear up this situation and make a decision on used (*active*) **USB** driver by viewing in *"Device Manager"* as it was mentioned in the beginning of this paragraph. Using operational tools of *"Device Manager"* you can switch back and forth with reasonable facility among both **USB** drivers, i.e. as you want you can make active these particular drivers which are required for current operating with module **E20-10**.

5. Overview of the hardware components and operation principles

Firstly, the description of hardware components which provides insight into **E20-10** operation principles is given in this chapter and detailing of operational characteristics is given below. Description does not cover low-level definition of hardware but it is quite sufficient for understanding of product important performance characteristics.

5.1. Block diagram

Module **E20-10** contains process nodes shown on diagram (**fig. 5-1**). Consider next functional unit **E20-10** according to this diagram.

Four identical analog paths consist of input offset current control circuit, input static commutator, controlled amplifier, active LPF of 3-order.

Input offset current control circuit is available in revision B of module **E20-10** only. In revision A typical input offset current makes -7 μA (in particular, this current caused overswing to ADC scale negative values under quiescent ADC analog input). This current was amplifier component property applied in revision A. Amplifier with incomparably lower input current may be applied in revision B. But, due to the fact of input current existence of revision A could be used in different propositions (for example, as signal external source connecting sign), that in revision B the negative offset current can be live on command (therewith, offset current is generated artificially) to be compatible with old revision, but *input offset current is dead by default in revision B* (p.**6.5.4.1**).

Input static commutator is designed to engage mode for measuring module **E20-10** own zero independently per ADC channel. Measuring of own zero prior data acquisition session and program record-keeping of measured value may compensate long-term temperature and time ADC zero drift. It should be noted, that this commutator is unappropriated for such zero compensation "on-fly" (i.e., during data acquisition).

Controlled amplifier has 3 transfer ratios programmed individually for each ADC channel. These transfer ratios implement input ADC subranges: ±3 V, ±1 B, ±0.3 V.

Active LPF in basic version has boundary frequency of 1.25 MHz (optimal for 4-channel mode at maximum acquisition frequency), and another versions[9] of **E20-10** with other boundary frequencies are technically possible (p. **3.3.2**).

Signal from active LPF outputs of each channel enters to *dynamic commutator performing* switching of signals with ADC conversion frequency from four analog paths to ADC input. Channel numbers switching sequence is arbitrarily given in control list.

Pipelined ADC — 14-bit high-frequency ADC of LTC2245 type of Linear Technology. This ADC has two major features which have a direct effect on **E20-10** architecture: deeply pipelined architecture of this ADC, ADC conversion frequency range of from 1.0 to 10 MHz.

Data enters to FPGA from ADC output. In revision A **E20-10**, beside the above mentioned mixing of ADC word size overloading feature the data flow is not further converted because calibration procedure is implemented here by upper-level tools (in computer). To calibrate flow of 10 megasamples per second (20 MB/s) "on-the-fly", especially if more than one module **E20-10*is connected to the computer,*** – is a resource-intensive procedure even for modern computer, so,*in revision B of module* **E20-10** *the data calibration procedure is implemented by FPGA tools*.

[9] this issue are to be arranged with L-CARD

In module of revision A the series Acex FPGA is used, in revision B the more resource-intensive FPGA of series Cyclon is used. These downloaded FPGA of Altera corporation perform full range of fast-acting logic operations in **E20-10**. FPGA firmware is downloaded from the computer through USB at each program initialising of **E20-10**[10]. **L-Card** does not rule out FPGA firmware upgrading (see p. 3.3.4) due to updating of **E20-10**.

Microcontroller AVR AtMega162 of Atmel corporation (hereafter - AVR)— this controller performs asynchronous programmable control of module (on upper-level commands), supporting information interchange through USB, FPGA downloading and control procedure, storing calibration factors and product serial number.

In revision A **E20-10** USB-controller ISP1581 is used – this is low-level USB controller controlled from AVR. More advanced USB-controller ISP1583 is used in revision B. Both these controllers of NXP corporation support protocols of full- and high-speed USB interface.

SDRAM -based FIFO buffer of 8 MV is used to buffer ADC data flow. Such depth of the buffer is quite sufficient for operating under any operating system at ADC maximum conversion frequency of 10 MHz [11]. Control logic of SDRAM is implemented in FPGA (detailed information about FIFO see in p.**5.2.4**).

*Two-channel asynchronous **DAC*** (option) is controlled from AVR asynchronously only using *control pipe* of USB interface and by relevant function of upper level.

Digital input register DI1...DI16 strobes 16 TTL-lines of data exactly parallel from digital inputs, AVR reads register content. *Note, that DI16 line has programmable alternative function of bi-directional acquisition signal START* .

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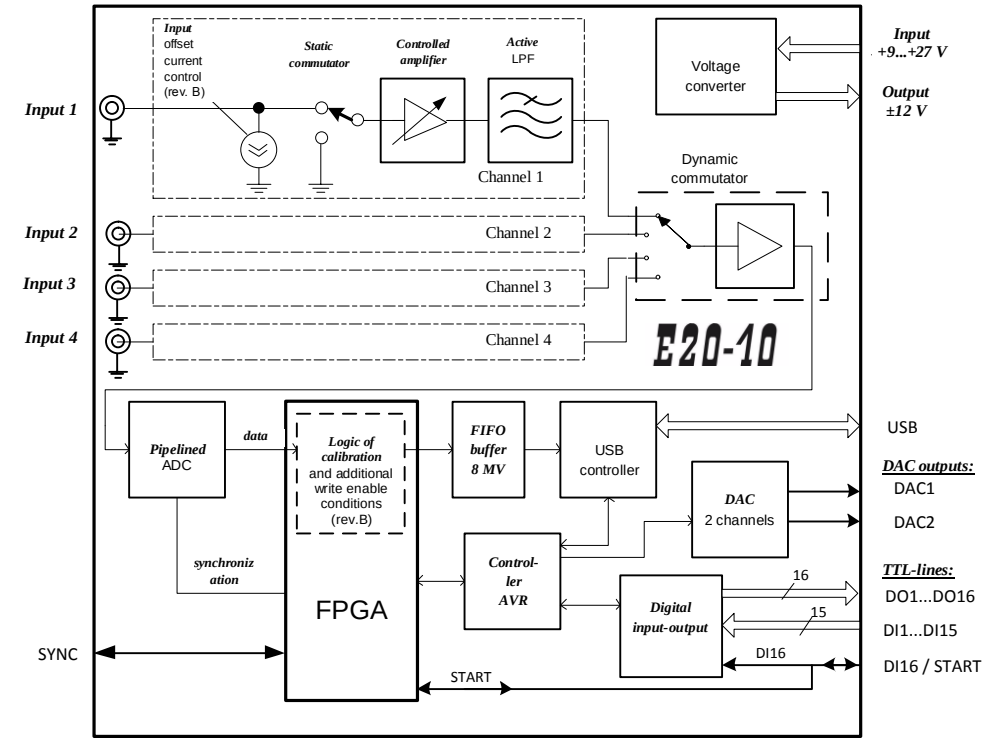
[10] it is enough to download firmware once upon **E20-10** energizing

[11] without interframe delays and other settings slowing down data acquisition



FPGA

***Fig. 5-1. Block diagram* E20-10**

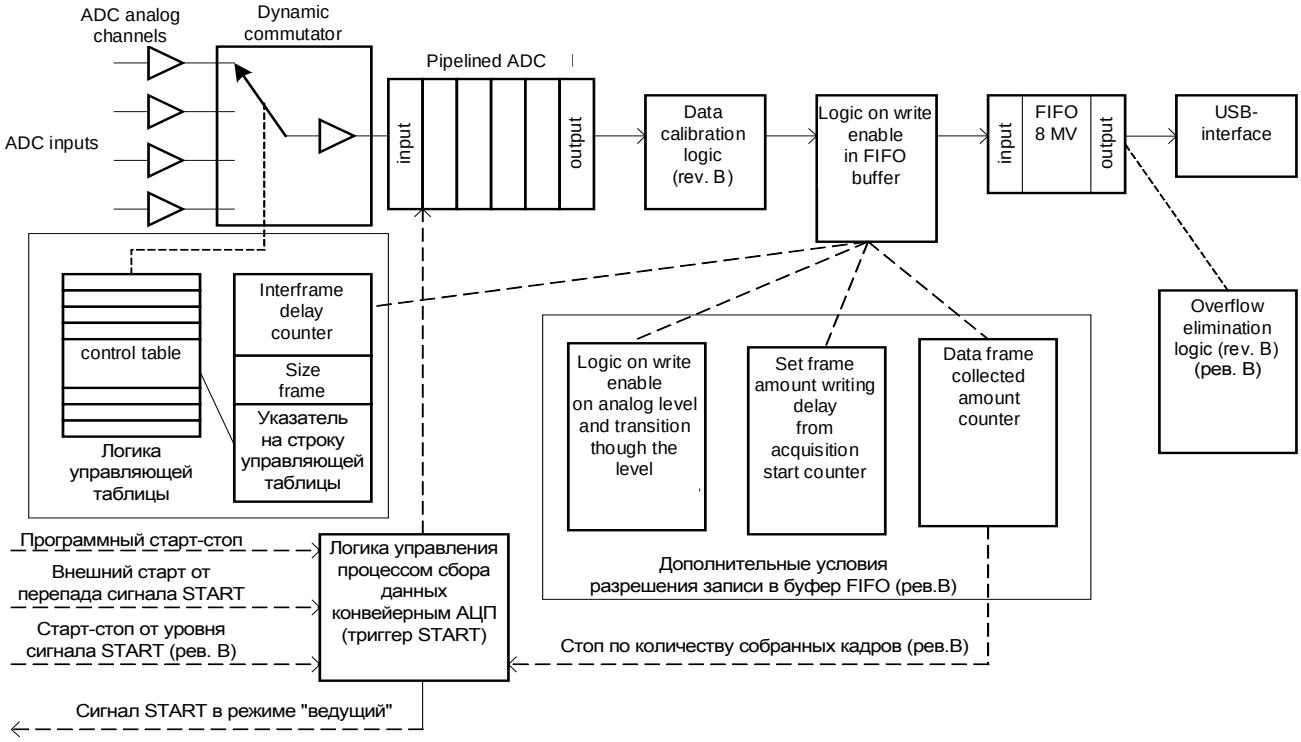


***Fig. 5-2. Explanation of data acquisition equipment logic interaction in* E20-10**

Digital output register DO1...DO16 sets exactly parallel 16 -bit data on TTL-outputs for programmable controllability of the third outputs state as well as for controllability of the third state on signal EN_OE (**table 6-2**).

START acquisition start synchronization input-output. If digital line DI16 for input asynchronous function is not active, then this digital line may be set in software to functions "master" (output) or "slave" (input) of START signal. These features can be used, for example, for multi-module synchronization of data acquisition start for several **E20-10** according to diagram "one master – some slaves" (p. **5.2.2**).

Digital *input-output of ADC synchronization frequency SYNC* can be used fro multi-module synchronization of ADC conversion frequency synchronization of several **E20-10** according to diagram "one master – some slaves" (p. **5.2.2**).

Voltage converter converts unstable input voltage of +9V...+27V into stable power supply voltages for internal nodes of **E20-10**. Auxiliary voltage of **±12V** is output from transmitter output to analog outputs connector of module *E20-10* for external device power supply.

LED indicator (not shown on diagram, output to front panel of module) is controlled directly from AVR. Connection conditions on USB and other events are signalized by mode and color of emission, details see in *Programmer's manual* [1].

5.2. **E20-10** operating principle.

USB-module **E20-10** does not use power supply circuit of USB 2.0 interface. To switch on module it is required to apply power voltage of +9.0V...+27V to it[12] through power connector (p. **6.3.1**) from network card including in delivery package (p. **3.3.1**) or from external constant-voltage source. Power supply circuit parameters for **E20-10** see in p. **7.4**.

Upon switching on the program of USB-device upgraded in AVR completes procedure on connecting on USB as soon as computer connection will be detected.

Upon successful detecting of **E20-10** by your computer operating system the[13] module is ready to operate on level of software applications using delivered by **L-Card** library functions, in particular, one of these functions is FPGA **E20-10 downloading –** this download is required to be performed once upon as **E20-10** switching on (see *Programmer's manual* [1]).

At the close of FPGA download from software level all information about this module **E20-10**, in particular, *serial number, module revision, AVR firmware version, FPGA firmware version* will be available.

Prior to start data acquisition it is required to configurate it in software, because *you may not change configuration settings during data acquisition*. Main configuration parameters are:

- *ADC conversion frequency* (within the range of from 1.0 to 10 MHz).
- *Data acquisition frame size: frame size, interframe delay duration* Number of sampled input channels can be flexible configurated from 1 to 4. ADC conversion frequency is divided among sampled channels in accordance with their quantity and sampling order (frequency). The required sampling order of channels forming the frame is previously recorded in control list with size of from 1 to 256 ADC paths, m. When data acquisition the numbers of channels are repeatedly read with given ADC conversion frequency (1...10MHz) and are sent to dynamic commutator as control signal. To achieve data acquisition lower frequencies the interframe delay is programmed which allows to achieve lower data acquisition frequencies. Under given nonzero interframe delay upon completion of control list access cycle (in frame completion) the relevant number of

[12] On trigging **E20-10** power supply voltage should be min. +9.5 V.

[13] device driver installation is performed under first-time connecting (p.**4.2**)

nonoperating periods of ADC conversion frequency is inserted; data on these periods are deleted on hardware level and, due to this, traffic on USB is not overloaded with garbage.

- *ADC conversion frequency synchronization mode* (p. **5.2.2)**. To implement external and multimodule synchronization mechanism of ADC conversion frequency you should use configured bi-directional TTL-signal SYNC (p. **6.3.1**).
- *Acquisition start mode* (p. **5.2.2**). To implement external, multimodule synchronous start of data acquisition you can use configured bi-directional TTL-signal START (p. **6.3.1**).
- *ADC channel input parameters*. It is noteworthy, that each channel individual installations on required voltage input subrange, on input offset current as well as on own zero measurement mode are not controlled in real time (synchronously) but they are controlled statically and asynchronously from AVR.

Main functional nodes engaged in data acquisition are shown in **fig. 5-2**. Note, that fairly large number of new functional nodes implemented in revision B have not been available in revision A (see verbal instructions of "Rev. B" on this figure).

In **E20-10 of revision A** "data acquisition control logic" is starting of "ADC —FIFO—USB-interface" pipeline from program start event or from external START signal edge. In fact, "START Trigger" indicates ADC start state (in combination with control list logic). In revision A pipeline stopping (START trigger clearing) is performed according to program pipeline stopping event only (followed by FIFO data clearing) and logic of write enable in FIFO buffer is activated from interframe delay mechanism only (interframe delay key point is described in p. **5.2.1**). Specifically, that START output signal state under "master" mode is fully complies with "START trigger" state.

In **E20-10 of revision B** the additional logic of write enable in FIFO buffer (acquisition stopping) which is directly relating to data analysis at ADC output is interstitial downstream of ADC pipeline but upstream of FIFO buffer: write enable on analog level, given amount of frames from acquisition start write delay counter, collected frames amount counter. All these new functional nodes are involved in new synchronization mechanism of revision B (see description of all synchronization modes in p. **5.2.2.1**), but, it is important to note, that these mechanisms are completely related not to acquisition pipeline starting but to operation of write enable to FIFO buffer mechanism only against ADC previously triggered in conjunction with "control list logic".

It follows, that "START trigger" as well as START sync signal under "master" mode behavior logic is unrelated to "added logic of write enable in buffer". This feature will be essential to the understanding of synchronization modes described below (p.**5.2.2**) where START signal is involved.

5.2.1. Channel sampling principle

In **E20-10** acquisition frame size can be set of from 1 to 256 (to 8192 ADC paths in FPGA new firmware, p. **3.3.4**). The following can be set: random sequence of channel numbers inside the frame, specified in control list as well as interframe delay of from 0 to 255 ADC conversion frequency periods (for **E20-10** of revision A) or from 0 to 65535 ADC periods (for **E20-10** of revision B). The given size of control list is always equal to acquisition frame size. Under any synchronization mode the data acquisition start is always bound to channel number specified on top of control list and nonzero interframe delay is always inserted upon completion of last channel number sampling at the bottom of control list of a given size. In any case, if data acquisition is not stopped the next channel number will be taken from top of control list (and following the period of frame given size from 1 to 256) upon completion of channel number sampling given in last string of control list. Each period of ADC channel number periodic reading from control list as well as each period of interframe delay counting are bound to given ADC conversion frequency period of **E20-10** (from 1.0 to 10 MHz).

5.2.2. *Synchronization in* **E20-10**

If synchronization is not required, that internal ADC conversion frequency source is used in **E20-10** as well as simple program data acquisition start. But, **E20-10** has also external synchronization tools both as on *ADC conversion frequency* as on *acquisition start*. These are two independent mechanisms which can be used both as separately and as together.

Synchronization on ADC conversion frequency (within possible range 1.0 – 10 MHz) is performed using SYNC line which can be configured in software to output or to input (**table 5-1**). Due to this the following problems can be solved:

- ADC conversion frequency -based synchronization of several **E20-10**. To do this you should switch on several **E20-10** according to diagram "master-slaves" connecting similar circuits GND and SYNC of several **E20-10.**
- Conversion frequency synchronization signal **E20-10** generating to external device, for example, to frequency meter to monitor conversion frequency.
- External synchronization on TTL-signal (with frequency of 1.0 – 10 MHz and on-off time 2) for external synchronization of one or more **E20-10** on ADC conversion frequency.

The following problems may be solved using acquisition start synchronization via START line configured in software to input or to output (**table 5-2**):

- Transmitting of acquisition program start internal signal through START line for synchronous starting data acquisition in other modules **E20-10**. To do this, you should switch on several **E20-10** according to diagram "master-slaves" connecting similar circuits GND and START of several **E20-10**
- **E20-10** data acquisition start synchronization from external source of TTL -signal.
- Transmitting of acquisition program start internal signal in **E20-10**through START TTL-line to external device for synchronization or indication of data acquisition process.

Module **E20-10** of revision "B" supports *additional permit conditions for ADC data recording in buffer memory of* **E20-10** (on edge in selected ADC channel, disabling transmission of given amount of frames from acquisition start)**,** as well as *additional conditions for acquisition stopping* (on data collected frames amount). In addition, "on level" data acquisition mode series is added in revision B. These additional synchronization conditions improve synchronization tools of module **E20-10** of revision "B" in comparison with revision "A".

The following limitation should be noted: *additional conditions for ADC data recording and acquisition stopping permit conditions can be applied inside one* **E20-10** *module only and they have no effect on START signal behavior in intermodule synchronization according to master-slaves principle.* At the same time, if desired, in different modules **E20-10** the similar auxiliary conditions for data recording and acquisition stopping permit conditions may be made , and as a result, under connecting "master-slaves" modules **E20-10** on START signals you may achieve conditions for synchronous operation of *additional conditions for data and acquisition stopping recording permit conditions* in different modules **E20-10** .

It is natural, that in multimodule connections of **E20-10** on "master-slave" principle the user must judiciously configurate control lists, interframe delays (and in **E20-10** of revision B the additional conditions for buffer write enable as well) of these modules in order to be able to make sense of relative time connections among the sample flows obtained from these modules. Master **E20-10** should be earlier started in software to collect data, because they should enter in start waiting from master, and in this case, upon slave data acquisition starting completion the data acquisition in masters will be started in hardware and synchronously with slave **E20-10**.

It should be noted, that when SYNC line configurating to function "slave" (under external synchronization of ADC conversion frequency from digital TTL- sync signal external source) it will

be incorrectly to feed SYNC pulses outside more rapidly than in 100 ns (10 MHz) or less often than in 1000 ns (1.0 MHz), because under this mode SYNC pulse is fed directly to ADC LTC2245, and, according to manufacturer's documents, this ADC operates within conversion frequency range of from 1.0 to 10 MHz. Severe requirements are also posed on SYNC signal on-off time (p.**7.1.3)**. It is natural, that SYNC signal from "master" **E20-10** complies with these requirements.

Note, that TTL-line DI16/START configurated "on input", electrically has pull-up resistor (providing specific one state of unconnected input), and TTL-line SYNC configurated "on input" does not have pull-up resistor, i. e. *certainty of SYNC unconnected input state is not provided*, **table 6-2.**

5.2.2.1. Synchronization modes

Possible synchronization modes for **E20-10** are given in tables below. Take note of information about what exactly revisions of **E20-10** one mode is implemented.

Table5-1. Modes of synchronization on ADC conversion frequency (on SYNC signal)

Synchronization on ADC conversion frequency	Implemented in revisions of E20-10	Notes
"internal"	A, V	ADC conversion frequency: $\frac{30}{n}$ MHz, where, n=3,4,5,…,29,30. SYNC line is not used (transfered to Z-state)
"internal-master"	A, V	SYNC line is configurated to output: signal with on-off time 2 and ADC conversion frequency is generated: $\frac{30}{n}$ MHz, where, n=3,4,5,…,29,30. ADC data physical sampling moment corresponds to SYNC output signal edge
"external - slave"	A, V	SYNC line is used "on input" for synchronization from TTL-output of external device: signal with frequency of from 1.0 to 10 MHz, with on-off time 2 (meander) is required

Table5-2. Acquisition start synchronization modes (on START signal)

Data acquisition start synchronization	Implemented in version E20-10	Notes
"software": - without additional start conditions - with additional start conditions, **table 5-3**	 A, V V	Software asynchronous start. Stopping possible conditions – **table 5-5** START line is in Z-state
"software – master on START signal": - without additional start conditions - with additional start conditions. **table 5-3**	 A, V V	START signal of master **E20-10** is fed by active level "1" (connected slave **E20-10** shall be in "on START signal edge" condition). Stopping possible conditions – **table 5-5** START line is in "on output" state

Data acquisition start synchronization	Implemented in version E20-10	Notes
"external - slave on START signal edge": - without additional conditions - with additional start conditions. **table 5-3**.	 A, V V	Start on START signal Stopping possible conditions - **table 5-5**.
"external – slave on START signal fall": - without additional conditions - with additional start conditions. **table 5-3**.	 A, V V	Start on START signal Possible stopping conditions see in **table5-5**.
"on level" data acquisition synchronization modes, **table 5-3**.	V	On signal analog level in selected channel

Table 5-3. Capability to set additional permit conditions for ADC data recording in buffer memory* E20-10*:

Additional conditions	Implemented in version E20-10	Notes
Blockage of given *N* number of frames recording from the acquisition start	B	$0 \le N \le 16777214$, where, N-integral
On bottomup transition through the given signal level in selected channel and blockage of *N* number of frames recording from acquisition start	B	$0 \le N \le 16777214$, where, *N*-integral
On top-down transition through the given signal level in selected channel and blockage of *N* number of frames recording from acquisition start	B	$0 \le N \le 16777214$, where, *N*-integral

Table 5-4. "On level" synchronization modes

"on level" acquisition modes (acquisition start and stop is performed on signal level)	Implemented in revision E20-10	Notes
"on signal level above threshold of signal in 1 ADC channel"	B	Stopping will occur at frame end edge
"on signal level above threshold of signal in 2 ADC channel"	B	
"on signal level above threshold of signal in 3 ADC channel"	B	
"on signal level above threshold of signal in 4 ADC channel"	B	
"on signal level below threshold of signal in 1 ADC channel"	B	
"on signal level below threshold of signal in 2 ADC channel"	B	
"on signal level below threshold of signal in 3 ADC channel"	B	
"on signal level below threshold of signal in 4 ADC channel"	B	

Table 5-5. Acquisition stopping conditions

Acquisition stopping conditions	Implemented in version E20-10	Notes
Software asynchronous stopping	A, B	based on frame edges
On number *M* of recorded frames acquisition restartable (*see notes 1, 2*) under settled start conditions, for example, to implement start-stop acquisition mode	B	$0 \le M \le 16777215$, where, *M*-integral

Note1:

In FPGA firmware of version 2.00.03 (details on firmware versions see in p. **3.3.4**) for restarting under any start condition it is required to activate software restart on upper software level (i.e. single start on condition is executed in practice). In FPGA 2.00.05 firmware the additional program start is not required under additional startup condition "on transmission through given signal level in selected channel" and stopping condition "on number of M recorded frames", due completing of the next stopping condition fulfillment the additional data acquisition start will begin automatically upon completing of new start condition fulfillment (i.e. multiple start on condition in practice). For another start conditions FPGA 2.00.05 firmware is similar to 2.00.03 firmware.

Note 2:

In future FPGA firmwares it is technically possible to implement software control of single-multiple start modes (in the context of note 1) on any specific start condition upon stopping "on number *M* of recorded frames". Make an enquiry to **L-Card**, if such mode is required to solve Your problems.

Visual illustration of **E20-10** synchronization modes is given in diagrams **fig. 5-3.** Frame size equal to 4, interframe delay duration equal to 6 ADC conversion frequency periods are taken as an example on diagrams; frame is configurated on sequence sampling of all 4 channels. Under such configurations the data numeration frequency per ADC channel will make $\frac{1}{10}$ given ADC conversion frequency.

Common case **fig. 5-3**for applying all possible synchronization conditions (except "on level" synchronization conditions which are discussed individually) is shown on top diagram. In **E20-10** of revision A the software data acquisition start (or on START signal edge) was applied, and upon start data were certainly recorded in FIFO buffer until data acquisition software stopping from upper level was sent (despite of frame edges). In **E20-10** of revision B you may use the configurations on additional recording conditions on signal edge, for example, as shown in diagram, in ADC 3-rd channel. In this case, frames will not fall in FIFO buffer (and, thus, will not fall in USB) till given additional condition will be fulfilled. As soon as the condition is fulfilled in the current frame, the data begining from the next frame will be fed into the FIFO and can be rolled back via USB. Blockage of transmission of given amount of frames starting from acquisition can be settled in revision B individually or as the second additional condition.

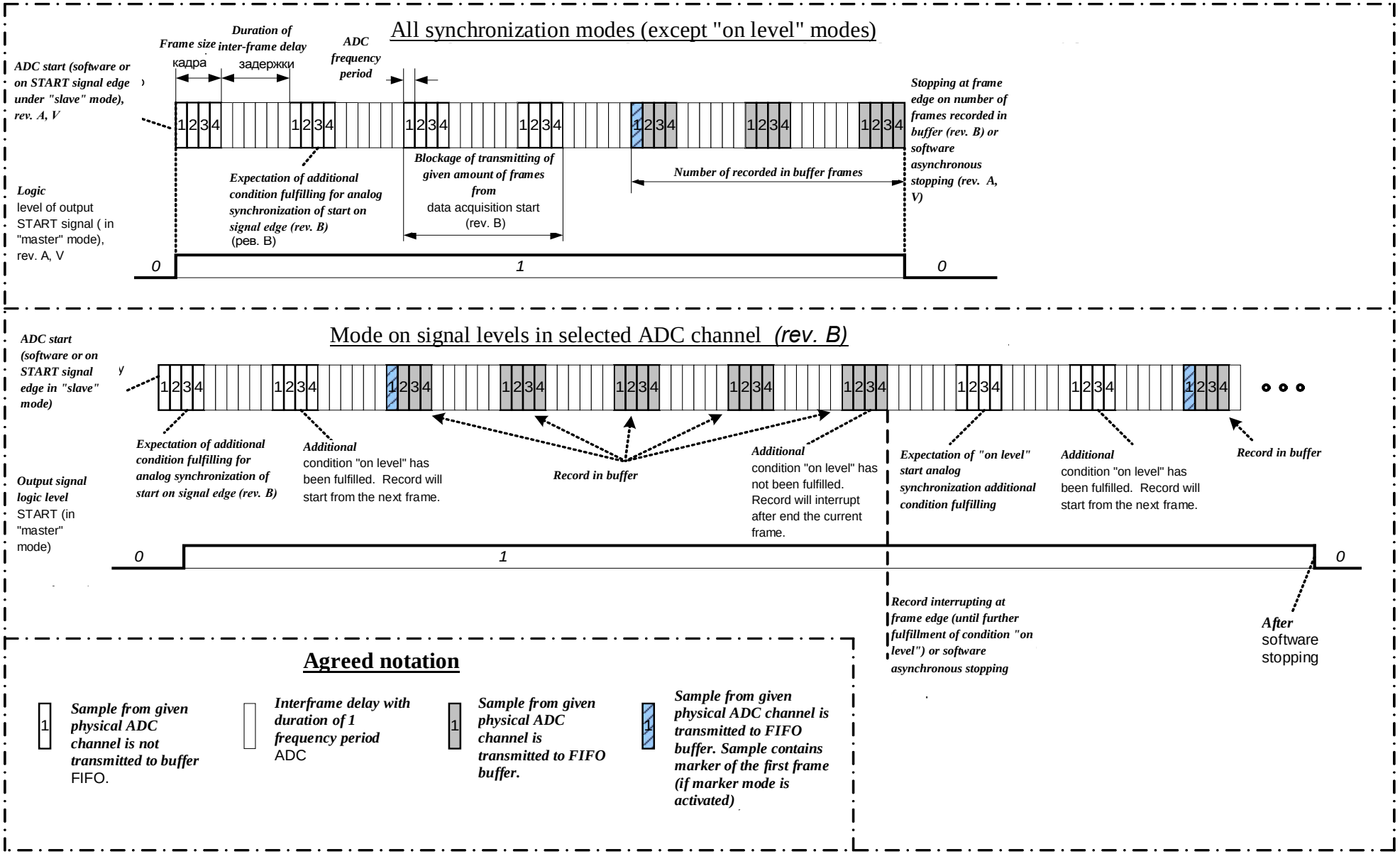
Stopping based on given amount of frames collection is provided in revision B except for asynchronous software acquisition stopping; furthermore, stopping edge will comply with end of last collected frame. In practice, this capability allows to carry out acquisition start-stop operation under preselected start mode (pay attention on notes to **table 5-5** on single and multiple start capabilities).

As it was mentioned in p. **5.2** and as shown in diagrams, START signal behavior does not depend on additional start conditions if it is configurated "on output ("slave").

Data acquisition on signal level synchronization mode (above or below given threshold) in selected (on diagram - on 3-rd) physical ADC channel is shown on bottom diagram (**fig. 5-3**) (in

rev. B only). Based on **fig. 5-2**, comparing threshold value will be performed with calibrated sample value, because data calibration logic in **E20-10** ***rev. B*** is upstream of logic of permission for recording in FIFO buffer. Logic of this synchronization mode is based on logic of permission for data recording in FIFO buffer, in addition, ADC functional node (in combination with control list logic) is started in advance and ADc sample values analysis from the relevant physical channel of **E20-10** hardware is performed prior data recording in FIFO buffer. *E20-10 will stay in waiting condition until preset recording condition are not fulfilled* (**table 5-4)**. Upon fulfilling of recording condition in current frame *FIFO buffer* will begin to fill up until recording condition "on level" are being fulfilled. In condition default the record will be stopped until condition "on level" will be fulfilled again or until software stopping command will be sent. Thereby, signal areas being selected on level on selected number of synchronizing channel and data from other physical channels written in frame will occur in FIFO buffer under "on level" synchronization mode. Thereof, all these data can be rolled back to computer due to their entering to FIFO buffer **E20-10** .

When synchronizing "on level" analog signal in **E20-10** ***rev. B*** for software recognition of data continuity edges the marking mechanism has been introduced for the first sample of data continuous area obtaining from **E20-10 (fig. 5-2).** If marker mode is activated, that logic artifact providing to differ beginning of next data continuous area on upper software level is inserted in the first sample of each data continuous area. Way of viewing marker in the data format of **E20-10** ***rev. B*** is explained in p. **5.2.3**.



Record in buffer Record in buffer. Fig. 5-3. Synchronization mode diagrams

5.2.3. Data format of **E20-10**

Data format from **E20-10** in normal mode (by default) is 16-bit signed integers (in radix complement) within the range of from -8192 to +8191. This means, that 14 low bits are information ones and 2 high bits contain extended sign of radix complement. Binary the data looks like (15-th bit is shown left, 0-th bit - right)[14]:

sssXXXXXXXXXXXXX,

where, s – extended sign of radix complement, X – code positions

Lack of information content of two code high bits provides their value manipulation in specific cases described in pp. **5.2.3.1**, **5.2.3.2**.

5.2.3.1. Coding of word size overloading sign **E20-10** or revision A

In **E20-10** of revision A the following coding of word size overloading sign is applied (if the relevant mode is activated): when no overloading, that data are transmitted unchanged, when overloading – the data are transmitted with inverted 14-th data bit **š**:

sšsXXXXXXXXXXXXX,

Based on radix complement representation of a number features, such inversion of 14-th bit, in any way, will be cause of resulting value of 16-bit code over the range of -8192…+8191, – this is software detectable sign of overloading.

In **E20-10** of revision B the word size overloading sign is not inserted in data format (p. **5.2.6**).

5.2.3.2. Coding of data continuous area start in **E20-10** of revision B

In **E20-10** of revision B the data continuous area beginning marker is applied which is coded by inserting value "01" in field of positions <15..14>, if marker mode is activated:

01sXXXXXXXXXXXXX,

Such representation of marker gives simple criteria of its software detecting - this is code value over 8191.

[14] In most programming languages, this format complies with "signed small integer".

5.2.4. FIFO buffer and its overloading elimination logic

E20-10 has on board 8 Mbyte memory where FIFO buffer is organized. Such depth of buffer is enough to, for example, compensate 400 ms of spooling delay via USB by operating system at maximum acquisition frequency of 10 MHz (with zero interframe delay). Experiments show, that this time interval is fair enough even in operation under Windows (under operating system of *un*real time) at average load of operating system with rest applications, in the absence of explicit computer resource exhaustion (see details in *Programmer's manual* [1]). Thereof, maximum spooling delay time will increase proportionally to decreasing of data transmission traffic in computer during data acquisition frequency decreasing and when setting to non-zero interframe delay. We referred in detail on buffer overflow situation processing inside **E20-10**.

In **E20-10** of revision A FIFO buffer overflow occurrence causes data acquisition stopping and upper-level program necessity to restart **E20-10**, that leads to time-consuming "freezing" of E20-10 out of data acquisition process. This problem has been strongly taken into account in **E20-10** of revision B. Here, the specific hardware logic for FIFO buffer overflow elimination against continuous acquisition has been entered. *Overflow elimination logic* will spool from FIFO data with volume multiple of minimum required one to eliminate FIFO overflow capability at the approach to edge of 8 megabit of data collected in FIFO. These emergency spooled data are thrown from data flow but, in principle, data acquisition without channel number accounting failure at upper level can be continued due to thrown data volume multiple always of frame size. So, in **E20-10** of revision B FIFO buffer overflow will always leads to unavoidable (in this case) data flow break but unlike revision A, you may not restart data acquisition **E20-10**.

It is noteworthy, that all revisions of E20-10 have upper software level tools to alarm FIFO overflow occurrence which indicate the user data flow from **E20-10** breakage (details see in *Programmer's manual* [1]).

5.2.5. Readings adjustment (calibration)

Module **E20-10** is delivered with calibrations recorded in **L-Card**. Relevant calibration factors (product serial number and other additional details as well) are recorded in Flash-memory of AVR controller.

Using calibration factors stored in Flash-memory of AVR controller you may account offset and scale errors (of gain factor) of analog path at each range.

In revision A of module **E20-10** *the data calibration procedure is implemented with upper level tools (in computer), and in revision B – with tools of* **E20-10** itself. Working with pure uncalibrated data in both revisions, on demand, the calibration mechanism may not be used, but you should take into account, that in this case dispersion in readings of different instances of modules **E20-10** can reach 5% of scale.

It also important to note, that in **E20-10** or revision B the linear calibration arithmetic – is integer of ADC data within the range –8192…8191. Calibration factors under calibrating of **E20-10** at manufacturer are set in such a way that extreme points of each ADC input subrange correspond to calibrated code values ±8000.

5.2.6. ADC word size overflow warning

ADC word size overflow signal is available at ADC chip output LTC2245, it is generated for each ADC sample and this signal is used in **E20-10** for this overflow warning . In overflow case ADC uncalibrated code takes one of extreme value -8192 or 8191 – depending on sign of input voltage supplied to ADC input.

It should be particularly emphasized that in **E20-10** not overflow alarm of ADC specified input subrange is captured but signal level alarm output over ADC specified subrange which resulting in incorrect presentation of this level by transmitter due to excessing conversion physical edges.

In **E20-10** of revision A when the relevant mode is selected, the ADC word size overflow alarm is mixed in 16-bit data format in such a way that under positive overflow the code rather more that 8191will be issued, and under negative overflow – much less than -8192. It is understood, that on upper level if You activate overflow alarm in software then You must use range -8192...8191 excessing events for overflow software warning and prior to process sampled signal in your program You must limit data range up to -8192...8191. If You apply calibration of ADC data at upper level og library function the abovementioned principle to select overflow alarm is not changed the only difference being linear data calibration function is applied for **E20-10** output data.

In *revision B the developers decided to abandon overflow alarm mixing in data flow and to perform channel-by-channel warning via control pipe channel of USB* interface and relevant library functions. Moreover, the procedure of software request on definite quantity of data from **E20-10** of revision B has been agreed with relevant software overflow presence bit in data quantity requested.

5.2.7. DAC optional

*Two-channel asynchronous **DAC*** (option) is controlled from AVR asynchronously only using *control pipe* of USB interface and by relevant function of upper level. This means, that DAC can be used for slow reproducing of constant voltages only under asynchronous control mode with mean time for response - tens milliseconds, depending on response current time of computer operating system.

6. Connection of signals

Signal assignments on **E20-10**connectors as well as signal maximum permissible characteristics and connecting ways are explained in this chapter.

6.1. General Information

The system user shall connect the signals and solder the connectors. Magnetic sweep cable for signal connectors (except cable BNC) are included in delivery package (p.**3.3**).

Installation of signal circuits with connection of signal sources, sensors, etc. to E20-10 module must be carried out by a qualified specialist.

User connecting resulting in exceeding of maximum permissible voltage and current values may cause **E20-10** parameters degradation or failure of **E20-10**, computer and other connected equipment. **L-Card will not be liable for damage caused by electrically improper signal connecting** .

For more details on way of signal connection to the measuring system and noise suppression, refer to specialized article titled: *Solutions of problems on electro-compatibility and interference protection during connecting of measuring equipment through the example of* **L-Card** L *company product.* [2]. References to articles on L.[**3**] connecting examples as well as on optimization of L.[4] connections are given in Chapter **Bibliography** of this manual on page **66**.

6.2. External connectors

This chapter describes in details connectors of **E20-10** from external connections point of view.

Voltage ranges given in tables in describing of signals made out to connector pins *are always specified in relation to AGND contact for analog signals and in relation to GND contact - for digital ones.*

E20-10 connectors packaging concept is as follows: analog signal connectors are in front, digital - at the rear.

6.3. Analog signal connectors

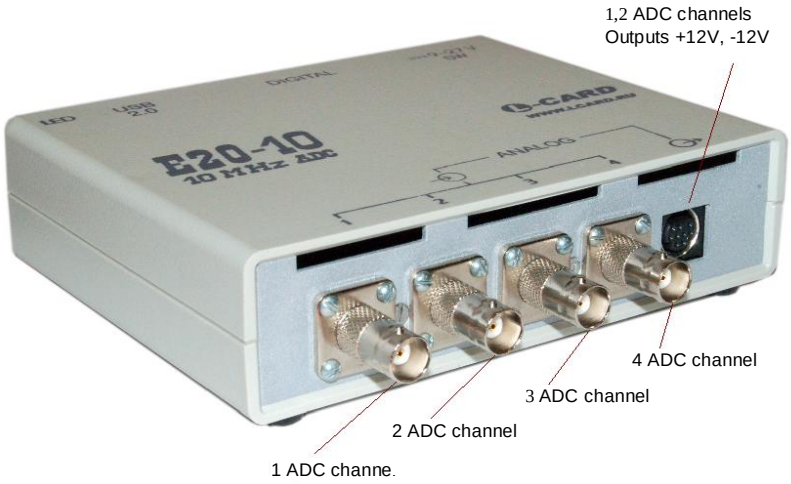


Fig. 6-1. Analog input connectors

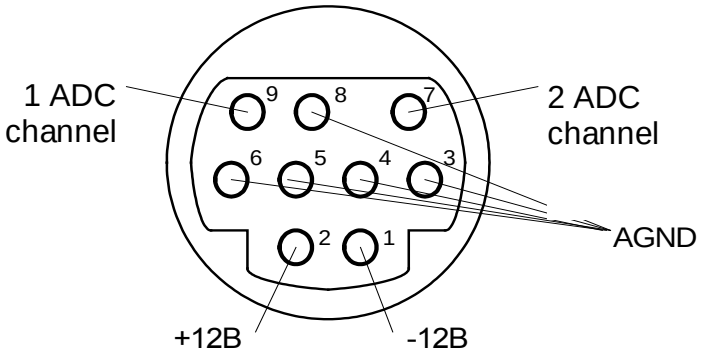


Fig. 6-2. Analog output connectors

The four analog inputs of **E20-10** module connectors type is -BNC plug in socket type with corresponding cable connector of BNC cable plug type. Channel matching is shown in **fig. 6-1**. The same matching is graphically shown on **E20-10** body.

Actually, in case of ac +12Vg of **E20-10**-12V ited (*but not recommended*!) to use domestic connector CP-50 instead of foreign-made BNC as a cable connector, but *in this*

case[15] possible difficulties can arise when connecting or disconnecting this connector with the plug in connector BNC on**E20-10** module.

Attention! Due to the non-conformity of domestic (made in Russia) connectors to the BNC standard, use of CP-50 connectors (cable parts or adapters) in some cases can cause a damage of plug in connectors BNC in **E20-10**.

Type of DAC analog output connectors and power outputs for **E20-10** — 9-contact socket MiniDIN. Contact assignment is shown in **fig. 6-2.** Relevant cable connector - is 9-contact cable plug MiniDIN.

Table. 6-1.On connectors analog signal assignment

Signal designation	Common point	Direction	Description
1 ADC channel	AGND	input	Single-phase (with common land) 1 ADC channel input, connector screen is connected with AGND
2 ADC channel	AGND	input	Single-phase (with common land) 2 ADC channel input, connector screen is connected with AGND
3 ADC channel	AGND	input	Single-phase (with common land) 3 ADC channel input, connector screen is connected with AGND
4 ADC channel	AGND	input	Single-phase (with common land) 4 ADC channel input, connector screen is connected with AGND
1 ADC channel	AGND	output	Single-phase (with common land) 1 ADC channel output
2 ADC channel	AGND	output	Single-phase (with common land) 2 ADC channel output
+12V, -12V	AGND	outputs	Bipolar (relative to AGND) external device power output
AGND	-	-	Analog land **E20-10**

[15] Historical roots of this problem belong to the non-conformity of metric standards of the former USSR to the western inch standards.

6.3.1. Digital signal and external power connectors

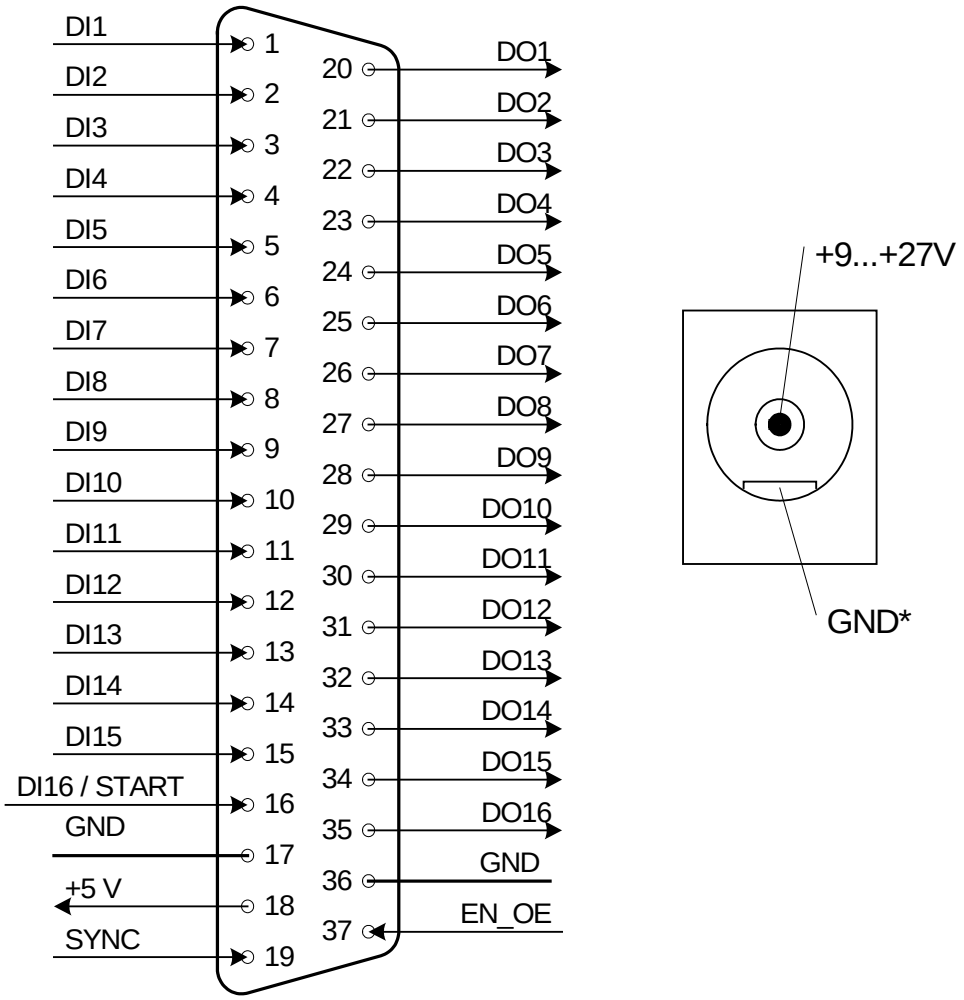


Fig. 6-3. Digital signal and external power connectors

Type of digital input-output signal connectors in **E20-10**: DRB-37F, relevant cable part of connector — DB-37M.

Attention! Metal edging (body) of cable connector DB-37M shall not be connected with any circuit.

External power connector type: DJK-02A, cable part relevant to it — DJK-10A.

Table 6-2. Connector DIGITAL I/O signals

Desig-nation of	Common point	Direc-tion	State after connection	Description
DI<16...1>	GND	Input		16-bit digital input: DI1-low bit, DI16-high bit, START and DI16 lines are combined
DO<16...1>	GND	Output	Z-state	16-bit digital output: DO16 – high bit, DO1 – low bit
GND	-	-	-	Digital land
+5V	GND	Output	+4.75...+5.0 V	Power output +5V of external circuits. see p. **6.4.5**
SYNC	GND	Input-output		Input-output of ADC synchronization signal (pull-up resistor is not available)
START	GND	Input-output		Input-output of data acquisition start signal, START and DI16 lines are combined. Pull-up resistor of 4.7 kOhm to circuit of +5 V
+9...+27 V	GND*	Input		Voltage input of +9...+27 V from external power supply source of 5W. On circuit GND* see in p. **6.5.3**
EN_OE	GND	Input		Control input for DO<16...1> line forced setting mode to active output upon module power feeding completion, in this case, software control function is ignored with output enable. To active the mode it is required to close circuits EN_OE and GND on cable part of digital signal connectors. If EN_OE input is unconnected the output enable software control mode is activated.

6.4. Characteristics of signal line inputs and outputs

Attention!: Prior to connect **E20-10** module to your system, it is required to strictly observe the parameters specified in tables of this section.

The manufacturer shall not be liable for E20-10 failure caused by violation of maximum permissible operation conditions.

The following symbols are given in tables of this section:

AI- analog input

DI – digital input

DOZ - Z-state transferability digital output

DIO - digital I-O

AIO - analog I-O

6.4.1. Operating mode

Module **E20-10** has the following input and output signal line characteristics.

Table 6-3. Characteristics of signal lines inputs and outputs, operating mode

Signal	Type	Input resistance	Maximum permissible conditions at input	Maximum permissible conditions at output	Pull-up resistor
Inputs of channels	AI	min. 5 MOhm (rev. A) 10 MOhm (rev.	±10 V		
DAC channel outputs	AO			Output short circuit may occur against AGND	
INT, DI1... DI15	DI	4.7 kOhm	-0.2V...+5.2V relative to GND		4.7 kOhm relative to +5V
DI16/ START	DIO	4.7 kOhm if configured for input	-0.2V...+5.2V relative to GND		4.7 kOhm relative to +5V
DO1... DO16	DOZ	—	—	±20 mA	—
SYNC	DIO	Min. 100 kOhm if configured for input	-0.2...+5.2 V relative to GND	±20 mA if configured for output	

Attention: It is not recommended to unload **E20-10** more than 0,7...1 W total power on all output circuits **E20-10** .

6.4.2. Power-off mode

Module **E20-10** switched off the external power supply source has the following input and output signal line characteristics:

Table 6-4. Characteristics of signal lines inputs and outputs, off mode

Signal	Type	Input resistance	Maximum permissible voltage at input	Maximum permissible conditions at output
ADC channel inputs	AI	min. 1 kOhm	±10 V	—
DAC channel outputs	AO	—	—	—
DI1...DI15	DI	min. 600 Ohm	-0.2...+5.2 V relative to GND	—
DI16/START	DIO	min. 600 Ohm	-0.2...+5.2 V relative to GND	-0.2...+5.2 V relative to GND
DO<1...16>	DOZ			-0.2...+5.2 V relative to GND
SYNC	DIO	min. 600 Ohm	-0.2...+5.2 V relative to GND	

6.4.3. Limiting through currents

Inside **E20-10** circuits AGND, GND, GND*, presenting on module connectors are interlinked (p. **6.5.3)**. This places certain restrictions on maximum permissible through currents through circuits AGND-GND-GND*.

Attention! Maximum permissible through currents exceeding can cause **E20-10**failure.

Table6-5. Maximum permissible through currents

Circuit	Maximum allowable output current
AGND-GND	0.1 A
AGND-GND*	0.1 A
GND-GND*	0.7 A

6.4.4. External power supply input characteristic

When **E20-10** is energized not from AD adapter including in delivery package (p. **3.3.1**) and from external direct current source the following parameters shall be taken into account:

Table 6-6. External power supply input characteristics

Parameter	Value	
	Rev. "A", "B"	**Rev. B.01**
Operating voltage range	+9.0…+27 V (engagement threshold +9,5 V)	+8.0…+40 V
Maximum permissible voltage	−30…+30 V	−45…+45 V
Power input under operating mode with off-load output circuits **E20-10**.	max. 5 W (rev. A) min 4.5 W (rev. B)	max. 4.5 W

6.4.5. External power supply outputs characteristic

When collecting currents from **E20-10** to power external devices it is required to take into account external power output characteristics.

Table 6-7. External power supply outputs characteristic

External circuit power supply source	**±12V**	**+5V**
Maximum output current	2 x 35 mA	35 mA **100 mA for E20-10 of revision B.01**
Current protection	stabilizer thermal protection	stabilizer thermal protection

Attention! It is not recommended to unload **E20-10** more than 0,7...1 W total power on all output circuits **E20-10** .

6.5. Specification and connection examples

This chapter contains certain major features for external circuits connecting to module **E20-10**.

6.5.1. Connections to USB

The following features shall be taken into account:

- Speed of 20 MB/s (corresponds to data acquisition frequency of 10 MHz at zero interframe delay) is close to maximum operational speed *high-speed* USB 2.0 interface. In particular, it means, that both **E20-10** connected to one USB-hub (or one USB-controller of the computer) can operate up to 10 MB/s each only.
- On the one hand, modern USB3.0 – hubs shall provide speed of 20 MB/s for each downstream port, on the other hand, hub's manufacturers are not obliged to provide such speed and in the pursuit of the product cheapening the versions [16]…are possible.
- Under combined connecting *high-speed* and *full-speed* USB devices to the same USB-hub the speed of USB will be set based on the slowest device, i.e. *full-speed* only.
- At speed *full-speed* (USB 1.1) the maximum achievable speed of data transmission **E20-10** — 1 MB/s (ADC 500 kHz), it can be set via corresponding setting of interframe delay. At higher frequencies FIFO buffer of **E20-10**will be overflowed, because USB *full-speed* bandwidth capacity will not provide the required speed of spooling from **E20-10** (buffer overflow will lead to data loss but not to service outage of E20-10).
- When several **E20-10** are used at speed of more than 10 MB/s it is recommended to connect them to *computer different controllers* – in this case, there should be no bandwidth capacity problems (otherwise, internal USB-hub on mother card will not provide 20 MB/s for each port). If required, you can use additional PCI or PCI Express expansion cards for USB-ports in auxiliary USB-controllers on the basis: 1 card for 1 module E20-10 (the required speed will be practically provided via USB).
- It should be noted, that when using several modules E20-10 at maximum speed with one computer there are objective physical limits for: - physical recording speed on hard disk (if your software uses such recording); - chipset operation speed via computer RAM, because data transmission from E20-10 to computer RAM is via DMA (i.e. with computer processor partial involvement); - computing load with exterior tasks actively working with RAM.
- Maximum length of USB cable according to standard - 5 m.

Attention! To avoid **E20-10** failures (particularly, at high operation speeds) it is highly recommended not to use the computer remote USB expansion ports to connect **E20-10** (these are the ports that use pin double-row connectors [17] on mother cards with extension cables and additional USB connectors, which are usually located either at the rear of the system block on additional bars or moved forward of the computer case) due to the lack of quality of these connections for a high-speed device like **E20-10** on several important

[16] L-Card can not warrant third-party product quality; prior to buy the selected hub it is necessary to be clear maximum speeds on downstream-ports.

[17] in general, such USB connector is not even specified in USB specifications 1.1, 2.0 and 3.0 [10] [11]

characteristics: unshielded connector on mother card, partially or fully unshielded cable from this connector, improper cable shield connection and remote connector.

6.5.2. Multimodule connections

You must keep the following rules in multimodule configurations with **E20-10**:

If modules are interconnected via digital lines (including via synchronization and interrupt lines) then modules GND lines shall be interconnected as well.

If different modules are conductively coupled via any circuits but they use different PC or different USB-hubs from individual power sources, then these PC or USB-hubs shall have common ground (if ground circuit is provided) and modules GND circuits shall be interconnected.

When interconnecting of bidirectional lines of different modules the inconsistent state *output to output* which can lead to lines overflow **E20-10**should be negated.

The modules connecting to USB issues are described in **6.5.1**. For information on proper use of GND, GND* and AGND circuits when connecting the devices, please, refer to **6.5.3**.

Higher levels of through currents are potential in multimodule connections E20-10 (pp.**6.5.3, 6.5.4.4**-**6.5.4.6**). Penetration methods: proper grounding, in-phase filters (specific recommendation providing detailed description of connecting case are given - on demand in L-CARD).

6.5.3. Circuits GND, GND* and AGND

Connecting external circuits of module **E20-10** shall be performed based on its internal connecting diagram for common wires from different connectors – **Fig. 6-4.**

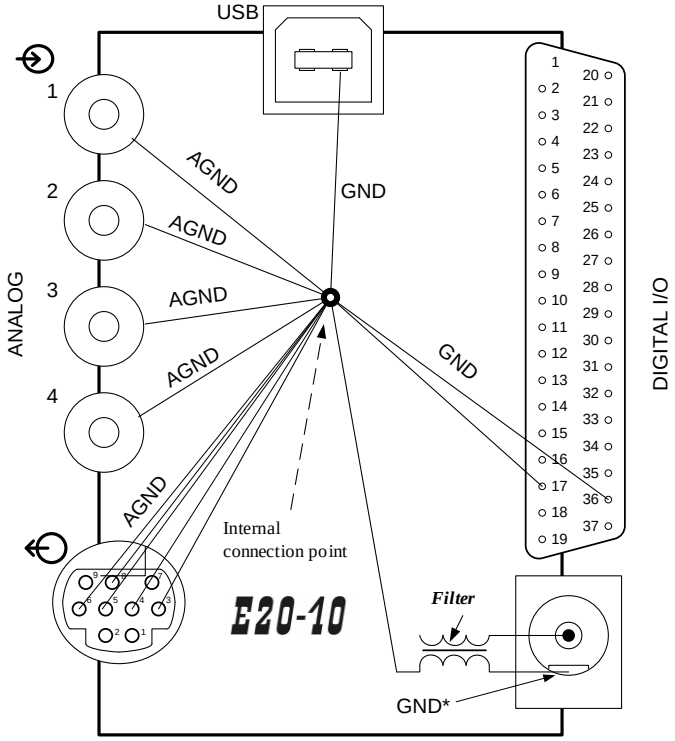


Fig. 6-4. Circuits GND, GND* and AGND

Module **E20-10** has no internal galvanic separations, hence, GND, GND* and AGND circuits have internal coupling (p. **6.5.3**): common wire of digital circuits GND in one point inside **E20-10** is connected to common wire of analog circuits AGND. **External power source common wire** is connected to the same *internal point* E20-10 via in-phase EMC filter.

On principle, that common wire of USB interface from computer (connected to computer case) is connected to common wires connection point inside of **E20-10.**

When connecting **E20-10** to external circuits you should remember, that the most proper connecting of **E20-10** is that connecting which would not result in through currents passage via circuits: **GND—AGND, GND—computer case or AGND—GND—computer case.**

Attention! Presence of abovementioned through currents can degrade signal-noise rate in **E20-10** channels, cause unsteady operation of USB or USB-hub, and when exceeding of maximum permissible through currents(**table 6-5**) **E20-10** and connected equipment failure.

If such currents are unavoidable on any case in your system it is required to take measures to minimisation them (pp.**6.5.4.5**, **6.5.4.6**).

General recommendation on instruments connecting are given in special article [2].

6.5.4. ADC input connecting

Some nitty-gritty issues on ADC input connecting are described herein.

6.5.4.1. Intrinsic input current of ADC analog input

This current was amplifier component property applied in revision A. Amplifier with incomparably lower input current (about 10 nA) may be applied in revision B. But, due to the fact of input current existence of revision A could be used in different propositions (for example, as signal external source connecting sign), that in revision B the negative offset current can be live on command (therewith, offset current is generated artificially) to be compatible with old revision, but input offset current is dead *by default in revision B*, see **fig. 6-5**.

ADC input intrinsic current of **E20-10** of revision A has negative sign, so,**when unconnected analog input of E20-10 the overswing to negative values side will be appeared**. This, on the one hand, leads to determinacy of unconnected analog input state, one the other hand, places restrictions on signal internal resistance on direct current, because intrinsic input current value multiplied by internal resistance of signal source (via direct current) will supply constant voltage of input offset signal of **E20-10**. For example, if source resistance is of 50 Ohm typical offset voltage will make 0.35 mV, and if 1 kOhm — 7 mV.

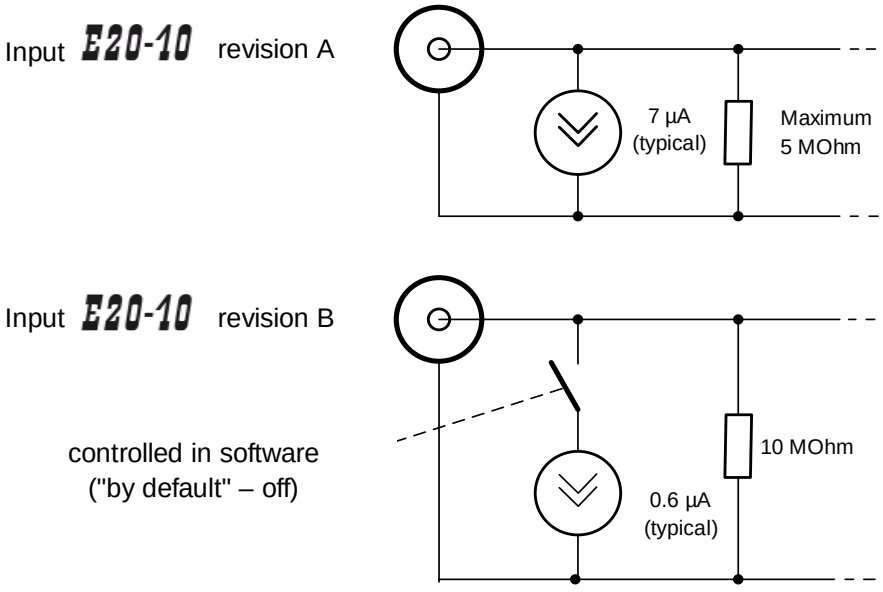


Fig. 6-5. Equivalent circuits of ADC input circuit via constant current (differences in revisions A and B)

6.5.4.2. Connecting to high-resistance output and alternate current output

For* E20-10 *of revision A, if your signal source outputs is alternate current output containing series coupling capacitor (i.e. on direct current – disconnection or resistance of more than 10 kOhm), then when connecting to such output it is required to connect additionally parallel resistor (max. 1 kOhm preferably) to signal source output[18]. This resistor generates the required

[18] Of course, such resistor connectivity depends on type and output capability of signal source

source resistance on direct current and minimizes input current effect (p. **6.5.4.1**) on ADC input zero offset voltage. We can state, that: ADC input of **E20-10** ***of revision A is incompatible with signal source with resistance of more than 10 kOhm on direct current.***

For **E20-10** ***of revision*** B under same case the minimization of input offset voltage for ADC input can be achieved by software disconnecting of offset input current and, in this case, conceptual restrictions of revision A are ended.

Please note, that in all revisions of **E20-10** it will be preferable to have signal source low resistance to optimize signal-to-noise ratio

6.5.4.3. On standard feeler oscillographic gauge connectivity

ADC input BNC connectors of **E20-10** suggest the users on standard feeler gauge connectivity to divider 1:1/1:10 rated at oscillograph input resistance of 1 MOhm and input capacitance of 15-30 pF. It should be noted, that such gauge on direct current under mode **1:10** in relation to ADC input is equivalent to high-resistance signal source (more than 10 kOhm) and with **E20-10** of revision A such *gauge under mode of 1:10 is incompatible with* ***E20-10*** *revision A* (p. **6.5.4.2**), but compatible with **E20-10** or revision B, if input current will be off in software (input current is disconnected "by default" in revision B). It is required to match the gauge. Consider these issues in details.

Standard feeler oscillographic gauge is, generally, rated at oscillograph input resistance of 1 MOhm. Under mode of 1:10 the device input resistance serves as gauge voltage divider "lower arm" of 1:10, while the gauge transfer impedance (about 9 MOhm) serves as divider "upper arm". *So, to provide dividing function 1:10 if oscillograph gauge it is required to have connecting in parallel to input E20-10 of resistor of 1.1 MOhm*. This resistor connected in parallel to input resistance E20-10 will provide required 1 MOhm cumulatively for standard feeler oscillographic gauge load.

We can assume**,** that in mode 1: 1 the standard gauge of the oscilloscope is rather well matched in frequency band up to 5 MHz with ADV input of **E20-10** of any revision, since in 1: 1 DC mode the through resistance of the gauge is not too high, and the inconsistency in alternating current affects the higher frequencies that do not fall within the bandwidth of the ADC input. In this case, input current curtailability in **E20-10** of revision B provides the gauge connectivity 1: 1 to high-impedance signal sources, as in the case of a conventional oscilloscope.

Gauge accurate matching across the alternating current in 1:10 mode can be performed with operating tuning condenser located on the gauge BNC connector, if, of course, your gauge has such a tuning.

The parallel connection to E20-10 input of a 1.1 MΩ resistor, as was recommended above, can technically be done by switching the oscilloscope gauge via BNC load adapter [19].

6.5.4.4. On effect of through currents on signal-to-noise ratio

ADC input of **E20-10** has bipolar, single-phase voltage input without galvanic isolation (see input types classification in 2).

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[19] This adapter is not delivered by L-card. When necessary L-Card is ready to consider the possibility of E20-10 modification release with input resistance of 1 MΩ. If you are interested in such E20-10 modification, please contact the L-Card office or the conference at www.lcard.ru

If you intend to achieve the best signal-to-noise ratio when connecting ADC single-phase input of **E20-10** to an external device (signal source), you must provide zero current (across the frequency bandwidth) passing along the screen of the coaxial cable of ADC input circuit, because, voltage loss on through impedance of the cable screen circuit is largely summed with the voltage of the useful signal at ADC input, that leads to a deterioration in the signal-to-noise ratio.

6.5.4.5. How can you find out that the through-currents degrade the signal-to-noise ratio in your connection diagram?

Let us say, You have connected ADC input of **E20-10** to external device and have found disturbances absent at external device output within digitalized signal spectrum. Root cause location:

- Disconnect coaxial cable connector from device (second cable end is connected to **E20-10**) and close central contact of disconnected connector to its housing. If disturbance in digitalized signal has disappeared this means that it is generated not in **E20-10** and not in cable as a result of its failure.
- Having connector central contact closed connect connector housing to device output connector housing. If disturbance is present, this means, that it has been generated due to through currents. If disturbance is absent, this means, that there is disturbance at device output signal itself.

6.5.4.6. How to solve the problem if the through currents are detected?

The following technical ways of solution will help you:

- *Ground the connected devices electrically close* , shorten connecting wires.
- Use galvanic isolation auxiliary equipment in system which break through current circuits on common wires.
- Connect signal to ADC output of **E20-10** via external in-phase filter [20]which will compensate alternate through current and disturbance will be absent in the signal.

6.5.4.7. On disconnected ADC inputs

Attention! Disconnected inputs are recommended to be set in intrinsic zero measurement mode or they are not required to be sampled.

ADC input intrinsic current (except of **E20-10** of revision B with input current disconnected in software) on ADC disconnected inputs can generate input voltage exceeding input signal specified subrange. Wherever sample the corresponding channel under input overload mode during data acquisition, then it can cause interchannel passing moderate increase . So, disconnected input should either be set in intrinsic zero measurement during normal operation - overload will be eliminated, or be unsampled (i.e. channel code corresponding to disconnected input shall be absent in control list).

6.5.1. Digital lines and synchronization lines connecting

All digital lines of **E20-10 (fig. 6-3)** have GND common wire circuit above which the connections with external digital nodes should be performed. GND circuit external connecting should always base on its internal connecting (p.**6.5.3**)

[20] To have technical help on technical details on such filter structure depending on signal source type, please, contact ***L-Card***

To implement "master-slaves" connection diagram the near located from 2- to 5- pcs. **E20-10** can be connected with twisted pairs by shortest path. Similar circuits of all **E20-10** are required to be connected implicitly (**fig. 6-3)**: GND–GND, SYNC–SYNC, START–START. When connections performing with twisted pairs one of the wire in pair should always be a GND circuit.

Connections optimal topology with short twisted pairs - is when two twisted pairs per each "slave" go separate ways from "master" according to radial principle in shortest path, and non optimal - is a sequential traversal topology. The compromise between the first and the second variant is appropriate in practice. Short twisted pairs can be replaced with short screened wire bridles (GND-screen).

The case of short connections of near located **E20-10** has been described above, but there is a technical possibility to significantly increase the length of connections and the number of synchronized **E20-10**. If you retransmit START and SYNC signals many times using transmitter microcircuit from master **E20-10** (connector power + 5V) then the number of **E20-10** connected according to "master-slaves" is unlimited technically! One of the examples of such connecting based on MLVDS technology is described in L.[**3**] , see page. **66**.

7. Specifications

All **E20-10** characteristics given below correspond to computer standard *USB 2.0* port connecting.

The following specifications indicate the main parameters of **E20-10** for its intended operating mode.

Attention! E20-10 module performance limits as well as signal line additional features are given in p. **6.4**.

7.1. ADC

Specification	Value
Number of channels	4 with "common ground" (single - phase)
ADC bit depth	14 bits
Sub-ranges of input signal	±3 V; ±1 V; ±0,3 V – independent programmable setting per channel
Limits of DC voltage maximum permissible reduced fundamental error of measurement	±0.25 %
Limits of the permissible relative basic error of measuring the AC voltage	According to p. **7.1.1**, **7.1.2**
Limits of the permissible relative fundamental error of the ADC conversion frequency	±0.005 %
Typical **signal-to-noise ratio**	70 dB (for **E20-10** of revision A) 73 dB (for**E20-10** of revision B)
Limits of maximum permissible complementary error against changes in ambient temperature within operational temperature range, per 10 ºC	0,5 against maximum permissible fundamental error limits
Maximum ADC conversion frequency	10.0
Minimum ADC conversion frequency	1.00 MHz (lower data acquisition frequencies are permissible using interframe delay internal mechanism implementing data reduction)

Zero offset when ADC input is unconnected	Less than 1 mV (typically) for E20-10 of rev. V
ADC samples frame parameters: – Frame size – ADC channels frame inside sampling sequence	 From 1 to 8192 ADC frames (in firmware 2.00.07 or older, see p. **3.3.4**) arbitrary (programmable)
Interframe delay time for **E20-10** of revision A for **E20-10** of revision B	programmable: 0-255 ADC conversion frequency periods 0-65535 ADC conversion frequency periods
Minimum data acquisition rate at maximum interframe delay and ADC conversion frequency of 1 MHz	7.8 kbyte/s (for **E20-10** of revision A) 30 byte/s (for **E20-10** of revision B)
Maximum data acquisition rate at zero interframe delay and ADC conversion frequency of 10 MHz	20 byte/s
ADC conversion frequency spectrum in internal synchronization	F_{ADC} = 30/k [MHz], where, k = {3, 4, 5, ..., 30}
ADC analog input DC input resistance	Minimum 5 MOhm (for **E20-10** of revision A) 10±0.5 MOhm (for**E20-10** of revision B)
Intrinsic input current of analog input: for **E20-10** of revision A for **E20-10** of revision B	 -15...0 µA (typical value -7 µA) 10 nA (typical value)
Typical value of conversion path upper passband frequency on level of -3 dB: **E20-10**, **E20-10-D, E20-10-D-I** **E20-10-1**, **E20-10-D-1, E20-10-D-1-I**	 1.2 MHz 4.5 MHz (on subrange ±3 V) 5.2 MHz (on subrange ±1 V) 3.5 MHz (on subrange ±0.3 V)
Inter-channel passage for **E20-10** of revision A, max.: - at constant voltage - at frequency of 1 kHz - at frequency of 1 MHz for **E20-10** of revision B, min.: - at constant voltage - at frequency of 1 kHz - at frequency of 1 MHz	 -50 dB -70 dB -60 dB -70 dB -75 dB -65 dB
Resistance to overloads by input measuring signal of DC voltage	±10 V (p. **6.4)**
Data correctability (calibration using factory calibration factors)	Yes (for **E20-10** of revision A – by software, in computer, for **E20-10** of revision B – by hardware **E20-10**) (p. **5.2.5**)

7.1.1. E20-10, E20-10-I, E20-10-D-I: limits of the permissible relative basic error of measuring the ac voltage

Frequency range of input signal, kHz	Limits of the permissible relative basic error of measuring the AC voltage, %
from 0.01 to 20 incl.	$\pm[0{,}2 + 0{,}02 \times (\frac{X_{AC}}{X} - 1)]$
more than 20 to 300 incl.	$\pm[2 + 0{,}03 \times (\frac{X_{AC}}{X} - 1)]$
more than 300 to 500 incl.	$\pm[3 + 0{,}05 \times (\frac{X_{AC}}{X} - 1)]$
more than 500 to 1000	$\pm[15 + 0{,}1 \times (\frac{X_{AC}}{X} - 1)]$

Notes

1 AC voltage measurement error is subject to limitation for signals peak values of which do not exceed measurement subrange specified value.

2 X_{AC} - is the AC voltage measurement limit, $X_{AC} = \frac{X_K}{\sqrt{2}}$ where X_K is the value of the specified voltage subrange.

3 X - is the value of the measured voltage.

7.1.2. E20-10-1, E20-10-1-I, E20-10-D-1-I: limits of the permissible relative basic error of measuring the ac voltage

Frequency range of input signal, kHz	Limits of the permissible relative basic error of measuring the AC voltage, %
from 0.01 to 20 incl.	$\pm[0{,}2 + 0{,}02 \times (\frac{X_{AC}}{X} - 1)]$
more than 20 to 300 incl.	$\pm[2 + 0{,}03 \times (\frac{X_{AC}}{X} - 1)]$
more than 300 to 1000 incl.	$\pm[3 + 0{,}05 \times (\frac{X_{AC}}{X} - 1)]$
more than 1000 to 2000 incl.	$\pm[5 + 0{,}1 \times (\frac{X_{AC}}{X} - 1)]$
more than 2000 to 4900	$\pm[30 + 0{,}3 \times (\frac{X_{AC}}{X} - 1)]$

Notes

1 AC voltage measurement error is subject to limitation for signals peak values of which do not exceed measurement subrange specified value.

2 AC voltage measurement error within input signal frequency ranges exceeding 1000 kHz is subject to limitation for measurement range of 1 V only under transmitters single-channel operational mode.

3 X_{AC} - is the AC voltage measurement limit, $X_{AC} = \frac{X_K}{\sqrt{2}}$ where X_K - is the value of the set voltage subrange.

4 X is the value of the measured voltage.

7.1.3. ADc synchronization system

Parameter, characteristics	Value
Parameters of SYNC external signal under ADC conversion frequency external synchronization.	Input TTL-signal with period of 100 – 1000 ns, on-off time of 1,90...2,10, with front/fall time of max. 5 ns.
ADC synchronization signal parameters: Propagation delay time in output: – START signal, max. – SYNC signal, max.	 One period of ADC start frequency 20 ns
Propagation delay time from output – START signal, max. – SYNC signal, max.	 One period of ADC start frequency 20 ns
Synchronization signal delay time dispersion in different modules **E20-10***:* – SYNC signals – START signals	 ±8 ns ±one period of ADC start frequency
START external signal duration, min.	50 ns

7.2. DAC

Parameter, characteristics	Value
Number of channels	2
Bit depth	12 bits
Settling time[21]	8 µs
DC voltage reproducing range	±5 V
Limits of the allowed reduced basic error of reproducing DC voltage	±0,3 %
Output current	2 mA
Limits of maximum permissible complementary error against changes in ambient temperature within operational temperature range, per 10 ºC	0,5 against maximum permissible fundamental error limits
Output resistance to sustained short circuit	Yes
Operational mode	Asynchronous

[21] This is output signal settling time for DAC used microcircuit without regard for much longer expected time of DAC control software-based asynchronous delay (p.**5.2.7**).

7.3. Digital lines

Parameter, characteristics	Value
Digital lines quantity - general purpose input - general purpose output - data acquisition start synchronization inputs - ADC start synchronization inputs	 16 16 1 (digital input one line alternative function)
Output current: - Digital line operational output current – Total load output current relatively to connected GND circuit, outputs being in logical item state	 Max. 8 mA (limiting current see p. **6.4**) max. 40 mA
Output logic levels	 0...+0.4 V ("logical zero") Min. 2.4 V ("logical unit"). (comply with series 74HCT, TTL/CMOS 5 V)
Input logic levels	-0.2...+0.6 V ("logical zero") +2.4...+5.0 V ("logical unit"). (comply with series 74HCT)

Attention! Digital lines performance limits see p.**6.4**

7.4. Power

This appendix contains power input-output characteristics for **E20-10** (see also p. **6.4.4**)

Parameter	Value
E20-10 power supply external source input parameters	
Operational voltage:	
– for **E20-10** of revisions A and B	+9.0...+27 V (when initiation voltage shall be within the range of +9.5…+27 V, operational capability upon actuation is within the range of +9.0...+27 V)
– for E20-10 of revision B.01	**+8.0...+40 V**
Power input (during operational voltage supplying, with off-load output circuits of **E20-10**):	
– for **E20-10** of revision A	to 5 W
– for **E20-10** of revisions B and B.01	to 4.5 W
Galvanic isolation from other circuits of **E20-10**	No
Input in-phase interference filter	Yes
Stability under power voltage negative polarity erroneous connection mode [22]	Provided
External devices power output +5V parameters:	
– output voltage	+5 V (+5% −10%)
– output current	35 mA (**100 mA for E20-10 of revision B.01**)
- current protection type	voltage stabilizer thermal protection [23]
Parameters of power output ±12V **of external devices E20-10**	
– output voltage	±12 V ±5%
– output current	35 mA
- current protection type	voltage stabilizer thermal protection

[22] actual situation: sometimes third-party supplies have network cards with power negative pole at connector central contact; in cross-connection of such card to **E20-10** the module will be operating but it will not operate from such card

[23] under thermal protection actuating **E20-10** normal operation is not provided

7.5. Physical properties

Parameter	Value
Body dimensions (without connectors projected parts)	142×132×40 mm
Weight	Max. 0.3 kg
Connector type *Digital I/O*	DB-37F
Connector type *USB*	DUSB-BRA42-T11
Analog output connector type Analog input connector types	MDNR-9J BNC – female chassis jack plug
Power connector type	DJK-02A
Mean time between failures	Min. 40000 hours
Service life	10 years

7.6. Operation conditions

7.6.1. Normal conditions

Parameter	Value
Normal operating conditions: – environment temperature, °C – relative humidity, % – air-pressure, kPa	 20±5 from 30 to 80 from 84 to 106

7.6.2. Operating conditions

Parameter	Value
For stability under climatic influences, the converters, in addition to the versions with the letter index I, correspond to GOST 22261, group 3 with an extended range of operating temperatures: – environment temperature, °C – relative humidity at an ambient temperature of 25 °C, % – air-pressure, kPa	 from +5 to +55 up to 90 from 70 to 106.7
For stability under climatic influences, converters of designs with the letter index I correspond to GOST 22261, group 4 with an extended range of operating temperatures: – environment temperature, °C – relative humidity at ambient temperature of 30 °C, % – air-pressure, kPa	 from -40 to +60 up to 90 from 60 to 106.7

8. Problems solution under abnormal situations

This Appendix attempts to classify possible abnormal situations which can occur in real practice and provides troubleshooting recommendations to the user.

External appearance of abnormal	Possible reasons	Troubleshooting measures
Computer operating system records unexpected disappearance of connection via USB interface during the operation. Indicator is yellow for a short time or constantly or blinks	1) Connection with USB cable is lost or USB cable is defective 2) Through currents via common wires connected to **E20-10** devices in your circuit are so high, that it will lead to USB interface unsteady operation.	Recover the contact, replace the cable Start with detecting through current flow circuit in your connection diagram. To this effect you should disconnect in series signal source and load connectors (except power input and USB) and, if upon next disconnecting USB interface operates steady, it means, that you have fount external device generating circuit of high through current flow via USB. Then, it is required either to ground common wire of detected device relatively to computer housing or to isolate this device galvanically bu some means. See recommendations in Ch.6.
In signal spectrum digitalized by **E20-10** the components you have not in your signal are present	1) Poor cores screening 2) Current circuit provoking this disturbance via common wires is present in your connection diagram. When coaxial cables closing from the signal source (without braiding disconnection from signal source) the disturbance exists and when the disturbance disappears when cable is fully disconnected from source, it means in-phase disturbance behavior	Use high quality screening Appropriate measures: – Use in-phase EMC filter at output of relevant signal source. - Connect common wires of all devices in one grounding point by shortest way using wire of maximum section. - Use auxilary galvanic isolation device of minimum capacity between part galvanically isolated. See recommendations in Ch.6.
Suspicions on the failure of **E20-10** equipment appeared while operating with **E20-10** with your software.	Your program may not operate properly on**E20-10***or* **E20-10** is actually faulty.	Check the suspect functions of **E20-10** using programs delivered by **L-Card** (or actually applying provided programming examples). In case the failure is confirmed, contact **L-Card.**

External appearance of abnormal	Possible reasons	Troubleshooting measures
When operating in subrange of ±3 V significant distortions occur during signal conversion, meanwhile, the operation of E20-10 module is restored either upon switching off and on the supply voltage of E20-10, or upon programmed switchover of the measurement subrange	in your measurement design voltage supplied to E20-10 input exceeds significantly measurement range of E20-10 having closed to edges ±10 V of maximum permissible voltage at E20-10 input or having exceeded these edges.	Take measures to limit input voltage of E20-10 signal. If you provide detailed technical data on your measurement design L-Card technical support will consult on this issue.

8.1. How to be consulted

A telephone call to **L-CARD** and explaining the problem "in layperson's terms" is, as a rule, a pure waste of time (both yours and another person's) because the specialist needs initial data describing your situation. There is a great amount of these initial data **(you can not remember all), so it is extremely necessary to send them to** L-Card **in writing (email, website conference, fax, regular mail or personal delivery to** L-Card, see the addresses on the reverse side of the title page of this book). The following initial data describing your situation are required:

- Your name and contact data.
- **E20-10** serial number (see on the module body or relevant program-accessible information).
- What computer (which chipset) is used and what type of operating system is used.
- What software and what device driver are used (indicate the version and other information which would help us to understand you).
- What software user settings of **E20-10** are used (ADC conversion frequency, input subrange, the number of channels sampled, duration of interframe delay, ADC synchronization and data acquisition start modes).
- External connections diagram (textual description of connections or a diagram sketch), numbers of connectors contacts and approximate length of wires must be specified.
- What signal sources are used and what output electrical parameters they have.
- Estimation of levels of the signals applied to the product contacts, which type of signal is used (point out specific parameters of signal, if known, pulse or sinusoidal, stray or periodical, frequency bandwidth).
- Under which conditions the product is being handled (laboratory, production).
- Describe the configuration of grounding circuits of the computer, if the sources of signals are grounded and how.
- Finally, describe the observed negative impact providing this description with at least any metric values or assessments!

If you do some work and provide these complete initial data, our specialist will be able to send you the most accurate and correct answer within the shortest possible time!

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