Multichannel data-acquisition systems

LTR Crate System

User Manual

- **Single-slot LTR crates based on CortexM4/CortexM0 dual core processor** with USB 2.0 and Ethernet interfaces (100BASE-TX):

  LTR-CU-1-4, LTR-CEU-1-4.

- **1-, 8- and 16-slot LTR crates with USB 2.0 interface:**

  LTR-U-1-4, LTR-U-8-1, LTR-U-8-2, LTR-U-8-3, LTR-U-16-1, LTR-U-16-2, LTR-U-16-3.

- **2-, 8- and 16-slot LTR crates with Blackfin processor** and USB 2.0/Ethernet interfaces (100BASE-TX):

  LTR-EU-2-5, LTR-EU-8-1, LTR-EU-8-2, LTR-EU-8-3, LTR-EU-16-1, LTR-EU-16-2, LTR-EU-16-3.

- **Analog and digital input-output modules:**

  LTR11, LTR22, LTR24, LTR25, LTR27, LTR34, LTR35, LTR41, LTR42, LTR43, LTR51, LTR114, LTR210, LTR212(M), LTR00.

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L-CARD

http://en.lcard.ru
en@lcard.ru

DAQ SYSTEMS DESIGN, MANUFACTURING & DISTRIBUTION

Author of the manual:
A.V. Garmanov

L-CARD LLC
117105, Moscow, Varshavskoye shosse, 5, block 4, bld. 2

tel.: +7 (495) 785-95-19
fax: +7 (495) 785-95-14

Internet contacts:
http://en.lcard.ru

E-Mail:
Sales department: en@lcard.ru
Customer care: en@lcard.ru

LTR Crate System

Revision history of this document		
Revision	**Date**	**Notes to the updates**
1.0.2	12-2005	The first revision available for users
1.0.3	01-2006	Chapter 1. updated. 0 added
1.0.4	01-2006	Updated: sub-paragraphs 5.2, 6.2
1.0.5	03-2006	Amended: sub-paragraphs 4.6, 5.3.1, 8.1.2, Table 8-3, Appendix A.5. Supplemented: paragraph 8.3.2.1. Added: paragraph 8.4.4, Appendix A.2.2.1.
1.0.6	04-2006	Supplemented: paragraph 8.4, Appendix A.5; added: paragraphs 3.9.1, 3.9.2, 8.3.3.
1.0.7	06-2006	Information about LTR22 updated. Chapter 14. added. Added: paragraphs 3.8, Appendix A.12; sub-paragraphs 3.5, 7.3.1 supplemented;
1.0.8	08-2006	Inserted: chapter about LTR41, LTR42 and specifications for LTR41, LTR42. Chapter 19. (about use of LE-41) supplemented.
1.0.9	09-2006	Information about LTR41, LTR42 supplemented
1.0.10	03-2007	For LTR11, START signal is denoted in Fig. Fig. 5-6. LTR34: paragraph 14.1.3 added
1.0.11	04-2007	Formal numbering of channels for LTR27 with H-27R submodules is changed (Fig. Fig. 7-7).
1.1.0	07-2007	Amendments are introduced subject to the certification results
1.1.1	10-2007	Error in Table 7-3 is corrected regarding submodules H-27U10 and H-27U20.
1.1.3	01-2008	LTR22 specification supplemented A.9
1.1.4	05-2008	LTR212 specification corrected A.2
2.0.1	10-2008	Chapters 3, 4, 5 significantly supplemented regarding the description of new modifications and design versions of LTR crate. New chapter 20. added
2.0.2	10-2008	chapter 20. supplemented. Paragraph 4.6.3 supplemented and corrected
2.0.3	10-2008	Paragraph 4.6.5 added, paragraph 4.7 corrected, sub-paragraphs 3.6.3.2, 3.6.3.3, 4.4.2 supplemented
2.0.4	10-2008	A discrepancy corrected fig. 6-6
2.1.0	03-2009	Raw data added for module LTR114 (new chapter 16. inserted). An error corrected in table 2-2 (indication of 16-slot crate dimensions)
2.1.1	07-2009	Information about LTR114 module (chapter 16.) significantly supplemented, Appendix A.14 with LTR114 specifications added. Information about LTR-EU-8-2, LTR-EU-8-3, LTR-EU-16-2, LTR-EU-16-3 crates added
2.1.2	02-2010	Information about extended functionalities of LTR-EU-8(16) Board Version = 1 in crates added, see sub-paragraphs 4.4.1, 4.4.2, 3.2.3, 3.2.5, 20.2, 20.3
2.1.3	05-2010	Appendices A.17, sub-paragraphs 4.4.1 table 2-5, table 2-6 , paragraph 20.3 added
2.1.4	05-2011	New chapter 18. about LTR00 dummy module inserted
2.1.5	09-2011	Information about the speed of data transmission over the Ethernet (table 2-2) updated
2.1.6	01-2012	Accuracy parameters of LTR114 adjusted (Table A.14, page 352)
2.1.7	04-2012	Paragraph 8.4 supplemented
3.0.0	05-2013	Chapters about new LTR24 (chapter 12. , AppendixA.10), LTR35 (chapter 15. , Appendix A.13), LTR210 (chapter 17. , Appendix. A.15) modules inserted. Sub-paragraphs 4.6.5, 4.7.1 supplemented
3.0.1	06-2013	Chapter 6. Information about new LTR212M module family added and supplemented
3.0.2	07-2013	Information about LTR24-1, LTR24-2 (chapter 12. , AppendixA.10) supplemented
3.0.3	09-2013	fig. 6-7, fig. 6-8 (connection of LTR212(M)) corrected
3.0.4	01-2014	Paragraph 8.4.6 added, page 155
3.0.5	02-2014	fig. 6-3, fig. 6-4 (functional diagrams of LTR212(M)) corrected

Revision history of this document		
Revision	**Date**	**Notes to the updates**
3.0.6	03-2014	New fig.9-2 and paragraph 9.4.4.1 (LTR41) added, chapter 15. (LTR35) supplemented
3.0.7	06-2014	Preliminary data about LTR25 chapter 13. module added, Appendix A.11
3.0.8	06-2014	Sub-paragraphs 11.4.5, 12.4.5 added
3.1.0	10-2014	Information about LTR-CEU-1-4 and LTR-CU-1-4 crates added. table 2-2, table 3-1 updated. Sub-paragraphs 2.2.1.1, 2.3.1, 3.2.6, 3.6.3.3, 3.6.9, 4.5, Appendix A.17, A.20 amended
3.1.1	12-2014	Thermocouple sensors are deleted from the recommended application area of LTR114.
3.2.0	01-2015	In Appendix A, metrological data for LTR212(M), LTR114, LTR24 updated subject to the results of the new LTR certification, Appendix A.23 added.
3.2.1	04-2015	Appendix A.17 on page 359 adjusted.
3.2.2	08-2016	Appendix A.21 supplemented with information about dimensional drawings. Sub-paragraphs 2.4.1, 3.6.1 supplemented with information about the possibility of installation on DIN-rail.

The last revision of this document is available on the web-site: http://en.lcard.ru/download/ltr.pdf.
L-Card reserves the right to update the documentation without notifying the users.

Contents

Chapter 1. What this document is about

This document *is* a User Manual written in a user-friendly manner as far as possible[1]. It describes the technical (hardware) properties of *LTR Crate System*, explains the operation rules and principles of functioning, contains technical specifications and contents of delivery.

This document does not cover any programming or software issues. These issues are addressed in the document titled "LTR Crate System. Programmer's Manual"[1].

Information contained in the manual does not contradict to the document *"LTR Measuring Unit. User Manual DLIZh.301422.0010 RE"* [11], but only describes the LTR in a user-friendly manner.

It should be noted at once that LTR, being a *Russian measuring device* ([10]), has an official title *"LTR Measuring Unit"*.

1.1 How this large book should be read and for whom it would be useful?

For convenient information finding, the book has a deeply hierarchical Table of contents (4 levels of headings) and a comprehensive system of hyper links. The logic of the book is based on the following principles: from *the general to the particular*, from *the simple to the complex*. It is noteworthy that this book is more convenient for reading in the electronic form (as compared to the printed form) because of an electronic Table of contents and a possibility to "travel" using hyper links. The keyword search function also helps to quickly find the required information when working with the electronic document.

Now let us clarify the application of chapters of this book:

Chapter 2. contains concise information about the consumer properties of LTR. This chapter is intended for a wide range of concerned persons who need get an insight into the technical capabilities of LTR system.

Chapter 3. contains information specifically related to practical issues of working with LTR. The issues discussed here will be of interest for specialists and operators.

Chapter 4. In case of introductory reading this chapter can be skipped as it contains a description of internal architecture of LTR crate which would not obviously be necessary at the first reading. In any case, the information contained therein is intended for specialists.

Chapters 5 through 16 contain a detailed description of each LTR module. Each chapter starts with a *general information* about the module, and then the detailed technical description is provided. These chapters are mainly intended for specialists.

Chapter 19. deals with specific configurations of LTR crates.

Chapter 20. is intended for highly-qualified programmers who are set for programming at the level of Blackfin processor.

0, page 324 contains specifications for LTR. Data contained therein are intended for specialists.

0, page 365 contains practical information on solдуving problems in abnormal situations. This information is intended for operators.

[1] but not according to GOST

1.1.1 Why should programmers read this book?

…in fact, it deals with hardware, not programming!

– As practice shows, a significant part of problems related to programming (in particular, those related to the very choice of the programming ideology for a specific application task) could be avoided if the programmer had previously imagined the architecture and features of the hardware he was trying to control, and, unfortunately, we have to admit that there is no faster way to get these ideas about LTR than *to read this manual carefully*.

Chapter 2. LTR Crate System. General characteristics and principles of construction

L-CARD presents a new LTR crate system which is a data acquisition system for production and research applications.

2.1 Intended purpose of LTR

LTR crate system is designed for building multi-channel analog and digital input/output measuring systems. In Table 2-1, tasks are listed which are typical for industrial and laboratory applications. These tasks are figuratively broken down by signal frequency (up to 20 Hz, up to 20 kHz, above 20 kHz), implying the approximate upper limit of the signal frequency band. To some extent, the tasks listed in the Table are solved with the use of LTR modules and submodules.

LTR crates can be equipped with an optional number of LTR modules in accordance with the order.

Table 2-1. LTR modules for typical user tasks

Task	**Signal frequency - up to 20 Hz**	**Signal frequency - up to 1-2 kHz**	**Signal frequency - up to 20 kHz**	**Signal frequency - above 20 kHz**
Signal digitizing: millivolt voltage of thermocouples	LTR27 + H-27T			
Signal digitizing: voltage up to ± 10 V	LTR27 + H-27U, LTR11, LTR22, LTR24, LTR114, LTR210.	LTR11, LTR22, LTR114, LTR24, LTR210.	LTR11, LTR22, LTR24, LTR210	LTR11 LTR210
Digitizing with high spectral signal fidelity: voltage up to ± 10 V, vibrometry	LTR22, LTR24	LTR22, LTR24	LTR22, LTR24	
Signal digitizing: resistance	LTR27 + H-27R, LTR114 (up to 4 kOhm) LTR212M-1 (quarter-bridge)	LTR114 (up to 4 kOhm)		
Signal digitizing: “bridge unbalance”	LTR212(M) LTR114	LTR212(M) LTR114		
Signal digitizing: current 0...5 mA, ±10 mA, 0...+20 mA	LTR27 + H-27I			
Signal digitizing: charge up to ±800 pC, up to ±9000 pC	LTR11 + LE-41, LTR22 + LE-41, LTR24 + LE-41 (0.3 Hz...22 kHz)	LTR11 + LE-41, LTR22 + LE-41, LTR24 + LE-41 (0.3 Hz...22 kHz)	LTR11 + LE-41, LTR22 + LE-41, LTR24 + LE-41 (0.3 Hz...22 kHz)	
ICP-sensor signal digitizing	LTR24-2 LTR25	LTR24-2 LTR25	LTR24-2 LTR25	LTR24-2 LTR25

Task	**Signal frequency - up to 20 Hz**	**Signal frequency - up to 1-2 kHz**	**Signal frequency - up to 20 kHz**	**Signal frequency - above 20 kHz**
Oscillographic module supporting connection to a standard oscillographic probe	LTR210	LTR210	LTR210	LTR210
Digital-to-analog signal conversion, voltage up to ± 10 V, auto-generation of a periodic signal	LTR34, LTR35	LTR34 (up to 3 kHz), LTR35	LTR35	LTR35
Measurement of signal frequencies and cycles with the signal pre-selection according to the programmable level: signal amplitude and selection levels up to ± 10 V	LTR51 + H-51FL	LTR51 + H-51FL	LTR51 + H-51FL or LTR51 + H-51FH	LTR51 + H-51FH
Multichannel signal detection of signals using the selection method according to the programmable level up to ± 10 V	LTR51 + H-51FL	LTR51 + H-51FL	LTR51 + H-51FL or LTR51 + H-51FH	LTR51+H-51FH
Asynchronous input/output of digital TTL signals	Asynchronous[1] input/output: LTR43, asynchronous input: LTR41			
Synchronous output of digital TTL signals	LTR35	LTR35	LTR35	LTR35
Controlling actuator circuits with the use of solid state relay	Asynchronous output: LTR42			
Determining the status of contacts connected to a common wire	Asynchronous input: LTR43			
Synchronization in a LTR crate, synchronization between LTR crates[2]	LTR41, LTR42, LTR43	LTR41, LTR42, LTR43	LTR41, LTR42, LTR43	LTR41, LTR42, LTR43

It is possible that the range of tasks solved by LTR can be expanded due to the introduction of new LTR devices which depends on the actual demand. The information about the current LTR offer package can be found on the web-site en.lcard.ru. You can also ask a question at a conference on L-Card's web-site and send an e-mail to the support team at en@lcard.ru.

You can submit your suggestions and comments either at a conference or via email, which will be carefully considered by L-Card.-

[1] asynchronous means not strictly periodic, when only average input-output frequency can be considered

[2] Own synchronization means of LTR crates are not taken into account in this table

2.2 Most important consumer properties of LTR.

In this section, summarized information about LTR is presented which is the most important for consumers. In addition, important details of the LTR crate system architecture concept are briefly described here.

2.2.1 LTR crate highlights:

- Modular design of the crate system which allows to equip the crate with the necessary set of LTR modules optimal for a specific user task.
- The LTR system provides for both large 8- and 16-slot crates and small 1- and 2-slot ones. It is possible to expand the system configuration flexibly with preserving full software compatibility of these crates[1]. In particular, this provides a starting opportunity for developers of new systems: as they can try an inexpensive LTR configuration with a little number of slots with a prospect for simple transition to a larger configuration in the future.
- Single index data format: The *32-bit format* contains, in addition to data, the channel number, module number and service information, which facilitates the software processing of multi-channel information.
- LTR crate control software works on the basis of the system-independent "client-server"-control interface.
- Galvanic isolation of any LTR module from the computer and crate frame which improves the quality and convenience of external connections.

Main consumer properties of LTR crates, depending on the modification and design version, are summarized in table 2-2. The system of LTR crates designation is described in paragraph 2.3.1.

[1] at the level of general hardware features of the selected LTR crates. You can find the full description of hardware features for each type of LTR crates in this manual.

Table 2-2. Basic characteristics of LTR crates

Characteristics	LTR CRATE							
	LTR-U-1-4	**LTR-U-8-1 LTR-U-8-2 LTR-U-8-3**	**LTR-U-16-1 LTR-U-16-2 LTR-U-16-3**	**LTR-EU-2-5**	**LTR-EU-8-1 LTR-EU-8-2 LTR-EU-8-3**	**LTR-EU-16-1 LTR-EU-16-2 LTR-EU-16-3**	**LTR-CU-1-4**	**LTR-CEU-1-4**
Maximum quantity of I/O LTR modules	1	8	16	2	8	16	1	1
Allocated slot of removable crate controller	No	No	No	No	No	No	No	
Crate controller module[1]	LTR021 (built-in)	LTR010 (built-in)		LTR031 (built-in)	LTR030 (built-in)		LTR021U (built-in)	LTR021M (built-in)
ARM /processor/ controller type	ARM controller AT91SAM7S256	AVR controller Atmega162		Blackfin signal processor ADSP-BF537			LPC4337 (CortexM4/CortexM0 dual core processor)	
RAM	64 KB	Two 4 MB FIFO buffers		32 MB			32 MB	
Interface	USB 2.0 full speed	USB 2.0 *high-speed*		USB 2.0 *high-speed* / Fast Ethernet (100BASE-TX)			USB 2.0 *high-speed*	Fast Ethernet (100BASE-TX) USB 2.0 *high-speed*
FPGA/CPLD type	CPLD EPM3128 does not require loading, is not user-updated	FPGA EP1K50 (Acex 1K) – loaded at start-up, – firmware is user-updated		FPGA EP1C30 (Cyclone I) – loaded at start-up, – firmware is user-updated			CPLD EPM240T100 does not require loading, is not user-updated	
Volume of hardware FIFO data/command buffer for transfer to the LTR module	No hardware FIFO buffer (this function is implemented by software)	12 commands/data (32 bit) for each LTR module		12 commands/data (32 bit) for each LTR module			No hardware FIFO buffer (this function is implemented by software)	
Possibility to update the firmware[2]	ARM controller	AVR controller FPGA		Load Flash memory ADSP, FPGA			ARM controller	

[1] The built-in crate controller module is an integral component of the crate configuration (not supplied separately).

[2] The user can update the firmware using the publicly available versions of updates provided by L-Card

Characteristics	**LTR CRATE**							
	LTR-U-1-4	**LTR-U-8-1 LTR-U-8-2 LTR-U-8-3**	**LTR-U-16-1 LTR-U-16-2 LTR-U-16-3**	**LTR-EU-2-5**	**LTR-EU-8-1 LTR-EU-8-2 LTR-EU-8-3**	**LTR-EU-16-1 LTR-EU-16-2 LTR-EU-16-3**	**LTR-CU-1-4**	**LTR-CEU-1-4**
Additional possibility of low-level crate programming	Not provided to user			Provided to user There is a possibility to connect a JTAG emulator			Provided to user There is a possibility to connect a JTAG emulator	
Flash data memory	No	No	No	2 GB Flash (option)			No	No
Number of digital crate synchronization inputs[1]	1 pc per input	0	0	2 lines per input 2 lines per output			2 lines per input 2 lines per output	
Maximum data transmission speed	**800 KB/s** (via USB 2.0 full speed)	**20 MB/s** (via USB 2.0 high speed)	**20 MB/s** (via USB 2.0 high speed)	**16 MB/s** (via USB high speed) **10 MB/s** (via Ethernet)			**2 MB/s**	
Crate design	PorTable	Mobile	Mobile, rack mounting (19" width, 3U height) is possible	PorTable	Mobile	Mobile, rack mounting (19" width, 3U height) is possible	PorTable	
Power supply voltage, V	$=12^{+12}_{-1}$	~220 (LTR-U-8-1) ~220/=12 (LTR-U-8-2) ~220/=27 (LTR-U-8-3)	~220 (LTR-U-16-1) ~220 /=12 (LTR-U-16-2) ~220 /=27 (LTR-U-16-3)	$=12^{+18}_{-1}$	~220 (LTR-EU-8-1) ~220/=12 (LTR-EU-8-2) ~220/=27 (LTR-EU-8-3)	~220 (LTR-EU-16-1) ~220 /=12 (LTR-EU-16-2) ~220 /=27 (LTR-EU-16-3)	$=12^{+12}_{-1}$	
Power supply source	Network card (supplied)	Built-in	Built-in	Network card (supplied)	Built-in	Built-in	Network card (supplied)	
Possibility of quick replacement of a LTR module	No	Yes	Yes	No	Yes	Yes	Yes	Yes
Maximum power consumption	8 W	80 V*A	150 V*A	20 W	80 V*A (80 W)	150 V*A (150 W)	10 W	10 W
Frame dimensions[2]	135x41x189 mm	236x133x378 mm	481x136x406 mm	135x61x189 mm	236x133x378 mm	481x136x406 mm	135x41x189 mm	

Notes:

1. For more details about the functionalities of LTR-EU crates, refer to paragraph 4.4.1

[1] without accounting for LTR modules synchronization lines

[2] no allowance being made for projecting parts of connectors, handle for 8-slot crate

2.2.1.1 Limits of the current implementation of LTR-U-1-4 crate.

Today, L-Card manufactures LTR-U-1-4 crate with USB 2.0 *full-speed* interface, while multi-slot USB LTR crates support *full-speed* and *high-speed* interface USB 2.0 (L[21]).

! The current implementation of LTR-U-1-4 with USB *2.0 full-speed* interface provides for limiting of data transmission speed above 800 KB/s.

Since LTR uses the 32-bit data format, the limits of the current LTR-U-1-4 implementation will lead to limiting the maximum frequency of LTR11 ADC (up to 200 kHz inclusively), LTR22 ADC (up to 52 kHz inclusively) modules, LTR34 DAC output speed (up to 200 kS/s) in the stream output mode (the output speed will remain up to 500 kS/s in the self-excited oscillator mode), as well as the speed of data acquisition from the LTR24, LTR25, LTR210 modules (up to 200 kHz inclusively).

For more details about the limits of LTR-U-1-4 implementation, see also paragraph 4.3.1 on page 72.

Note: Single-slot LTR-CU-1-4 and LTR-CEU-1-4 crates have no speed limits described above!

2.2.2 General consumer properties of LTR modules (overview):

In all LTR modules, inputs and outputs of the modules are galvanically isolated from the crate frame and power supply circuits. The galvanic isolation is made using the newest elements named "digital insulators".

In LTR modules, functional and design succession has been preserved to the maximum extent in relation to similar modules of LTC and- H2000 systems, but the direct compatibility of LTR modules with these systems is not supported.

Universal crate synchronization through LTR43 module or similar functionalities of LTR-EU, LTR-E, LTR-CEU, LTR-CU crate controller.

The maximum power consumption of a single LTR module is up to 6 W.

2.2.2.1 LTR11 module (14-bit 400 kHz ADC, 16/32 switched channels)

- 400 kHz ADC frequency can be flexibly redistributed among the switched channels[1]. The number and order of channel inquiring are programmable.
- Independent program setting for each channel of the input signals range (± 10 V, ± 2.5 V, ± 0.6 V, ± 0,15 V).
- In the programmable "Check Input Lines" mode, the user can detect breaks and short circuits of input lines.
- Programmable ADC startup modes: internal, edge-triggered or at external signal fall.

More information about LTR11 can be found in paragraph 5.1, page 95; the specification for LTR11 is presented in Appendix A.1, page 324

[1] to achieve maximum ADC accuracy in the multi-channel mode at ADC frequency of more than 50 kHz, it is recommended to connect the inputs of LTR11 to the low-resistant signal source with as short cable as possible

2.2.2.2 LTR212(M) is a strain-gauge module

- Up to 8 strain-gauge channels.
- Functionally is similar to- LC212, but is implemented on a modern element base and is compatible with LC212 -connector contacts.
- The software-switched reference voltage source (+5 V or +2.5 V) provides power supply to 8 strain gauges with a resistance of 100 Ohm each.
- Digital filtering in ADSP2185M.-
- New LTR212M modifications with extended quarter bridge connectivity and other features

More information about LTR212(M) can be found in paragraph 6.1, page 110; the specification for LTR212(M) is presented in Appendix A.2, page 327.

2.2.2.3 LTR27 module can carry up to 8 H-27x measuring sub-modules

- Full compatibility with H-27x measuring sub-module family.
- Full compatibility of input connector contacts with LC237, H27, E270. LC-237, H-27, E-270 carriers.
- Ensures ± 0.05% accuracy of current, voltage, and resistance measurements.
- Channel-by-channel galvanic isolation.
- The maximum data acquisition frequency is 100 Hz per channel.

More information about LTR27 can be found in paragraph 7.1, page 134; the specification for LTR27 is presented in Appendix A.3 , page 331.

2.2.2.4 LTR43 is a digital- I/O and crate synchronization module

- Functionally, is similar to H-43 and is compatible with its contacts.
  - 4 I/O ports for TTL signals (up to 32 lines in total), each port is configured in software for input or output.
  - Digital asynchronous input/output or stream quasisynchronous input with an average input period from 10 ms to 10 μs (possible input irregularity is about 1 μs).
- All TTL inputs have pull-up resistors to +5 V, so these inputs are useful for scanning the status of external switches connected to a common wire.
- LTR crate synchronization functions: second mark generator with internal or external triggering.
- Separate galvanically isolated section with an external RS 485 interface (for example, for controlling several LE41 charge amplifiers) and a ± 12 V power supply for external devices (for example, for up to 4 LE41 amplifiers).

More information about LTR43 can be found in paragraph 8.1, page 143; the specification for LTR43 is presented in Appendix A.5, page 333.

2.2.2.5 LTR41 и LTR42 modules of digital input, output and synchronization have channel-by-channel galvanic isolation

- LTR41: Digital input of 16 -TTL/CMOS-signals (5 B -logic) as well as current logic signals (up to 25 mA) with channel-by-channel optoisolator.
- LTR42: Output of 16- control signals by external actuators via optorelay outputs with channel-by-channel galvanic isolation. The optorelay actuating circuit can be connected into DC or AC circuits.
- Synchronization of data acquisition in a single crate or in a multi-crate system is similar to LTR43.

- External device stabilized power supply output +5 V 0.3 A.

More information about LTR41, LTR42 can be found in paragraph 9.1, page 156; LTR41 specification for is presented in Appendix A.6, page 335, LTR42 specification is presented in Appendix A.7, page 336.

2.2.2.6 LTR51 is a frequency and time interval metering module

- Allows measuring using the *adjoining intervals method*[1]: frequency from 0 to 170000 Hz, time intervals from 0 to ∞ with 2 μs resolution. Input signal voltage range is ±10 V.
- Allows multi-channel signal detecting using the selection method according to the programmable level of up to ± 10 V.
- Architecture is scalable from 2 to 16 channels by installing from 1 to 8 two-channel H51Fx sub-modules-.
- Functionally is similar to H-51. Is compatible with H51connector- contacts.
- H-51Fx sub-modules are supplied in two design options: low-frequency -H51FL for signals with a bandwidth of up to 15 kHz; high-frequency -H51FH for signals up to 170 kHz.
- Each channel has an input threshold device for selecting signals by level with adjusTable upper and lower hysteresis thresholds. This allows selecting the components of complex signals by level, measuring their frequencies and time intervals.
- H51Fx sub-modules can be pre-set with jumpers for the range of hysteresis threshold adjustment (± 1.2 V or ± 10 V).- Within each threshold adjustment range, there are 256 basic setting units for accurate software threshold setting. For both hysteresis threshold ranges, the input signal range is ± 10 V.
- LTR51 module is synchronized with the common LTR crate reference generator (see the specifications in Appendix
- Flexible downloaded architecture of LTR51 allows assigning completely different functions to the same module hardware by transforming LTR51, for example, into a **logic analizer** simply by downloading other FPGA firmware without taking module out of the crate. -L-Card company is ready to consider the possibility of such implementations at your request.

More information about LTR51 can be found in paragraph 10.1, page 165; the specification for LTR51 is presented in Appendix A.8, page 336.

2.2.2.7 LTR22 module (16 bit sigma-delta audio ADC, 4 channels)

- Functionally, is similar to H22- and is compatible with its connector contacts[2].
- The architecture of 4 -independent data acquisition channels (without dynamic switching) - with separate ADC channels.
- Independent software configuration for each input signal subrange channel: *±10 V, ±3 V, ±1 V, ±0.3 V, ±0.1 V, ±0.03 V* (for comparison: in H-22-, the subrange configuration was partially dependent due to simultaneous activation of a 1:10 attenuator for all channels).
- High-quality differential inputs of 4- channels. A common-mode signal range is ±10 V in - any subrange.

---

[1] the method is described in the document titled "HB-16 Specialized Measuring Complex. User Manual"[8] in the H-51 module description, see paragraph 13.4.4

[2] the main differences with H-22: changes in frequency grids and subranges of input signal levels

- An extremely broad ADC frequency tuning range for sigma-delta ADC (from several kHz to 78 kHz).
- Built-in LPFs with an optimal configuration (a suppression band always starts from half the ADC sampling frequency) for any specified ADC frequency.
- A special DC component cut-off mode is simultaneously activated by software means for -4 channels, and compensates the DC component of a signal in the ±10 V range.
- Logical signs of LTR22 overload (ADC scale exceeded) with an input signal are individual for each channel.
- In contrast with H-22-, LTR22 has no RS-485 -interface to control LE-41 charge amplifier (now this function is implemented -centrally in LTR43).

More information about LTR22 can be found in paragraph 11.1, page 177; LTR22 specification is presented in Appendix A.9, page 337.

2.2.2.8 LTR24 module (16-bit sigma-delta audio ADC, 4 channels)

LTR24 module is a development of LTR22 module by a number of qualitative parameters. LTR24 modifications with an option of a direct connection of ICP sensors are available.

For more details, refer to paragraph 12.1, page 191.

2.2.2.9 LTR25 module (24 bit sigma-delta audio ADC, 8 channels for ICP sensors)

LTR25 is a specialized ADC for working with ICP sensors.

More details are provided in Chapter LTR25 LTR25 ADC module (announce) .

2.2.2.10 LTR34-4 and LTR34 modules-8 (16-bit DAC, 4 and 8 channels)

- A reasonable balance is achieved between the DAC quality for direct and alternating current.
- Data output modes for DAC channels: *asynchronous output*, 1, -2, -4 -and 8-channel *synchronous stream output*, 1-, 2-, 4- and 8-channel *synchronous generation of a periodic signal* (previously recorded in LTR34 buffer)
- *Sample stream output frequency for the DAC* channel is Fs = F/N, where F- is selected from 31.25 kHz to 400 kHz (60 frequencies), N- is a number of channels (N = 1, 2, 4 or 8).
- *Sample stream output frequency for the DAC channel in a free-running mode* is Fs = F/N, where F is selected from 31.25 kHz to 500 kHz (61 frequencies), N is a number of channels (N = 1, 2, 4 or 8).
- Each channel has two single-phase outputs: 1:1 and 1:10. Output signal ranges for each channel: ±10 V in 1:1 output, ±1 V in 1:10 output.
- *The periodic signal* free-running mode allows for pre-recording of 2 to 2,000,000 samples into DAC buffer, and then starting a synchronous cyclical sample output from DAC *buffer without data swapping from PC* (free-running mode).
- *An external start input with a galvanic optoisolator* allows for starting a synchronous data output from an external synchronization signal.

More information about LTR34 can be found in paragraph 14.1, page 227; LTR34 specification is presented in Appendix A.12, page 348.

2.2.2.11 LTR35 module (24-bit DAC, 8 channels).

LTR35 module is a high-performance multi-functional sound DAC and generator.

For more details, refer to paragraph 15.1, page 238.

2.2.2.12 LTR210 module (high-speed ADC, 10 MHz, 14 bit, 2 channels).

LTR210 (chapter 17. , page 271) is an oscillographic module with frame-by-frame data collection via 32 MB buffer module memory. An option for multi-module synchronization is available ensuring multi-channel parallel frame-by-frame data acquisition.

2.2.2.13 LTR114 module (24-bit ADC, 16/8 channels for voltage/resistance measuring)

- 24-bit 4 kHz differential input ADC with switching option for up to 16- channels, with ±10 V, ±2 V, ±0.4 V input subranges specified by software independently for each channel.
- Resistance measurement while switching up to 8 channels using a 4-wire diagram (up to 8 channels may function as a switchable current source for a 4-wire resistance measurement diagram). Resistance measurement ranges: 0÷400 Ohm (at current = 1.0 mA), 0÷1200 Ohm (at current = 0.33 mA), 0÷4,000 Ohm (at current = 0.1 mA). Resistance measurement modes: - standard mode (up to 4 kHz), − oscillating reference current mode (up to 2 kHz).
- LTR114 implements the following possible ratios between the numbers of voltage/resistance measurement channels: 16/0, 14/1, 12/2, 10/3, 8/4, 6/5, 4/6, 2/7, 0/8 (of course, smaller numbers of measurement channels in the above-mentioned pairs are also implemenTable)
- Auxiliary service function: check for a breakage or short circuit of external signal lines
- Functions of the external universal interface line:
  - Support of the "1-wire" interface (in particular, for **DS18S20** external temperature sensor).
  - Synchronization of data acquisition among several LTR114 modules based on the "master-slave" principle.
- Mode of check for a breakage or short circuit of external signal lines.
- Backup (duplication) mode.

Chapter 16. LTR114 description is presented in (page 247). The operational characteristics are given in Appendix A.14 on page 352.

2.2.2.14 Prototype module LTR00

LTR00 module is intended for mounting of user nodes (option is available to user). LTR00 board has:

1) Node of stabilized supply source +5 V (0,2 A), +-15 V (2x0,04A) (both having separate galvanic isolation) which can be applied for different demands.

2) Available for order of LTR00 modification:

- Panel of LTR00-01 module has spare DRB-37M connector for user connections.
- Panel of LTR00-02 module is blind and does not have connector.

3) LTR00 has constructive option of mounting the printed-circuit board as per user design (drawings will be provided) as the second level; this board will have PLD/PBD plug connections

with carrier board having the possibility of connection to supply circuits, signal circuits from the DRB-37M connector. *This design will give the user opportunity to apply its own printed-circuit board keeping markeTable condition of module in whole.*

4) Over the entire free area of LTR00 board there are spare slots for output elements with spacing 2,54 mm and scale of slots SMD with spacing 1,27 mm for narrow SOIC (frame width is 150 mil), there are 4 mounting holes for supports of user board.

For more details about LTR00 module, refer to L. [6], page 367.

2.3 Designation of LTR crates, modules and sub-modules.

2.3.1 Modifications and design versions of LTR crate

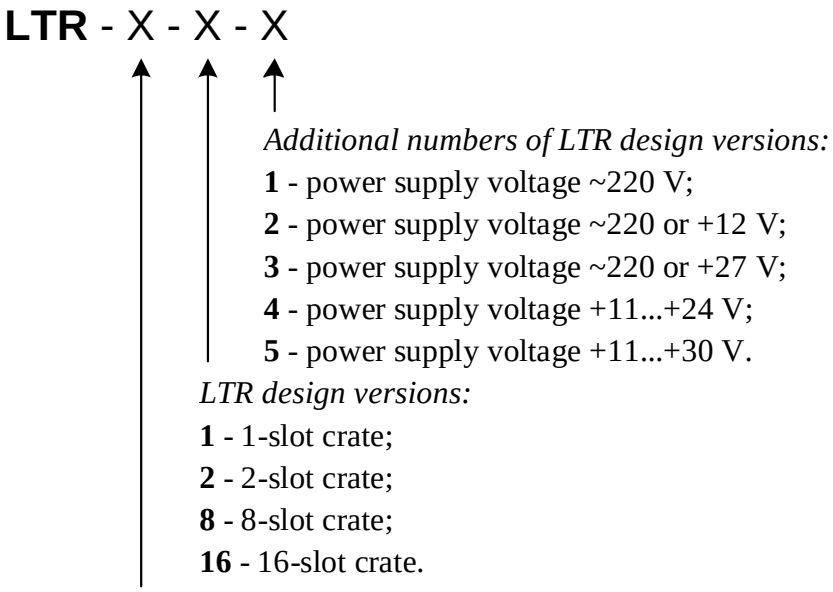


Fig. 2-1. LTR crate designation system

You may send a request about available modifications and design versions of a LTR crate to L-Card.

Below are the designations of LTR structural units determining the LTR composition when ordering.

2.4 LTR crate and modules configuration

Table 2-3. LTR crate configuration

Component	LTR-CU	LTR-CEU	LTR-U			LTR-EU		
	Design version		Design version			Design version		
	1-4	**1-4**	**-1-4**	**-8-1 -8-2 -8-3**	**-16-1 -16-2 -16-3**	**-2-5**	**-8-1 -8-1 -8-3**	**-16-1 -16-2 -16-3**
USB 2.0 cable, type A-B, length 1.5 – 2.0 m	1 pc.	1 pc.	1 pc.	1 pc.	1 pc.	1 pc.	1 pc.	1 pc.
Ethernet Pathcord cable, cat. 5e, length 1.5 m	–	1 pc.	–	–	–	1 pc.	1 pc.	1 pc.
220 V network cable	–	–	–	1 pc.	1 pc.	–	1 pc.	1 pc.
Blank panels for unused crate slots	–	–	–	The number is specified in the order		–	The number is specified in the order	
CD-ROM with the documentation and software	1 pc.	1 pc.	1 pc.	1 pc.	1 pc.	1 pc.	1 pc.	1 pc.
Synchronization connector cable	MDN-9 connector – 1 pc.		AUD-31 connector – 1 pc.	–	–	MDN-9 connector – 1 pc.		
External power supply source - network card ~220V	1 pc.	1 pc.	1 pc.	–	–	1 pc.	–	–
Low-voltage power connector cable	DJK-10A –1 pc.		DJK-10A –1 pc.	–	–	DJK-10A –1 pc.	–	–
2 GB Flash memory	–	–	–	–	–	Option – to be specified when ordering		

The CD-ROM supplied contains this document, the programmer's manual, the user manual, the verification procedure, *LTR -server* software, UTS (universal test-stand) software, programming examples, drivers.

Updated software and documentation can be found in the file library on our web-site: en.lcard.ru/download

Ordered crates and modules are supplied with the relevant certificates.

LTR modules have additional parts specified in Table 2-4.

Table 2-4. LTR modules configuration

Module	Additional components	Number of
LTR11	DB-37F connector with shell	1 pc.
LTR22	DB-37F connector with shell	1 pc.
LTR24, LTR24-1, LTR24-2	DB-37F connector with shell	1 pc.
LTR25	DB-37F connector with shell	1 pc.
LTR27	H-27x sub-modules DB-37F connector with shell	from 1 to 8 pcs (according to the order) 1 pc.
LTR34	DB-37F connector with shell	1 pc.
LTR35	DB-37F connector with shell	1 pc.
LTR41	DB-37F connector with shell	1 pc.
LTR42	DB-37F connector with shell	1 pc.
LTR43	Jumper[1] DB-37F connector with shell	9 pcs. 1 pc.
LTR51	H-51Fx sub-modules DB-37F connector with shell	from 1 to 8 pcs (according to the order) 1 pc.
LTR114	DB-37F connector with shell DS18S20 temperature detector	1 pc. 1 pc. (if this is specified in the order)
LTR210	Additional cables and modules can be supplied under a separate order.	–
LTR212, LTR212M-2 LTR212M-3	DB-37F connector with shell	1 pc.
LTR212M-1	DB-37F connector with shell LTR212H mezzanine card for soldering quarter-bridge balancing resistors with fasteners included in the scope of supply	1 pc. 1 pc.

Notes:

1. When ordering LTR modules supplied with LTR-U-1-4, LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4, the standard panel of LTR-module FRN1L is not included into the scope of supply (for the module configuration, see paragraph 3.4).

2. Modules are installed into LTR-U-1-4, LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4 crates by the manufacturer in accordance with the order. The user should not make any changes into the configuration of these crates (see paragraph 3.6.2.2, page 52). When ordering any configurations of these crate which include LTR43 or LTR51 modules, do not forget to specify the jumpers status (see, respectively, paragraph 8.4, page 148, and paragraph 10.2, page 166).

[1] for module configuring

2.4.1 Additional devices connected to a LTR crate

These devices are not included into the LTR configuration but can be integrated into a LTR crate, for example: LE41 charge -amplifier (see chapter 19. , page 305 for the description of special configurations), cables and other products.

Table 2-5. LTR crate. Additional devices manufactured by L-Card

Item	Intended purpose	Note
Mounting set DIN-LTR2	LTR-EU-2-5 crate mounting set for mounting on DIN-rail	Mounting on DIN-rail is possible for LTR-EU-2crates manufactured after August 2016. These crates have mounting openings.
LTRN00 module	LTR prototype module	Installed into LTR crate, has fields of metallized holes on the printed circuit board with a pitch of 2.54 mm and free contacts on DRB-37 connector for user connections, and also has galvanically isolated ± 15 V and + 5 V voltage sources (the total load power is up to 4 W)
LE-41 module	4-channel- charge amplifier	Installed outside the LTR crate[1].
OP-27TR	Cold junction compensator	
37-contact -terminal block		Only for test connection to LTR-modules without soldering (see paragraph 3.6.7, page 61).
LTR-CMF1A cable adapter	This adapter cable (with DB-37F and DB-37M connectors at the ends) is an *in-phase noise suppression filter*. It is used to prevent failures of LTR crate - equipment in the- event [2]of connection to external equipment generating high-speed impulse noise applied relatively to the grounding point of LTR crate frame	Is connected to the user connector of LTR-modules. The manual see L. [3]
LTR-CMF1B set	This is a set for filter (similar to LTRCMF1A) installation by the user inside -the casing of the cable part of the DB37F -connector	The manual see L. [3]
DS18S20 temperature detector	Is used in LTR114 for temperature measurement	Supplied if specified in the order

[1] L-Card does not supply ready-made cables for connecting LE-41 to LTR. For specific recommendations, refer to sub-paragraph 19.1.1, 19.1.2..

[2] as well as in many other products, including those manufactured by L-Card, which have a block signal connector of DRB-37M (or DB-37) type, with the casing directly connected to the grounded casing of the product.

Item	Intended purpose	Note
RS485-UART cable	It is used to expand the functionality of LTR-EU, LTR-CU, LTR-CEU crates and represents an implementation of RS-485/RS-422 interface galvanically isolated from Blackfin processor crate controller	Not supported for LTR-EU Board Version = 0 crates (paragraph 4.4.1) . When using this cable with an available LTR-EU-8/16 crate (or when ordering a new crate) ask L-Card specialists if your crate supports 160 mA output external device power current in a 3.3 V circuit on the SYNC connector (fig. 3-5). If this is not supported, L-Card can upgrade the crate as necessary. LTR-EU-2 Board Version ≠ 0 crate does not require the above mentioned upgrading.
LTR-JTAG cable	Is used for connecting an inexpensive JTAG emulator ADZS-ICE-100B to LTR-EU crates.	See fig.20-2
2 GB micro SD-card	Is used as user memory in LTR-EU crates.	External installation into the connector is only possible for LTR-EU Board Version ≠ 0

In table 2-6, items are listed which are not manufactured by L-Card but can be purchased from external suppliers.

Table 2-6. LTR crate. Useful additional devices supplied by external suppliers

Item	Intended purpose	Note
ADZS-USB-ICE	JTAG emulator	Full-speed USB interface with the data transmission rate of up to 150 kB/s. Manufacturer: Analog Devices www.analog.com
ADZS-HPUSB-ICE	JTAG emulator	High-speed USB interface with the data transmission rate of up to 2 MB/s. Manufacturer: Analog Devices www.analog.com
ADZS-ICE-100B	JTAG emulator	This JTAG emulator is dramatically cheaper than the above one and has a "minimalistic" frameless design. USB interface with the data transmission rate of 255 kB/s. Manufacturer: Analog Devices www.analog.com For connection to LTR-EU, LTR-JTAG (table 2-5) cable is needed.

We recommend to purchase products from Analog Devices through their official distributors (the list of distributors can be found on web-site www.analog.com)

2.4.2 Specific cables for LTR system.

Generally, design and manufacturing of specific cables is the user's concern. However, in principle, it is possible that the cable be designed and manufactured by L-Card *under a separate order* according to your requirements which shall be discussed with L-Card.

Chapter 3. LTR crate operation

This chapter contains consolidated practical information about the design, installation, connection and operation of LTR crates.

3.1 General information about the LTR crate design

A LTR crate, as a structural unit, is designed for installation of LTR family modules and providing an interface between the host -computer and LTR- modules.

8- and 16-slot crates have a desktop porTable design (8-slot crates are equipped with a large instrument handle for carrying, 16-slot crates have two small handles on their sides). 16-slot crates are suiTable for installation in a standard 19" rack. The frame is made of an aluminum alloy with external plastic elements. 8- and 16-slot crate design allows for rapid replacement of LTR-modules.

1- and 2-slot crates have a porTable design based on a plastic frame. A LTR module is installed into the frame by the manufacturer. For a user, it is a challenge to replace the LTR module in the crate[1].

The front panel of all LTR crates is a panel with 37-pin connectors of LTR-modules (type DB-37M). All LTR modules have connectors of the same type.

LTR crates have the following external structural elements: frame, front and rear panels with user connectors, indication, power switch and reset button. Key internal elements include: crate controller, motherboard (for installation of LTR-modules), power supply unit. In Table table 3-1, the summarized data for all these components are presented, in particular, designations of crate controllers, motherboard, and power supply units used. These structural designations will be used hereafter in functional descriptions of the crates (chapter 4.) .

! All structural elements inside a LTR crate are numbered starting from one. Mounting seats in the LTR-crate, channel numbers in LTR -modules and submodules, numbers of slots in LTR modules for installation of submodules, as structural elements, are always numbered - starting from one.

It should always be taken into account that this agreement does not in principle prescribe how the above entities will be coded (addressed) in the program: probably, from zero, but any other way of coding specified in the programming manual may be used as well.

In 2-slot LTR-EU-2-4 crate, from top to bottom numbering order is used for LTR modules while in 8 and 16-slot crates, LTR modules are numbered from left to right.

The front view of LTR crates is presented on page 34-35.

The front view of LTR-EU-8 and LTR-EU-16 crates is not shown. It is different from LTR-U-8 and LTR-U-16 crates, respectively, with its front panel design.

[1] but this is, in principle, possible, in case of accurate handling and having appropriate skills

Fig. 3-1. LTR-U-8-1 (-2, -3) crate

Fig. 3-2 LTR-U-16-1 (-2, -3) crate

Fig. 3-3. LTR-U-1-4 crate

Fig. 3-4. LTR-EU-2-5 crate

In 8- and 16-slot crates, front panels are narrow bars located to the left of the first module slot.

Descriptions of the indication, switches, and connectors located on the panels of LTR crates for all modifications and design options are presented in sub-paragraphs 3.2 - 3.2.5.

The appearance of single-slot LTR-CU-1-4 and LTR-CEU-1-4 crates is different from LTR-U-1-4 with the design of the rear panel, marking on the top of the frame, and a label on its bottom.

Table 3-1. Generalized structural characteristics of LTR crates

Structural characteristics	LTR-U (LTR-CU, LTR-CEU)			LTR-EU		
	Design version			Design version		
	LTR-U-1-4 (LTR-CU-1-4, LTR-CEU-1-4)	**LTR-U-8-1 LTR-U-8-2 LTR-U-8-3**	**LTR-U-16-1 LTR-U-16-2 LTR-U-16-3**	**LTR-EU-2-5**	**LTR-EU-8-1 LTR-EU-8-2 LTR-EU-8-3**	**LTR-EU-16-1 LTR-EU-16-2 LTR-EU-16-3**
Number of slots of LTR modules	1	8	16	2	8	16
Crate design	PorTable	Mobile	Mobile, rack mounting (19" width, 3U height) is possible	PorTable	Mobile	Mobile, rack mounting (19" width, 3U height) is possible
Dimensions[1]	135x41x189 mm	236x133x378 mm	481x136x406 mm	135x61x189 mm	236x133x378 mm	481x136x406 mm
Power supply voltage, V	$+12^{+12}_{-1}$	~220 (LTR-U-8-1) ~220/=12 (LTR-U-8-2) ~220/=27 (LTR-U-8-3)	~220 (LTR-U-16-1) ~220/=12 (LTR-U-16-2) ~220/=27 (LTR-U-16-3)	$=12^{+18}_{-1}$	~220 (LTR-EU-8-1) ~220/=12 (LTR-EU-8-2) ~220/=27 (LTR-EU-8-3)	~220 (LTR-EU-8-1) ~220/=12 (LTR-EU-8-2) ~220/=27 (LTR-EU-8-3)
External network card (supplied)	Yes	No	No	Yes	No	No
Built-in crate controller	LTR021 (LTR021U, LTR021M)	LTR010	LTR010	LTR031M	LTR030	
Built-in crate motherboard	No	LTR001	LTR001 – 2 pcs per crate	LTR031C	LTR001	LTR001 – 2 pcs per crate
Internal crate power supply unit	Internal voltage converter	LTRP1 LTRP12 LTRP27	LTRP1 LTRP12 LTRP27	Voltage converter as a component of LTR031M controller	LTRP2	LTRP2
LTR module panel used when installing into a crate	Special panel	Basic panel design		Special panel	Basic panel design	
Indicators at the front of the crate	no	"U"	"U"	"U" "E"	"U" "E"	"U" "E"

[1] no allowance being made for projecting parts of connectors, handle for 8-slot crate

Structural characteristics	**LTR-U (LTR-CU, LTR-CEU)**			**LTR-EU**		
	Design version			**Design version**		
	LTR-U-1-4 (LTR-CU-1-4, LTR-CEU-1-4)	**LTR-U-8-1 LTR-U-8-2 LTR-U-8-3**	**LTR-U-16-1 LTR-U-16-2 LTR-U-16-3**	**LTR-EU-2-5**	**LTR-EU-8-1 LTR-EU-8-2 LTR-EU-8-3**	**LTR-EU-16-1 LTR-EU-16-2 LTR-EU-16-3**
Indicators on the rear of the crate	"U" (LED, Activity, Link)	no (**LTR-U-8-1**) "~220V", "=12V" (**LTR-U-8-2**) "~220V", "=27V" (**LTR-U-8-3**)	no (**LTR-U-16-1**) "~220V", "=12V" (**LTR-U-16-2**) "~220V", "=27V" (**LTR-U-16-3**)	No	No	No
Connectors at the front of the crate	37-pin DB-37M plug in the number corresponding to the number of installed modules					
Connectors on the rear of the crate:	**Connector type**					
– "~220 V"		AC-1	AC-1		AC-1	AC-1
– Low-voltage external power supply connector	DJK-02A	No (**LTR-U-8-1**) BPD-1 terminal (**LTR-U-8-2, LTR-U-8-3**)	No (**LTR-U-16-1**) BPD-1 terminal (**LTR-U-16-2, LTR-U-16-3**)	DJK-02A	No (**LTR-EU-8-1**) BPD-1 terminal (**LTR-EU-8-2, LTR-EU-8-3**)	No (**LTR-EU-16-1**) BPD-1 terminal (**LTR-EU-16-2, LTR-EU-16-3**)
– "USB"	DUSB-BRA42-T11					
– "Ethernet""	No (74990112116A)	no	no	RJ-45	RJ-45	RJ-45
– External synchronization connector	AUB-33 (MDN-9M(P))	no	no	no	MDN-9M(P)	MDN-9M(P)

Structural characteristics	LTR-U (LTR-CU, LTR-CEU)			LTR-EU		
	Design version			Design version		
	LTR-U-1-4 (LTR-CU-1-4, LTR-CEU-1-4)	**LTR-U-8-1 LTR-U-8-2 LTR-U-8-3**	**LTR-U-16-1 LTR-U-16-2 LTR-U-16-3**	**LTR-EU-2-5**	**LTR-EU-8-1 LTR-EU-8-2 LTR-EU-8-3**	**LTR-EU-16-1 LTR-EU-16-2 LTR-EU-16-3**
Grounding terminal	The grounding connector is defined on the external synchronization connector (grounding terminal on the rear panel)	BP-9B (**LTR-U-8-1**) BP-3B (**LTR-U-8-2, LTR-U-8-3**)	BP-9B (**LTR-U-16-1**) BP-3B (**LTR-U-16-2, LTR-U-3**)	BP-9B	BP-9B (**LTR-EU-8-1**) BP-3B (**LTR-EU-8-2, LTR-EU-8-3**)	BP-9B (**LTR-EU-16-1**) BP-3B (**LTR-EU-16-2, LTR-EU-16-3**)
Reset button	No (is located on the rear panel)	No		On the rear panel	On the front panel	On the front panel
Ventilation system	Passive	Internal fans	Internal fans	Internal fan	Controlled adaptive internal ventilation with temperature and fan speed control	Controlled adaptive internal ventilation with temperature and fan speed control

Note: in the Table , the types of block parts of connectors are indicated.

3.2 Description of crate panels and connectors.

3.2.1 LTR-U-8-1 and LTR-U-16-1

The front view of LTR-U-8 (Fig. Fig. 3-1) and LTR-U-16 (Fig. 3-2) crates (-1,-2,-3 depending on additional design version number)[1]is visually similar.

To the left of slot 1, a panel is mounted with a single **two-color LED indicator which shows the status of connection via the USB interface**:

- Continuous green glowing means a *high-speed* connection via the USB interface.
- Continuous red glowing means a connection via the full-speed interface.
- If the indicator is off, this indicates that the crate is off.

These are the main statuses of the indicator programmed by the crate controller. For complete information about the indicator status, refer to the Programmer's Manual[1].

On the rear panel of LTR-U-8-1 and LTR-U-16-1 crate there are:

- grounding terminal;
- connector for connecting the network cable ~ 220V (the network cable is supplied with the crate, see paragraph 2.4);
- network power unit switch;
- connector for connecting the USB cable (the USB cable is supplied with the crate, see paragraph 2.4);
- power supply unit fan grill;
- factory label with the crate name, serial number and year of manufacture.
- Types of connectors and names of internal structural elements of the crate are specified in table 3-1.

The appearance of the rear panel may vary slightly, depending on the location of the components of the standard PC power supply used in these crates.

[1] The crate designation system is described in paragraph 2.3.1, page 13.

3.2.2 LTR-U-8-2, LTR-U-8-3, LTR-U-16-2, LTR-U-16-3

The front view of LTR-U-8 (Fig. Fig. 3-1) and LTR-U-16 (Fig. 3-2) crates (-1,-2,-3 depending on additional design version number)[1]is visually similar.

To the left of slot 1, a panel is mounted with a single **two-color LED indicator which shows the status of connection via the USB interface**:

- Continuous green glowing means a *high-speed* connection via the USB interface.
- Continuous red glowing means a connection via the full-speed interface.
- If the indicator is off, this indicates that the crate is off.

These are the main statuses of the indicator programmed by the crate controller. For complete information about the indicator status, refer to the Programmer's Manual[1].

On the rear panel of LTR-U-8-2, LTR-U-8-3, LTR-U-16-2, LTR-U-16-3 crates there are

- nominally separated low-voltage and high-voltage power supply sections, each one having its own power switch, LED indicators, connectors for connecting ~ 220 V in the high-voltage section and "+" and "-" terminals for low-voltage power supply (= 12V in **LTR-U-8-2, LTR-U-16-2** crates or =27 V **in LTR-U-8-3, LTR-U-16-3 crates).** Network cable ~220 V is supplied with the crate, see paragraph 2.4.
- grounding terminal;
- connector for connecting the USB cable (the USB cable is supplied with the crate, see paragraph2.4);
- power supply unit fan grill;
- factory label with the crate name, serial number and year of manufacture.
- Types of connectors and names of internal structural elements of the crate are specified in table 3-1.

Table 3-2. Statuses of power indicators located on the rear panel of LTR-U(EU)-8(16)-2(3) crates

Indicator ~220V	Indicator =12V(=27V)	Status
○	○	Off
●	○	Powered from network ~220 V
○	●	Powered from low-voltage source =12 V (=27 V)
○	●	Low-voltage source is connected, but its voltage is insufficient to turn on the power supply
●	●	220 V network and low voltage sourse 12 V (= 27 V) are connected simultaneously. In this state, power for powering the LTR crate is supplied from ~ 220 V network

3.2.3 LTR-EU-8 and LTR-EU-16

The front view of these crate is only different from the appearance of LTR-U-8 (Fig. Fig. 3-1) and LTR-U-16 crates (Fig. 3-2) with the front panel design (to the left from the 1st slot)

[1] The crate designation system is described in paragraph 2.3.1, page 13.

having **"U"**USB interface status indicator, **"E"** Ethernet interface status indicator, and "R" hidden reset button[1]**.**

"U" indicator statuses:

Green glowing means a *high-speed* connection via the USB interface.

Red glowing means a connection via the *full-speed* USB interface.

Continuous yellow-and-orange glowing means that there is no connection via the USB interface.

"E" indicator statuses:

Green glowing means that there is Ethernet connection (link) on the physical level.

Red Ethernet glowing means that there is no Ethernet connection on the physical level (probable cause: the cable is not connected).

If both **"U" and "E"** indicators went off, this means, under normal conditions, that the crate is off (de-energized).

In case that the indicators are off when the crate is on, contact the support team of L-Card.

These are the main statuses of the indicators programmed by the crate controller. For complete information about the indicator status, refer to the Programmer's Manual[1].

"R" reset button has two functionalities:

- *short pushing* (for less than 1s) leads to the *normal* initial processor boot-up mode;
- *long pushing* (for more than 10 s, or earlier than in 10 s after the crate is powered on) calls *the alternative* processor boot-up mode.

In LTR-EU Board Version ≠ 0 (paragraph 4.4.1) crate controllers, the watchdog timer is disabled in the *alternative processor boot-up mode* so that it does not interfere with the use of JTAG emulator (paragraph 20.3).

For software aspects of the *boot-up modes*, refer to the Programmer's Manual[1].

On the rear panel of LTR-U-8-1 and LTR-U-16-1 crates there are:

- grounding terminal;
- connector for connecting the network cable ~ 220V;
- network power unit switch;
- connector for connecting the USB cable (the USB cable is supplied with the crate, see paragraph 2.4);
- connector for connecting the Ethernet cable (*category 5e*);
- "SYNC" synchronization connector
- power supply unit fan grill;
- factory label with the crate name, serial number and year of manufacture.

[1]sunken button, not protruding above the panel surface

- Types of connectors and names of internal structural elements of the crate are specified in table 3-1.

SYNC connector has two digital inputs DIGIN1 and DIGIN2, two digital outputs DIGOUT1, DIGOUT2, three digital grounding contacts GND, two 3.3 V external device power outputs (fig. 3-5). In all LTR-EU crates, this connector has the same contact assignment and pinout.

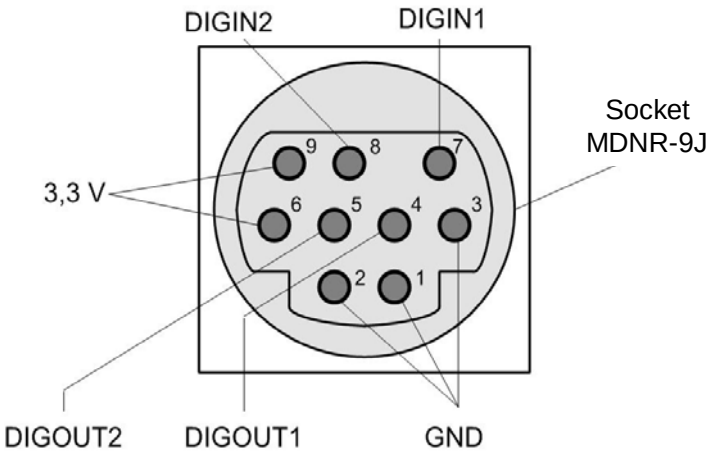


Fig. 3-5. SYNC connector of LTR-EU, LTR-CU, LTR-CEU crates

Table 3-3. Synchronization signals of LTR-EU crates

Signal	Signal type	Signal description
DIGIN1	TTL digital input	Input with programmable crate synchronization or general-purpose digital input functions
DIGIN2	TTL digital input	Input with programmable crate synchronization or general-purpose digital input functions
DIGOUT1	TTL digital output with Z-state	Output with programmable crate synchronization or general-purpose digital output functions
DIGOUT2	TTL digital output with Z-state	Output with programmable crate synchronization or general-purpose digital output functions

For more details on connection, see paragraph 3.6.9, page 61.

On the rear panel of LTR-EU-8-2, LTR-EU-8-3, LTR-EU-16-2, LTR-EU-16-3 crates there are

- nominally separated low-voltage and high-voltage power supply sections, each one having its own power switch, LED indicators, connectors for connecting ~ 220 V in the high-voltage section and "+" and "-" terminals for low-voltage power supply (= 12V in **LTR-EU-8-2, LTR-EU-16-2** crates or =27 V **in LTR-EU-8-3, LTR-EU-16-3 crates).** Network cable ~220 V is supplied with the crate, see paragraph 2.4.
- grounding terminal;
- connector for connecting the USB cable (the USB cable is supplied with the crate, see paragraph 2.4);
- connector for connecting the Ethernet cable (*category 5e*);

- "SYNC" synchronization connector (fig. 3-5).
- power supply unit fan grill;
- factory label with the crate name, serial number and year of manufacture.
- Types of connectors and names of internal structural elements of the crate are specified in table 3-1.

Read about new functionalities of LTR-EU crates in paragraph 4.4.1.

3.2.4 LTR-U-1-4

The front view of a single-slot crate is shown on fig. 3-3.

The front panel of LTR-U-1-4 [1]crate serves as the front panel both for the crate and the LTR module and has only one LTR module connector corresponding to the first slot of the LTR module.

On the rear panel of LTR-U-1-4 crate there are:

- connector for connecting the USB cable (the USB cable is supplied with the crate, see paragraph 2.4);
- synchronization connector (the cable part of the synchronization connector is supplied with the crate, see paragraph 2.4), fig. 3-6. *SYNC INPUT synchronization signal is transmitted directly to ARM crate controller interruption input* (paragraph 4.3)
- external power connector = 12-24V (~ 220 V network card and spare cable part of the power connector are supplied with the crate, see paragraph 2.4), fig. 3-6.
- LED indicator

LED indicator status:

● Continuous or pulsed red glowing means that there is a full-speed connection via the USB interface.

○ If the indicator is off, this indicates that the crate is off.

These are the main statuses of the indicators programmed by the crate controller. For complete information about the indicator status, refer to the Programmer's Manual[1].

Factory label with the crate name, serial number and year of manufacture is underneath the frame.

Types of connectors and names of internal structural elements of the crate are specified in table 3-1.

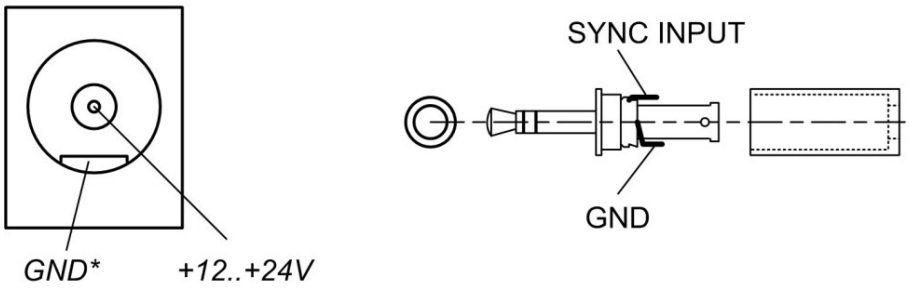


Fig. 3-6. LTR-U-1-4 crate external power supply and and synchronization connector

[1] structural designation: LTR021-U-1 panel

3.2.5 LTR-EU-2-5

The front view of the crate is shown on fig. 3-4.

The front panel of LTR-EU-2-5[1] crate serves as the front panel both for the crate and the LTR module and has the connectors of two LTR modules on it. The upper connector corresponds to the first module slot in the crate. On the front panel, there are also "U" and "E" crate status indicators:

"U" indicator statuses:

- Green glowing means a *high-speed* connection via the USB interface.
- Red glowing means a connection via the *full-speed* USB interface.
- Continuous yellow-and-orange glowing means that there is no connection via the USB interface.

"E" indicator statuses:

- Green glowing means that there is Ethernet connection (link) on the physical level.
- Red Ethernet glowing means that there is no Ethernet connection on the physical level (probable cause: the cable is not connected).
- If both **"U" and "E"** indicators went off, this means, under normal conditions, that the crate is off (de-energized).
  In case that the indicators are off when the crate is on, contact the support team of L-Card.

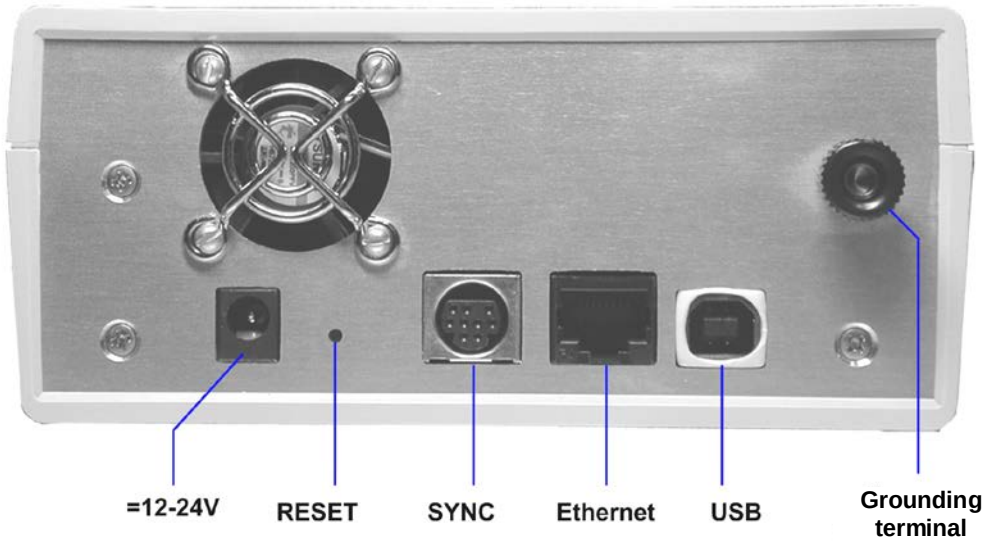


Fig. 3-7. Rear panel of LTR-EU-2-5 crate

[1] structural designation: Panel: LTR-EU-2

On the rear panel of LTR-EU-2-5 crate there are:

- connector for connecting the USB cable (the USB cable is supplied with the crate, see paragraph 2.4);
- connector for connecting the Ethernet cable (*category 5e*);
- synchronization connector (the cable part of the synchronization connector is supplied with the crate, see paragraph 2.4), the connector description is presented on fig. 3-5, table 3-3
- external power connector = 12-30V (~ 220 V network card and spare cable part of the power connector are supplied with the crate, see paragraph 2.4);
- fan grill;
- crate grounding terminal;
- "R" reset button.

The reset button has two functionalities:

- Short pushing (for less than 1s) leads to the normal initial processor boot-up mode;
- Long pushing (for more than 10 s, or earlier than in 10 s after the crate is powered on) calls the alternative processor boot-up mode.

! In LTR-EU Board Version ≠ 0 (paragraph 4.4.1) crate controllers, the watchdog timer is disabled in the *alternative processor boot-up mode* so that it does not interfere with the use of JTAG emulator (paragraph 20.3).

For software aspects of the *boot-up modes*, refer to the Programmer's Manual[1].

SYNC connector has two digital inputs DIGIN1 and DIGIN2, two digital outputs DIGOUT1, DIGOUT2, three digital grounding contacts GND, two 3.3 V external device power outputs. In all LTR-EU crates, this connector has the same contact assignment and pinout (fig. 3-5, page 43).

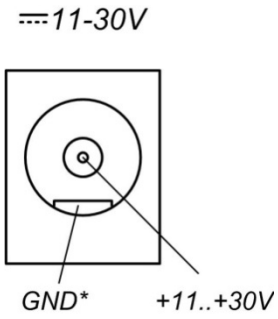


Fig. 3-8. External power supply connector of LTR-EU-2-5 crate

Factory label with the crate name, serial number and year of manufacture is underneath the frame.

Types of connectors and names of internal structural elements of the crate are specified in table 3-1.

Read about new functionalities of LTR-EU crates in paragraph 4.4.1.

3.2.6 LTR-CU-1-4 and LTR-CEU-1-4.

The front view of a single-slot crate is the same, including the marking fig. 3-3.

The front panel of LTR-CU-1-4 and LTR-CEU-1-4 crates serves as the front panel both for the crate and the LTR module .

A schematic view of the rear panels is shown on fig. 3-9, fig. 3-10. On the panels there are:

- crate grounding terminal ⏚;
- LAN connector for connecting the Ethernet cable *(category 5e)* (the LAN connector is available only in LTR-CEU-1-4 and is supplied together with the cable in the scope of supply of the crate, see paragraph 2.4*)*; on the LAN connector, there are Link and Activity indicators showing the status of Ethernet connection as shown in fig. 3-10;
- SYNC synchronization connector (the cable part of the synchronization connector is supplied with the crate, see paragraph 2.4), the connector description is presented on fig. 3-5, table 3-3.
- external power connector = 11-24V, the connector pinout is shown on fig. 3-11(~ 220 V network card and spare cable part of the power connector are supplied with the crate, see paragraph 2.4);
- RESET button;
- connector for connecting the USB cable (the USB cable is supplied with the crate, see paragraph 2.4);
- LED indicator of USB interface status.

Crate LED indicator statuses:

Green glowing means a *high-speed* connection via the USB interface. Blinking green glowing can be observed during the data transmission.

Red glowing means a connection via the *full-speed* USB interface.

Continuous yellow-and-orange glowing means that there is no connection via the USB interface.

If the indicator goes off, this means that the crate is powered off.

Statuses of the indicators on the LAN network:

Yellow glowing of the Link indicator means that there is a connection on the physical Ethernet level.

The Activity indicator glows green during the data transmission.

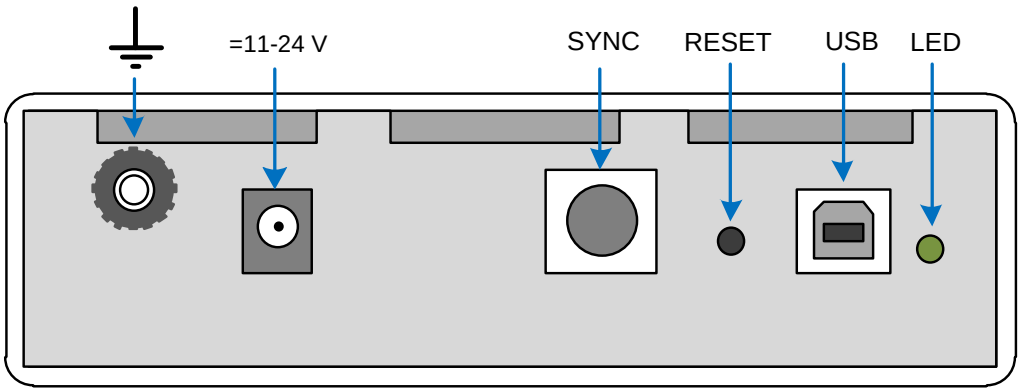


Fig. 3-9. Rear panel of LTR-CU-1-4 crate

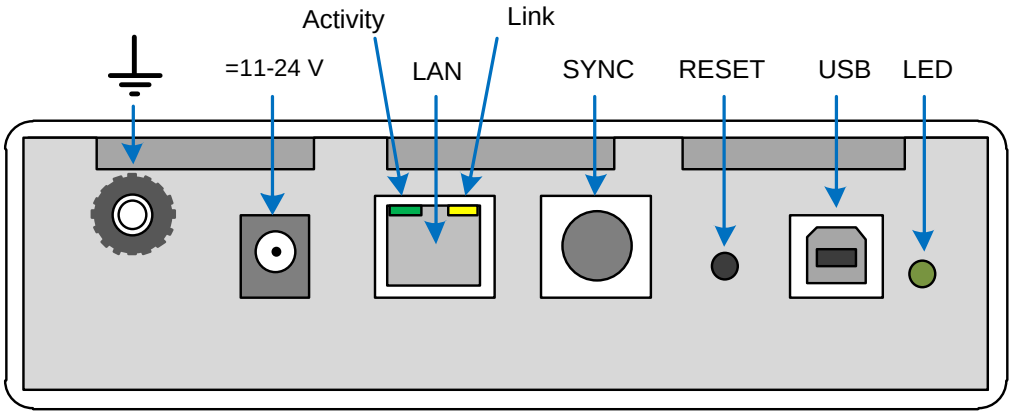


Fig. 3-10. Rear panel of LTR-CEU-1-4 crate

The type, pinout and contact assignment of SYNC synchronization connector corresponds to the similar connector of LTR-EU crates according to fig. 3-5 and table 3-3 on page 43.

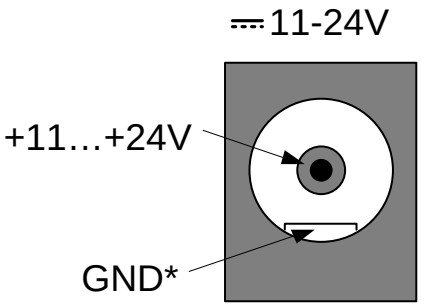


Fig. 3-11. External power supply connector of LTR-CU-1-4, LTR-CEU-1-4 crates

3.3 Ventilation in LTR crates.

In LTR-U-1-4, LTR-CU-1-4, LTR-CEU-1-4 crates, passive ventilation is used. Ventilation openings are located at the bottom of the crate frame and on its front and rear panels.

In 2-, 8- and 16-slot crates, active ventilation is used. The air is drawn from the crate bottom by internal fans and is discharged from the back of the crate through the crate power supply unit.

In LTR-EU-8 and LTR-EU-16 crates, adaptive ventilation system is used with automatic temperature control inside the crate and crate fan speed control. This system helps to reduce the noise generated by crate fans and increase the service life of the fans.

3.4 Information about the LTR modules design

Structurally, all LTR modules are a 134x102 mm PCB with a FRN1L panel screwed to it (for example, fig. 5-1). On the module panel there is DB-37M user signal connector. There is a handle on the bottom. A label with the module designation is glued on the module handle.

FRN1L panel has a lower and an upper fixing screws for fixing the module when mounted into the crate.

The LTR module panel also has an electrostatic grounding tab on the inside that comes into contact with the crate frame only if the panel fastening screws are tightened. In 8- and 16-slot crates, re-arrangement of LTR modules is relatively simple (for details, refer to paragraph 3.6.2).

It should be noted that when LTR modules are installed in LTR-U-1-4, LTR-EU-2-5 and LTR-CU-1-4, LTR-CEU-1-4 crates, the standard panel of FRN1L module is not used, and its functions are performed by the front panel of these crates (for LTR210, a special panel is used which is always taken into account when ordering). It is meant that a quite complicated operation for installing the module inside LTR-U-1-4, LTR-EU-2-5, LTR-CU-1-4 and LTR-CEU-1-4 crates should be carried out by the manufacturer in the crate production process. However, in case of accurate handling and having appropriate skills, the user may carry out the operation for re-arrangement of modules in the crate by his own efforts (for details, refer to paragraph 3.6.2).

3.5 Serial number

L-Card serial number is used for products identification and traceability at all production, -operation *and repair* stages- which has the following form:

2C425775 (a digit– a letter – a six-digit number)

Serial number (s/n) is applied to the crate and modules by printing method and, in addition, s/n can be accessed by the user in the software. At the production stage, it is hardwired into the non-volatile memory of the crate controller and modules. It is accessible for users *only for reading* through library functions. *UTS* software supplied with the crate (paragraph 2.4, page 29), shows the serial numbers of the modules and LTR- server software shows the serial numbers of the crate.

When contacting L-Card's support team with a technical question regarding any purchased L-Card product, always indicate its *serial number*. This will enable the specialist to obtain the necessary additional information about this product.

! The first digit in the serial number is *the number of the product version* related to the hardware of this product. In special cases, if a new version of the same product is updated with functional (electrical) differences essential to the user, the relevant information will be introduced in *this manual* with reference to the version number of the product.

Do not confuse the number of the product version with the firmware versions of these products (paragraph 3.8, page 63) as these concepts are different and in most cases independent from each other. Read about serial number reading by software In the Programmer's Manual[1].

3.6 LTR crate installation and connection

3.6.1 Installation of LTR crates

The crate position shown in fig. 3-1 – fig. 3-4 is a normal position for installation on a Table.

! When installing the LTR crate, be sure to ensure that there is free inflow of air into the bottom of the crate and that there is free air outflow from the rear side of the crate!

For installation on a Table, crate is supplied with rubber stubs.

16-slot LTR crate can be installed in a 19" rack but for this you may need to remove the plastic panels from the side walls of the rack frame.

2-slot crates (starting from those manufactured in August 2016) can be installed on a DIN-rail with the use of additional accessory DIN-LTR2 (for details, visit http://en.lcard.ru/products/accesories/din-ltr2).

! To ensure proper air circulation, LTR-EU-2-5 should be installed on DIN rail only with the fan grill up!

3.6.2 Installation of modules into a crate

Usually LTR crates are supplied with pre-installed modules but if you need to change the configuration of the modules in the crate, then (in case of 8- and 16-slot crates) you can do it yourself (for more details, refer to paragraph 3.6.2.1).

! Modules are installed into LTR-U-1-4, LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4 crates by the manufacturer in accordance with the order. Changing the configuration of these crates by the user is complicated (paragraph 3.6.2.2). When ordering any configurations of these crate which include LTR43 or LTR51 modules, do not forget to specify the jumpers status (see, respectively, paragraph 8.4, page 148, and paragraph 10.2, page 166). When ordering LTR212M-1, if a mezzanine board with user complementary quarter-bridge resistors is to be used, it should also be taken into account that installation of a mezzanine board can be difficult for the user (paragraph 3.6.2.2) in LTR-U-1-4, LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4 crates.

3.6.2.1 Changing the configuration of modules in a 8-slot or 16-slot crate.

Before the mechanical re-arrangement of the modules, turn off the power using the switch on the rear side of the LTR crate, then disconnect all external connections of the module and carefully unscrew the upper and lower screws on the front module panel and perform its rearrangement.

Install LTR modules carefully, strictly along the crate guides. Prior to the installation, make sure that the contacts of the module interface connector are not damaged or contaminated. After the installation, tighten both panel fixing screws.

! It is forbidden to install in the crate (or remove from it) a LTR module with a connected user connector.

Do not operate a LTR module with loose fastening screws on the front panel of the module. Also check that the hexagon -screws on the front panel of the module are tightened.

Only when the screws of a LTR module are tightened, the electrostatic capacitance circuit of the galvanic isolation of the module is in contact with the crate frame, which ensures the sTable operation of the LTR[1] *module*.

3.6.2.2 Changing the configuration of modules in LTR-U-1-4, LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4 crates

LTR modules are installed in LTR-U-1-4, LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4 crates by L-Card according to the order. This can be considered as a very strong manufacturer's recommendation not to disassemble these crates by yourself for the following reasons:

- L-Card will assemble and test the final product properly, which you are certainly interested in.
- In general, L-Card, as the manufacturer, shall be warranty liable only if these crates are assembled by L-Card.
- In case of defects and malfunctions related to incorrect and inappropriate product assembly, the warranty liability of L-Card for this product shall be terminated.

However, if the above arguments still do not make you doubtful, you have the appropriate skills and are able to disassemble, change the LTR module board and re-assemble it again properly, then we assume that this option is is conditionally possible for you. When doing this, observe the following rules:

- Proceed to crate disassembly only after turning it off and checking that the cable parts of the crate connectors are completely disconnected.
- The top and bottom crate covers are disassembled by unscrewing the 4 self-tapping screws connecting the frame covers.
- For LTR-U-1-4 (LTR-CU-1-4, LTR-CEU-1-4) crates, the LTR module must be disconnected from LTR021 (LTR021U, LTR021M) crate controller board. For LTR-EU-2-5, the couple of LTR modules are disconnected from LTR031C motherboard simultaneously. Attention! At once remember the correct factory orientation of the LTR module relatively to LTR021 (LTR031C), since there is no allowed alternative way to install the LTR module in these boards connector (the connectors do not have a key for unambiguous installation).
- The front panel is disconnected from the LTR module by unscrewing the pair of hexagonal screws from the outside of the panel, as well as the pairs of screws at the corners of the LTR module board.
- Having replaced the LTR module boards, conduct the further assembly in the order reverse to the order of disassembly. Prior to the installation of the top frame cover, *check if all the split pairs are properly joined*.
- The LTR crate may only be powered on after its assembly is complete.

[1] A responsible user can check with the multimeter the contact of the metal fringe of the connector (type DRB-37M) on the front panel of the module installed in the crate with the crate grounding terminal (located on the rear side of the crate)

3.6.3 Specific issues of LTR crates connection

Below we will consider the specific issues of connecting LTR crates without going into particulars of an individual LTR module connection (these issues are dealt with in detail in the chapters devoted to the corresponding module).

General rules of signals connection in the LTR crate system are set forth in paragraph 3.6.6 on page 58.

General rule: In LTR crates having a low-voltage power input, the polarity of the voltage source connection indicated on the panel must be observed and the maximum permissible voltage must not be exceeded. Otherwise, the crate power supply unit may fail!

3.6.3.1 Connection of 8- and 16-slot LTR crates of all design versions

When connecting these crates, it should be taken into account that the common wire of the USB interface is galvanically connected inside the crate with the frame and the grounding terminal of the crate, and also connected to the grounding tab of the mains plug. From this, important warnings immediately follow:

Do not connect or disconnect the network power cable when the USB cable is connected to the computer. Otherwise, by discharging the network filters you can damage the USB ports of the LTR crate and your computer

Table 3-4. Input voltages of low-voltage power supply in 8- and 16-slot LTR crates

Crate	Input voltage of low-voltage power supply	
	operating	limit
LTR-U-8-2 LTR-U-16-2 LTR-EU-8-2 LTR-EU-16-2	+(11 …15) V	+22 V
LTR-U-8-3 LTR-U-16-3 LTR-EU-8-3 LTR-EU-16-3	+(22…30) V	+33 V

In 8- and 16-slot crates, it is not recommended to break the low-voltage supply circuit of the crate "on the run" (when the low-voltage power section of the crate is switched on). Turn off the low-voltage power supply section at the rear side of the crate before disconnecting the low-voltage supply terminals of the LTR crate.

The operating range of the line supply voltage for 8- and 16-slot LTR crates is (220±20) V 50 Hz.

For recommendations on connecting to the computer via USB and Ethernet, refer to sub-paragraph 3.6.4, 3.6.5.

3.6.3.2 Connection of LTR-U-1-4 crate

When connecting LTR-U-1-4 crate, consider the maximum permissible conditions for SYNC INPUT signal and the external power input of the crate (table 3-5).

Table 3-5. LTR-U-1-4. Maximum permissible conditions for circuits

Signal	Type	Maximum permissible conditions	Note
SYNC INPUT	Digital input	-0.5...+5.5 V	20 kOhm to zero (to the GND circuit) pull-up resistor
"=12-24V"	External power input	-30V...+25 V relatively to GND*	In case of negative supply voltages, the current in the supply circuit is close to zero (there is diode protection for a case of negative voltage supply) and the crate is switched off
Through-current going through common wires of "USB" – "SYNC INPUT" – "=12-24V" circuits must not exceed 0.1A (fig. 3-12) [1].			

When connecting LTR-U-1-4 to external circuits, consider the internal circuitry for connecting common USB wires, SYNC INPUT and external power input "=12-24V" (fig. 3-12).

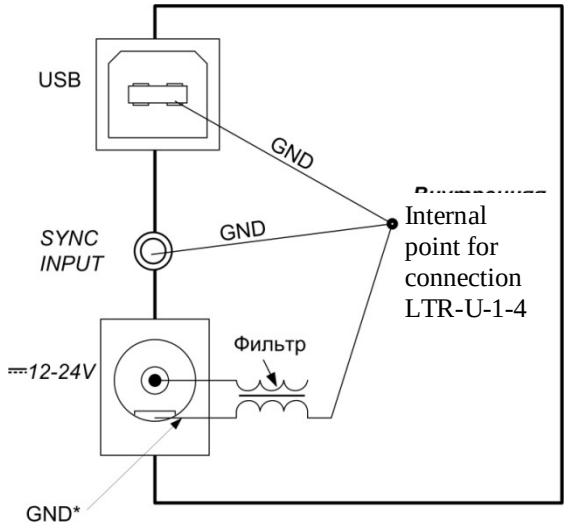


Fig. 3-12. Interconnection of common interface wires in LTR-U-1-4

LTR-U-1-4 crate and the LTR module installed in it go into the *operational state* (paragraph 4.8, page 93) only when the external power source and the USB interface being in the active state are connected simultaneously.

Despite that LTR-U-1-4 crate does not have a separate grounding terminal, GND connector of the cable part of SYNC INPUT connector can be used as the grounding point for the crate (fig. 3-6, page. 44). To improve the noise immunity of the USB interface, it is recommended to connect this grounding circuit to the computer grounding circuit (to the computer case under the screw near its power source, if the computer case has a conductive housing).

[1] If properly connected, this through-current will be close to zero.

The metal casing of the cable part of DB-37F signal connector serves as the signal grounding point and the connection point of the signal screen in LTR-U-1-4 crate. This point must be connected to the screen circuit (signal grounding) of the signal source (sensor).

If LTR212 (M), LTR11, LTR22, LTR24, LTR27, LTR51, LTR114 modules are installed in LTR-U-1-4 crate to reduce the random component of the measurement error, to optimize the signal-to-noise ratio (and also in case of high-noise environment), a screened connection to the signal connector of LTR module must be used. It is recommended to leave the screen (or screens for individual groups of signals) connected only on the side of LTR-U-1-4 crate.

3.6.3.3 Connection of LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4

For recommendations on connecting to the computer via USB and Ethernet, refer to sub-paragraph 3.6.4, 3.6.5.

When connecting LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4 crates, consider the maximum permissible conditions at SYNC synchronization connector and the external power input of the crate (table 3-6).

Table 3-6. LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4. Maximum permissible conditions for circuits

Signal	**Type**	**Maximum permissible conditions**	**Note**
DIGIN1 DIGIN2	Digital input	-6V...+6V	
DIGOUT1 DIGOUT2	Digital output	-0.3V...+5.5V at current below 20 mA	Load current at the output not more than ±40 mA
=11-30V (**LTR-EU-2-5**)	External power input	-0.3…+33V relatively to GND*	No protection against negative power supply
=11-24V (**LTR-CU-1-4, LTR-CEU-1-4**)	External power input	-30V...+25 V relatively to GND*	There is protection against negative power supply
3.3V	Power output	60 mA current relatively to GND	It is highly recommended to avoid a short circuit at this output, since it will cause de-energizing of the entire digital part of the crate (in particular, the processor).
Through-current going through common wires of "USB", "SYNC", "=11-30V (=11-24V)" interfaces and the grounding terminal must not exceed 0.1A (fig. 3-12) [1].			

When connecting LTR-EU-2-5 to external circuits, consider the internal circuitry for connecting common wires of "USB", "SYNC", "= 11-30V" interfaces, grounding terminals and signal connector housings of LTR modules (fig. 3-13). Internal connections in LTR-CU-1-4, LTR-CEU-1-4 are similar fig. 3-13 except for the only one signal connector of the LTR module.

[1] If properly connected, this through-current will be close to zero.

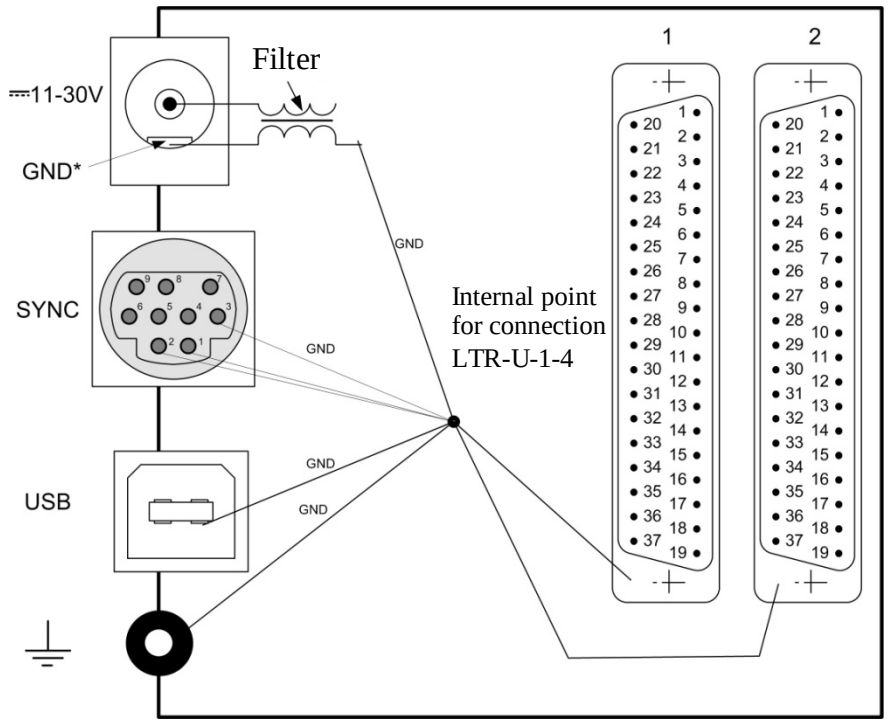


Fig. 3-13. Interconnection of common wires in LTR-EU-2-5

LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4 crates and LTR modules installed in them go into the *operational state* (paragraph 4.8, page 93) only when the external power source is connected regardless of the USB and Ethernet interfaces connection.

LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4 crates have a separate grounding terminal on the rear panel (similar to the other multi-slot crates). To improve the noise immunity of the USB interface (and also to reduce the noise from the external impulse network card), it is recommended to connect this terminal to the grounded computer case (in the case of a conventional computer case, via the grounding tab of the mains plug). In case of Ethernet, it is recommended to connect the grounding terminal to the signal grounding circuit of measuring equipment.

The metal casing of the cable part of DB-37F signal connector serves as the signal grounding point and the connection point of the signal screen in LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4 crates. It is recommended to connect the signal connector housing to the screen circuit (signal grounding) of the signal source (sensor).

If LTR212(M), LTR11, LTR22, LTR24, LTR27, LTR51, LTR210 modules are used to reduce the random component of the measurement error, to optimize the signal-to-noise ratio (and also in case of high-noise environment), a screened connection to the signal connector of LTR module must be used. It is recommended to leave the screen (or screens for individual groups of signals) connected only on the side of LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1 crates.

3.6.4 Connecting a LTR crate to the computer via USB

When connecting a LTR crate to the computer, strictly observe the following rules:

When powered from 220 V network, LTR the crate and the computer system unit must be grounded through the grounding pins of network cable plugs (like the rest system units, where grounding is provided, for example, the monitor). In addition, all these devices must be powered from one network phase. A multi-slot crate system must also have common grounding and a common network phase.

The computer system unit can be connected to the LTR crate via a USB cable and disconnected from it only after the grounding pins of the network cable plugs of these devices are connected to the grounding circuit which ensures that the potentials of the housings of these devices are equalized. Otherwise, the computer and the LTR crate may fail!-

In case that USB is used, the computer and crate grounding circuits must be connected to the grounding bus at one point, or the computer system unit casing must be connected to the crate grounding terminal in the shortest possible way.

A USB 2.0 A-B type cable with a length of up to 5 meters[1] can be used as the USB cable. With the use of active extenders, the total connection length can theoretically be up to 25 meters.

The crate power switch is located on the rear side of the crate. After the above connections are performed, the power switch can be turned on. The manner and color of glowing of the indicator located on the left side of the crate front panel indicates the connection status via the USB interface on the side of LTR crate controller[2].

3.6.5 Connecting a LTR crate to the computer via Ethernet

To connect LTR-EU, LTR-CU-1-4, LTR-CEU-1 crates to the computer via a Ethernet category 5e cable with crimped RJ-45 connectors at the ends, you can use either a straight-through (patch cord) cable or a cross (crossover) cable.

In all LTR-EU, LTR-CU-1-4, LTR-CEU-1 crates, Ethernet interface lines are galvanically isolated from other crate circuits. The galvanic isolation voltage is 500 V.

[1] for the USB standard restrictions, see Universal Serial Bus Specification [21]

[2] Mode details about the indicator statuses can be found in LTR Crate System. Programmer manual [1]

3.6.6 General rules for signal connection in LTR system

The system user shall connect the signals and solder the connectors.

Installation of signal circuits with connection of signal sources, sensors, etc. to LTR crate and modules must be carried out by a qualified specialist.

If the voltage and current supplied to LTR exceed the *permissible limits*, this will lead to the degradation of performance or failure of the LTR system or the connected equipment. **L-Card shall not be responsible for any damages caused by incorrect connection of signals**.

All LTR modules have galvanic isolation of signal circuits from the crate frame and ground. This important property allows to really increase the measurement accuracy when LTR is connected to different signal sources as compared to systems without galvanic isolation[1].

It should noted that no real technical device used for galvanic isolation will not be able to ensure the uninterrupted operation in case of an unlimited rate of noise growth. Proceeding from this, we can formulate the basic rules for LTR connection:

RULE 1. If your signal sources do not have galvanic connection with LTR crate frame, then it is recommended to connect the common wires going from these signal sources to the signal grounding terminal in the shortest possible way. This measure will really limit the rate of noise growth, and, therefore, will in principle ensure the uninterrupted operation of the galvanic isolation.

"So why, then, is the galvanic isolation implemented in the LTR system if I have to ground the galvanically isolated part of this system? I will lose the galvanic isolation if I do so?" This question is very typical for most users and therefore a detailed answer is required:

- Firstly, the main purpose of galvanic isolation is not ensuring the direct current isolation as a goal in itself (except for some rare special cases, see Rule 3) but grounding the galvanically isolated part of the system at a single point being the most optimal grounding point in each case. On the contrary, if the LTR crate was not galvanically isolated, this single grounding point would be inside it and, in this case, any attempt of external grounding would result in more than one grounding point, which is much worse because of generation of through-currents between the grounding points which are actually going through the crate.
- Secondly, we do not force users to ground crates but only recommend this if this is technically possible. The reasons are below:
  - Any isolated circuit of the system is a high-impedance system input relatively to the ground. In order to reduce the noise substantially at such an input, we either have to connect it to the ground in the most low-impedance way, or to screen it (for the screening, see Rule 4).
  - Considering the typical application conditions, the environment in which a LTR crate operates will always be polluted with noise. Even an ordinary computer can become a source of major noise[2].
  - If there is a galvanically isolated part in the system which is isolated from the ground and there are conditions for charge accumulation[3], then an unpredictably large potential can accumulate due to the absence of a path for electrostatic discharge drain to the ground, which will lead to a short breakdown of the galvanic isolation and, almost certainly, to a malfunction of the system (see Rule 2).

[1] for example, if most of modules in a LTR crate had no galvanic isolation.

[2] at least because it can be equipped with a pulsed power supply of unknown origin with an unpredictable level of noise

[3] for example: structural elements rubbing against each other

RULE 2. If there is an essential requirement that the signal sources must be galvanically isolated from the ground and there are factors of charge accumulation, then it is necessary to ensure the path for charge drain to the ground through a high-resistance resistor. Just think, wouldn't it be easier to ground the system?

RULE 3. If it is essential that LTR inputs be galvanically isolated because they are under the potential of a voltage source connected to the ground, it could be suggested, as a noise suppression measure, to ground the potential of the voltage source through a capacitance or a noise suppression filter connected relatively to the crate grounding point.

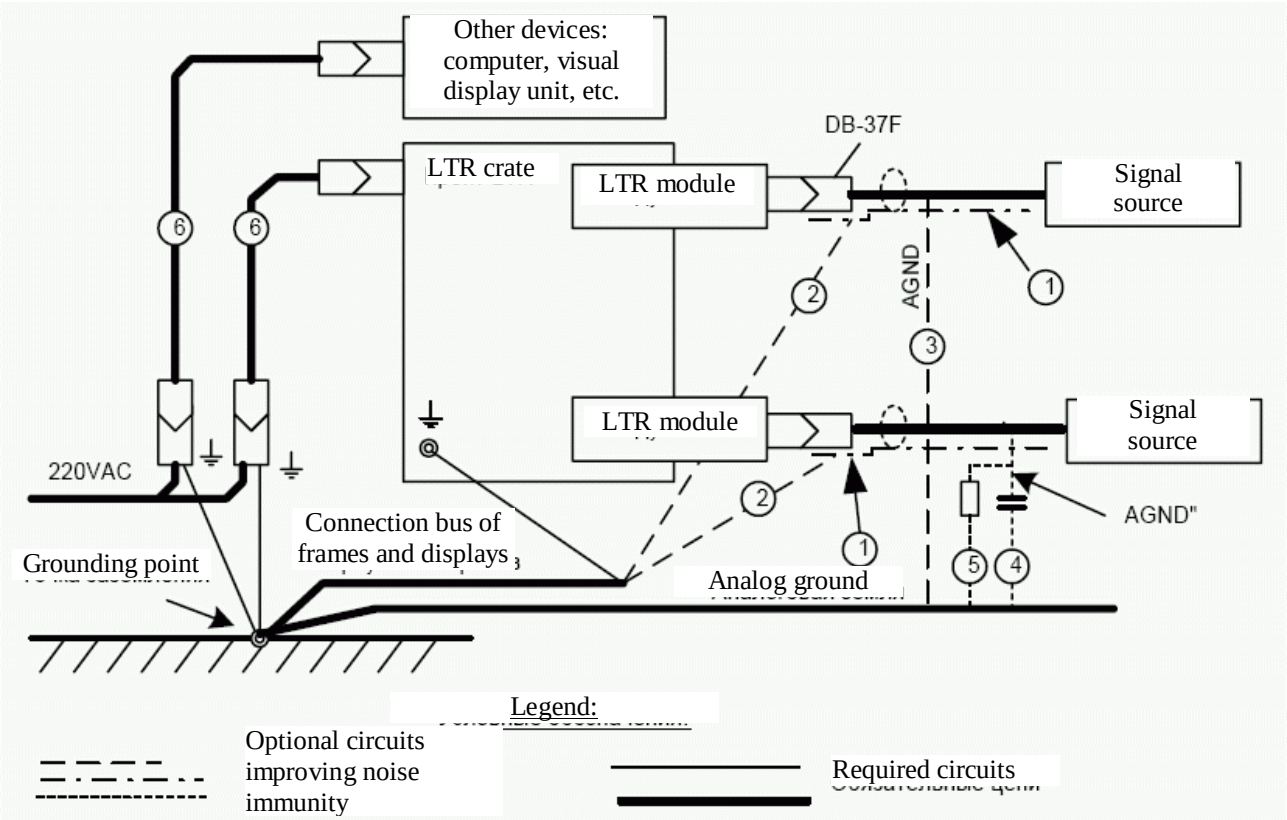
RULE 4. If it is impossible to ground your sources, then they should be screened together with the cables suiTable for the LTR. In this case, it is enough to place the cable in the shield (braid) and solder it to the metal casing of DB37F cable connector-. To avoid through-currents going through the cable braids, do not connect the cable braid to any circuit, except for the direct connection to the crate grounding terminal.

RULE 5. If your signal sources are connected to a LTR module with a long (more than 3...5 m) cable, then in any case it is recommended to use an external screen (see Rule 4).

An illustration of the connection rules is shown in Fig. 3-14.

You may say, *"I didn't ground, didn't screen, and I even don't know how the signal sources are grounded. Everything is still working, and I have no problems."* The answer is: a professional - approach to connectivity issues is based not on waiting for problems, but on minimizing them at the very stage of development of the connection diagram and topology.

For more details on connection of signals to the measuring system and noise suppression, refer to L-Card's specialized article titled "*Solutions of problems related to electro-compatibility and noise protection during connection of measuring equipment through the example of a L—Card* [2] product." Also pay your attention to the following literary sources: [17], [18], [19], [20], [22], [23], [24], [25], [26], [27].



1. If the display is available it should be connected with the frame of DB-37F cable connector
2. Additional measure for display grounding will improve noise immunity
3. Grounding of common wires of signal sources of circuits (AGND) will additionally improve noise immunity Each galvanic isolated part shall have maximum one grounding point!
4. When common wire of signal source is under the potential of external source and it can not be grounded then this can be done by means of high-voltage capacity (through EMC filter capacity)
5. When potential of common wire relative to the ground is not determined and it is impossible to ground the common wire and there are factors of electrostatic charge accumulation, then it is required to provide the drain circuit through high-resistance resistor
6. Network cables of devices having grounding circuit

Fig. 3-14
Generalized LTR connection diagram

3.6.7 Use of terminal block

37-contact board of DB-37F-increaser terminal blocks allows for connecting external signals to the LTR module connector quickly and without using a soldering iron. The permissible wire cross-section is up to 0.75 mm^2. There are openings on the terminal board for mechanical fixing of bundles.

! The terminal board should only be used in case of respective system pre-settings and advanced connections. For normal operation of equipment with the declared metrological characteristics, it is required that external signal circuits be connected with de-soldering of the connector's mating parts.

3.6.8 Connection of an in-phase noise suppression filter

In-phase noise suppression filter is used to prevent failures of LTR crate equipment- in the event of connection to external equipment generating high-speed impulse noise applied relatively to the grounding point of LTR crate frame.

As an option, *LTR -CMF* filter can be used, see the manual [3]. The filter is connected to the user 37-contact LTR- module connector.

3.6.9 Connection of synchronization signals in LTR-EU, LTR-CU-1-4, LTR-CEU-1 crates.

When connecting DIGIN/DIGOUT/GND synchronization circuits to the synchronization connector of these crates (this does not apply to synchronization signals of LTR modules!), it should be taken into account that these crate circuits are not isolated from the frame and the grounding circuit of the crate. It follows from the above that if two LTR- EU crates have different grounding points, then DIGIN/DIGOUT/GND synchronization signals of different crates may not be directly connected, otherwise, *through grounding currents* going through the LTR crate can result not only in unsTable operation of the crate, but also in its malfunction.

Crates synchronization with different grounding points in DIGIN/DIGOUT/GND circuits is only possible in case of use of elements and devices for galvanic isolation which can be powered from the synchronization connector:

1. Optrons.
2. Digital isolators.
3. RS-485/422-UART transceiver cable with galvanic isolation L.[7], page 367. This cable can be used, for example, to receive a second synchronization pulse from the master crate and transmit a second pulse to the next level slave crate.

You can get advice on the details of such connections by e-mail (en@lcard.ru) or in the conference on the web-site en.lcard.ru, having explained the details of your specific task.

3.7 LTR powering on and testing

Strictly observe the rules set forth in paragraph 3.6.4, page 57!

3.7.1 Powering-on and testing with LTR- server

In case of test LTR powering-on, you do not need to connect the connectors of LTR- modules inserted into the crate. Using the CD-ROM (paragraph 2.4, page 29) install LTR software on your computer: drivers, LTR-server and UTS programs.

Ensure in advance that your computer has a USB 2.0 interface (*high-speed*) and that USB 2.0 controller drivers are installed.

Connect the LTR crate to the computer via USB, turn on the LTR crate (if this is the first turning on, the operating system will prompt you to install the LTR driver).

Continuous green glowing of the indicator on the front crate panel indicates that there is a sTable crate connection via USB 2.0.

Run LTR- server software. It will recognize the crate (its serial number will be displayed) and provide the list of LTR -modules installed in the crate.

Turn off the LTR crate and, in a few seconds, turn it on again. LTR- server program must adequately display the hardware turning on and off and correctly display the installed LTR-modules.

Note that LTR- server program has a tab that displays a report about each connection with the LTR- crate.

So, the launched LTR- crate and LTR- server are ready for interaction with any *client*[1] *program* which will work with the crate through the server.

3.7.2 UTS testing

For testing of LTR functionalities, L-Card provides universal demonstration client program UTS (universal test stand).

Install and run UTS. In LTR- menu, select the module to work with. Select the module configuration item and the required settings there. Choose one of the three virtual measuring instruments: oscilloscope, multimeter, or histogram meter. After these steps, the process of data acquisition from the selected module will be started and the data will be displayed by the virtual meter[2].

In more detail, software issues are considered in the document "LTR Crate System. Programmer's Manual"[1].

[1] in the context of the client-server ideology adopted in LTR

[2] note that in some LTR modules, state of unconnected inputs is indeterminate, see the characteristics of the signal line inputs of the corresponding LTR- module

3.8 Updated LTR firmware

In LTR, the following programmable elements are used having the relevant firmware versions which users can update themselves in accordance with the official L-Card updates:

- *Firmware of loaded FPGA of LTR crate controller (if such FPGA is used in this crate, see table 2-2).* The firmware files for loaded FPGA are included in the supplied software package. This firmware configures FPGA *after each crate powering on*. After the successful loading, the computer reads the information line from LTR -crate, containing information about FPGA firmware version, the firmware creation date, and other comments. In particular, TTF_FILE (file name), FpgaVersion, FpgaComment information is displayed by LTR- server program during the LTR- crate boot process after its powering on.
- *LTR crate micro controller (ARM controller, signal processor) firmware (see table 2-2).* LTR crates are supplied with already braided non-volatile controller memory (with Boot Loader function). The version of this firmware (FirmwareVersion) is available in the software. L-Card can, if necessary, release a new version of this firmware (updates are posted on L-Card website). In this case, the user has an opportunity to update the micro controller firmware himself. In particular, LTR server program displays the FirmwareVersion value during LTR- boot- process after its powering on.
- *LTR module micro controller firmware-(see table 3-7).* Similarly to the crate micro controller: the firmware, if necessary, can be updated by the user, updates are posted on L-Card web-site, the version number of the current firmware is available in the software.
- *LTR -module non-volatile FPGA firmware.* Some LTR-modules (for example, LTR51, *see* table 3-7) may have loaded FPGA. This firmware, if necessary, can be updated by the user, updates are posted on L-Card web-site, the version number of the current firmware is available in the software.

The procedure for firmware updating is described in the document "LTR Crate System. - Programmer's Manual"[1].

Do not confuse the number of the product version with the firmware versions of these products (paragraph 3.5, page 49) as these concepts are different and in most cases independent from each other.

Non-volatile CPLD logic chips used in LTR, are only programmed by the manufacturer.

In table 3-7, information is given about the firmware of LTR modules, which the user can update himself in accordance with official updates of L-Card software.

Note also that LTR-EU crate controllers have new hardware differences, see Board Version, paragraph 4.4.1.

Table 3-7. Updated LTR modules firmware

Module	Type of programmable component	User-updaTable firmware
LTR11	Atmega 8515 controller	Yes
LTR22	Atmega 8515 controller	Yes
LTR24 (-1, -2)	CPLD MAXII	No
LTR25	FPGA Cyclone IV	Yes
LTR27	Atmega 8515 controller	Yes
LTR34	CPLD MAX3000A	No
LTR35	FPGA Cyclone III	Yes
LTR41	Atmega 8515 controller	Yes
LTR42	Atmega 8515 controller	Yes
LTR43	Atmega 8515 controller	Yes
LTR51	Atmega 8515 controller	Yes
	FPGA EP1K30	Yes
LTR114	Atmega 128 controller	Yes
LTR210	FPGA Cyclone III	Yes
LTR212(M)	ADSP-2185M signal processor	Yes

3.9 LTR crate operation

When operating LTR crates, the installation and connection requirements must be observed (paragraph 3.6). For permissible environmental conditions, see Appendix A.19, page 362.

! It is inadmissible to power on and operate LTR crates in an environment that does not comply with the operating conditions (Appendix A.19, page 362).

3.9.1 About connection of external signals "on the run"

! In general, failure-free equipment operation after connecting an external connector to a working LTR crate with the wires connected from an external device is not guaranteed.

It's another matter if such *hot cable connection* is desirable, then you can take measures to dramatically reduce the probability of failure with this connection:

- The probability of failure will be small if the connected circuits are pre-grounded.
- The probability of failure will be minimal if the external circuits are connected through an in-phase filter (paragraph 2.4.2, page 32).

If, in principle, you do not need to re-configure the external links of the LTR crate *on the run*, it is *strongly recommended* that you re-connect the cable when a need arises:

- First, turn off the LTR crate using the rear switch.
- Change cable connections observing the recommendations given in paragraph 3.6.2.2, page 52.
- Turn on the LTR crate. After its definition by the LTR- server, application client programs may be run.

3.9.2 Failures and the general ideology of recovery after a failure

Below the general ideology of recovery after a failure is considered, regardless of the reasons for its occurrence.

In systems with continuous operating cycle, as well as in redundant systems, automatic software recovery after a failure of data acquisition/output is usually provided.

Considering the LTR architecture (chapter 4. , page 67), an error theoretically can arise at its - different levels: at the module level, LTR-crate level, and the level of a computer USB-device. In Table 3-8, possible failures are listed (by levels of occurrence) as well as their developments and recovery procedures.

Table 3-8. Failures.

Failure	Failure development	Recovery
LTR module error	An error of index information received from the module is found out (the field of the cyclic data counter is in the format of the data coming from the LTR-module), or a command is received from the LTR- module indicating an error, or LTR -server does not recognize a LTR -module for some time[1]	It is recommended to perform a software restart of this LTR- module (which will take 1-4 s)
Data buffer overflow in LTR crate controller, if the -host computer run out of time to evacuate the data	Data acquisition process stops; at the top software level this information is available through user functions[2]. In this case, the crate indicator will blink. Also check if the USB 2.0 computer controller is in the *high-speed* mode!	Hot (no power-off) re-initialization of the LTR crate controller with FPGA reboot in the crate controller (takes 1-2 seconds), waiting for auto-definition of LTR- modules in the crate (takes about 5 seconds), LTR module software startup-, LTR module setup-, starting data acquisition and data output, when these actions are performed in parallel (simultaneously for each LTR -module which is supported by the system), another several seconds are required for restart of the LTR modules in the crate.
USB- device disappeared from the system	The operating system fixed the disappearance of a USB- device from the system	Full re-initialization of the LTR crate is required after the USB- device definition

3.9.3 Time of LTR modules initialization.

! The initialization time of all LTR modules in the crate will be minimal if these procedure is performed as parallel processes which is basically possible for LTR hardware and software.

[1] LTR server does not recognize a LTR-module for some time which may be the case, for example, if the current protection of this LTR module has tripped in the result of the external over-current on the output lines of the LTR module, which led to the restart of LTR module power supply system.

[2] see LTR Crate System. Programmer manual [1]

Chapter 4. Overview of LTR crate architecture.

If you are reading this manual for the first time, you can skip this chapter.

In it only the information on internal functional (logic) arrangement of LTR crates will be given without considering their design as design issues important for users have been considered before (chapter 3.).

4.1 Basic principles of LTR crate architecture

Unlike the backbone-trunk building principle (which is, for example, used in VME, VXI, PXI), LTR crate does not have a single trunk inside it. LTR crate controller located inside the crate is connected by individual serial channels to LTR modules. Thus, all LTR modules have individual radial connections with the crate controller, and there is no direct connection between the LTR modules.

LTR uses single 32-bit index information format which means that the addressing of the module number in the LTR crate, the channel number, and the command/data attribute are contained in the 32-bit data word format. Due to this, working with information in LTR system is very convenient at all levels of data processing, because, for example, for any 32-bit data word taken from the stream going from LTR modules it is possible to determine the module number and the channel number from which this word has come.

In the first generation of LTR crates with USB interface (named LTR-U -...), crate controller performs the task of simple translation of data and commands between the host computer and LTR modules, addressing these data to the LTR modules and back in accordance with the index information. In addition, crate controller performs the task of data buffering, preventing their loss even in case of significant time of fading of the host computer´s operating system.

LTR module interface uses galvanic isolation elements for data and power circuits.

LTR modules are powered by the power supply (converter) unit installed in their crate.

LTR crate uses a single reference frequency generator (Appendix A.16, page 359) synchronizing the data acquisition in this crate.

In the second generation of LTR crates (named LTR-EU- ...) with Blackfin processor, USB 2.0 and Fast Ethernet interfaces, it became possible, in addition to direct command/data translation via the crate controller, to process part of the commands/data translated to LTR modules and back at the crate controller level which is ensured by high-performance Blackfin processor (type ADSP-BF537). This provides a principal opportunity to solve real-time tasks requiring quick control reactions between LTR modules at the crate controller level. Actually, users of LTR-EU- ... crates are in principle able to use free resources of Blackfin processor for solving their own real-time tasks, having modified L-Card's standard software supplied with LTR-EU crates in accordance with these tasks. That is why the low-level controller description (chapter 20.) is given below for this type of crates; however, this description is addressed only to specialists who want to program a LTR-EU crate at the level of Blackfin processor.

Let us continue considering the arrangement of LTR crates in detail with crates grouping by similar architectures:

For our purpose, LTR-U-8(16) crate group will include LTR-U-8-1, LTR-U-8-2, LTR-U-8-3, LTR-U-16-1, LTR-U-16-2, LTR-U-16-3 crates which are 8- and 16-slot crates with high-speed USB 2.0 interface, ~ 220V network power supply or with a universal ~220/=12V or ~220/=27V power supply (see the designation system in LTR, paragraph 2.3.1).

LTR-U-1-4 crate with USB 2.0 full-speed interface will be set off into a separate group as it has significant differences from LTR-U-8(16) because its architecture is based on ARM processor. It should be noted at once that the resources of this processor are fully used for regular interface tasks and this processor can not be used for additional user functions.

LTR-EU crate group will include LTR-EU-2, LTR-EU-8-1 and LTR-EU-16-1 crates with Blackfin processor, USB 2.0 *high-speed* and Fast Ethernet interfaces.

4.2 Arrangement of LTR-U-8(16) crates

LTR-U-8(16) crate consists of LTR010 crate controller, one or two 8-slot LTR001 motherboards, LTRP1 power supply (LTRP12, LTRP27) and fans. Unlike LTR-U-16, LTR-U-8 crate contains only one motherboard forming slots 1 to 8. In "-1" design versions (the last figure in the designation), crate is equipped with a standard computer network power supply ~220 V with a panel (this structural unit is called "LTRP1 power supply unit"). In "-2" and "-3" design versions, crate is equipped with a universal power supply with an option for crate power supply not only from the 220 V network, but also from a 12 V DC power supply (LTRP12 power supply unit) for "-2" design versions, or from a 27 V DC power supply (LTRP27 power supply unit) for "-3" design versions.

LTR010 crate controller together with LTR001 motherboards performs low-level interface functions between the host computer and LTR modules. In addition, on LTR001 motherboards pulsed power supply units of LTR modules are located with a system of smooth start of power supply at power-up and current protection in the power circuit. LTR001 motherboards also send attributes of presence of a LTR module (in operating *mode*, see 4.8, page 93) in a certain crate slot to the crate controller. These attributes are program-accessible.

As an example, let's consider the general arrangement of LTR-U-8(16) crates .

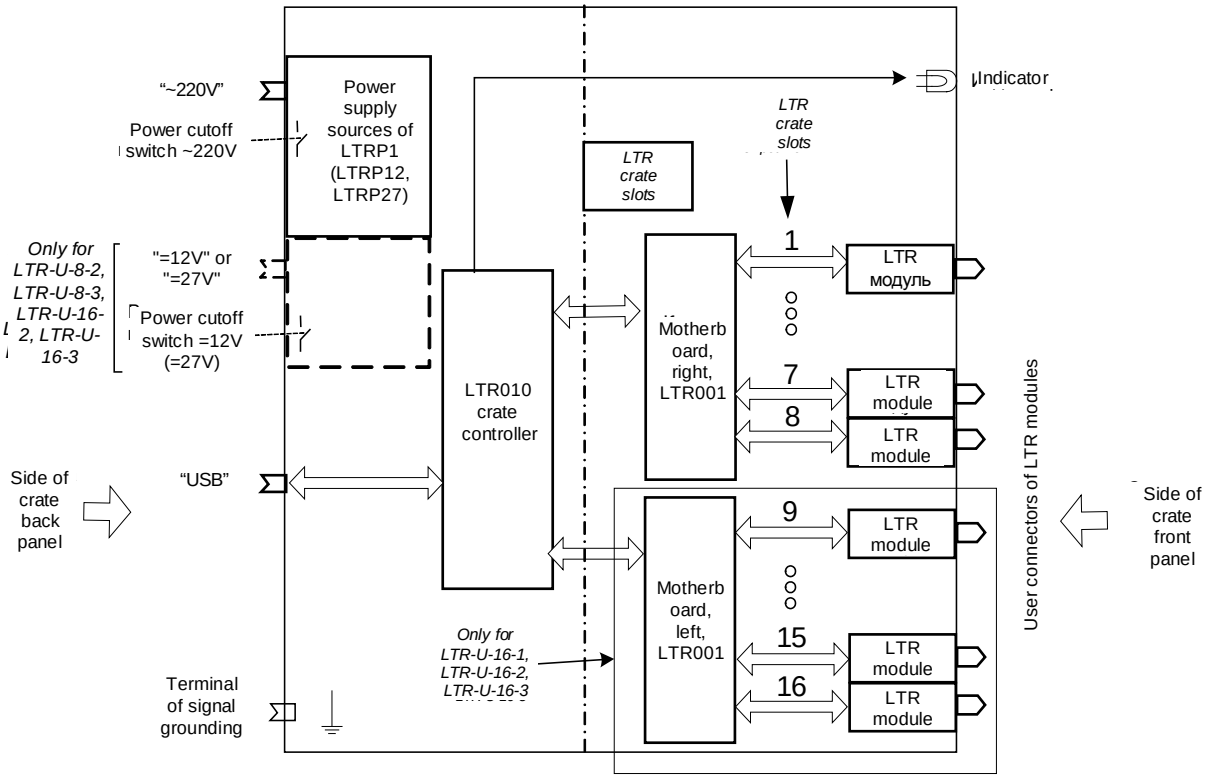
On the front side of the crate, there are slots for LTR-modules 1 to 16 (from left to right) or 1 to 8, and a two-color indicator showing the USB interface status.

In "-1" design version, there is a power supply on the rear side of the crate with a 3-pin connector for 220V network cable, a power switch, a USB cable connector and a signal grounding terminal.

In "-2" and "-3" design versions, on the rear side of the crate there is a universal power supply with a panel conventionally divided into a high-voltage part (~220 V) and a low-voltage part. On the high-voltage part of the panel, the following elements are located: a 3-pin connector for 220V network cable, a power switch, and a crate ~220V network operation indicator. Also, there are a USB cable connector and a signal grounding terminal on the panel.

It should be noted at once that the universal power supply unit (in "-2" and "-3" design versions) does not perform the function of a backup power source, but is only intended for alternative use of power supplies units of the LTR crate, which is convenient, for example, when the same LTR crate is used both in stationary conditions (when powered from ~220 V network) and "off-line" (when powered from a low-voltage power supply).

LTR-U-8-1, LTR-U-8-2, LTR-U-8-3, LTR-U-16-1, LTR-U-16-2, LTR-U-16-3 crates



4.2.1 Arrangement of LTR-U-8(16) crate controller

LTR-U-8-1, LTR-U-8-2, LTR-U-8-3, LTR-U-16-1, LTR-U-16-2, LTR-U-16-3 crates are equipped with LTR010 controller. The crate controller block diagram is shown in fig. 4-1. It contains an AVR micro controller of Atmega162 type, a USB controller of ISP1581 type, FPGA from ACEX1K family, and a SDRAM memory.

AVR micro controller performs general control functions such as:

USB controller programming, support of USB protocol.

Receiving and transmitting information via a USB control channel (Control Pipe).

FPGA programming (FPGA firmware must be loaded with the use of software from the computer when the LTR crate is initialized and each time when the LTR crate is powered on).

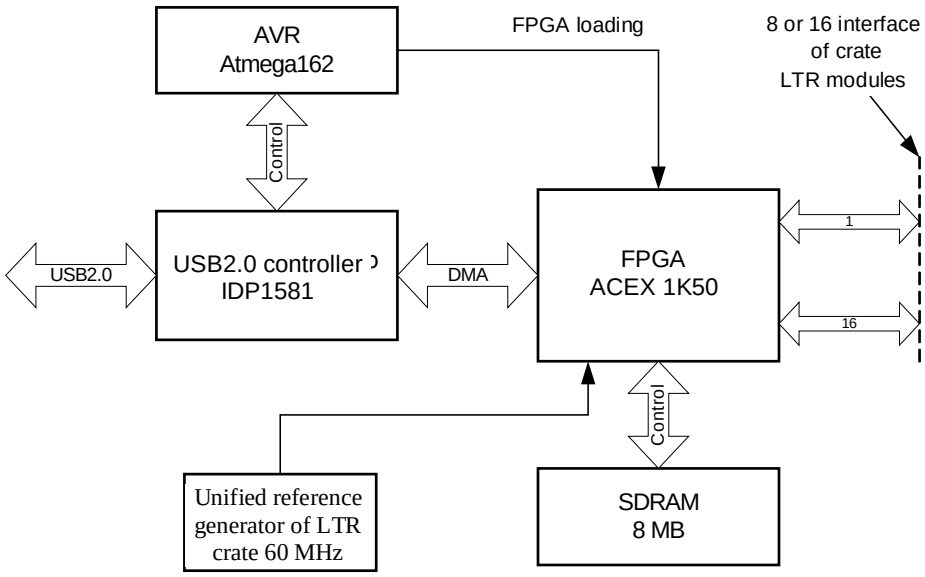
Arrangement of data packets transfer from USB to a FPGA-based buffering system and back.

When the system is started via the USB control channel, FPGA configuration is loaded. After the configuring, FPGA performs the following low-level hardware functions:

Arrangement of data buffering in SDRAM memory (two FIFOs, 4 MB each: one for receiving, the other for transmitting).

Hardware support of DMA protocol for data transmission to ISP1581 and back.
Data transfer and synchronization interface for 16 LTR-modules.

Fig. 4-1. Arrangement of LTR010 crate



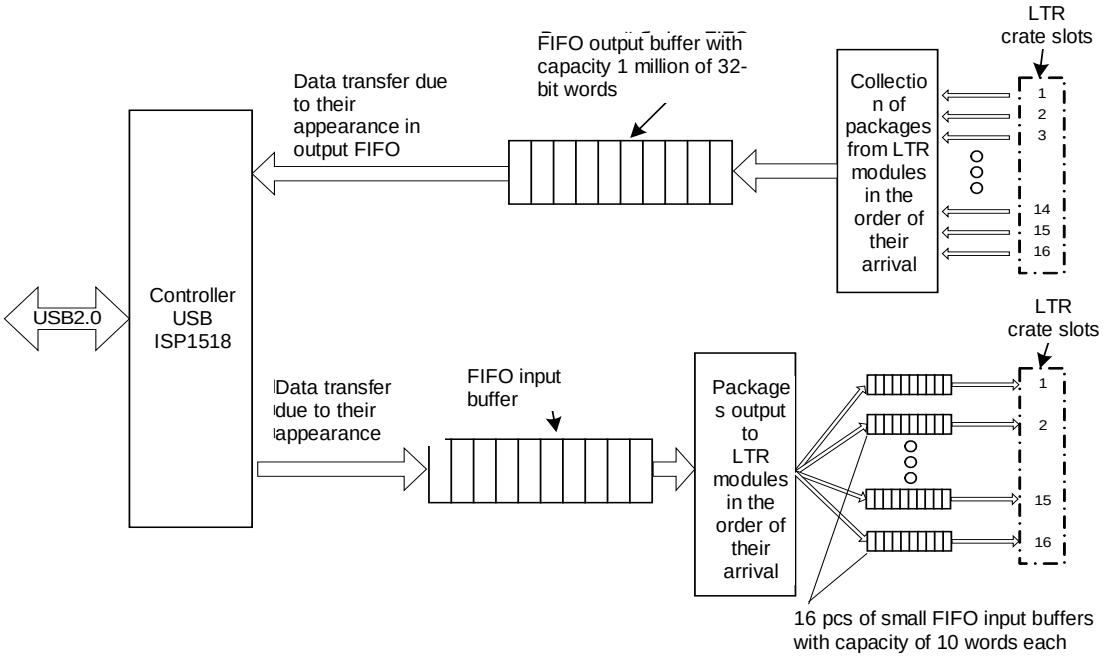


Fig. 4-2. Data paths in LTR010 crate controller

In fig. 4-1. arrangement of ltr010 crate , data paths in LTR010 controller are shown for 16-slot LTR crate (for 8-slot crates, the paths are similar). Data are collected from LTR modules in the order in which they are received. All data obtained from all LTR modules are stored in the form of

32-bit words in a single output FIFO buffer in the order they are received. The hardware provides a linear structure of 32-bit words buffering which means that a word that is received earlier from any LTR module will be the first in the FIFO. This special aspect becomes important when considering the principles of data synchronization in LTR crate (see 4.7, page 91). Essentially, FIFO is necessary for ensuring the continuity of the data flow in conditions of possible short-term fading of the computer's operating system.

The data flow going to LTR modules is buffered in a single input FIFO, and then the hardware, sequentially selecting data from it, fills 16 small input FIFOs as they are emptied. In turn, the hardware sends the information from small input FIFOs with the speed determined by the interface of LTR-modules.

With these input and output FIFO buffers, the AVR controller monitoring the state of the USB controller and buffers can arrange highly-efficient packet data exchange alternately in both directions.

4.3 Arrangement of LTR-U-1-4 crate

LTR-U-1-4 architecture is a "miniature" of the architecture of LTR crate with one module. On LTR-U-1-4 block diagram it is shown that the function fig. 4-3 of LTR crate controller is performed by all crate equipment, except for the LTR module itself:

The functions of data buffering in both directions based on the FIFO principle, as well as the function of USB 2.0 *full-speed* controller are performed by a modern AT91SAM7S256[1] controller which operates based on a 32-bit ARM RISC processor. All software of AT91SAM7S256 controller is stored in the internal non-volatile memory of the controller and can be updated via USB.

The low-level interface of the LTR-module is implemented on FPGA basis (loading at power-up is not required)

Functionally, these are two independent serial data channels: from a LTR module to AT91SAM7S256 and back.

The function of power supply unit for the LTR module is performed by an external unstabilized voltage converter. The voltage converter ensures sufficiently continuous power consumption from an external power source in a wide range of input voltage change, which is important when powering LTR-U-1-4, for example, from batteries.

It is crucially important that the entire interface, including AT91SAM7S256, is powered from USB, so the USB device will be defined by the computer's operating system (and the crate will be defined by the LTR server) when a USB cable is connected even if no power is supplied to the voltage converter from an external source, in which case the LTR module will be de-energized, i. e. powered off.

[1] a product of Atmel Corporation, www.atmel.com

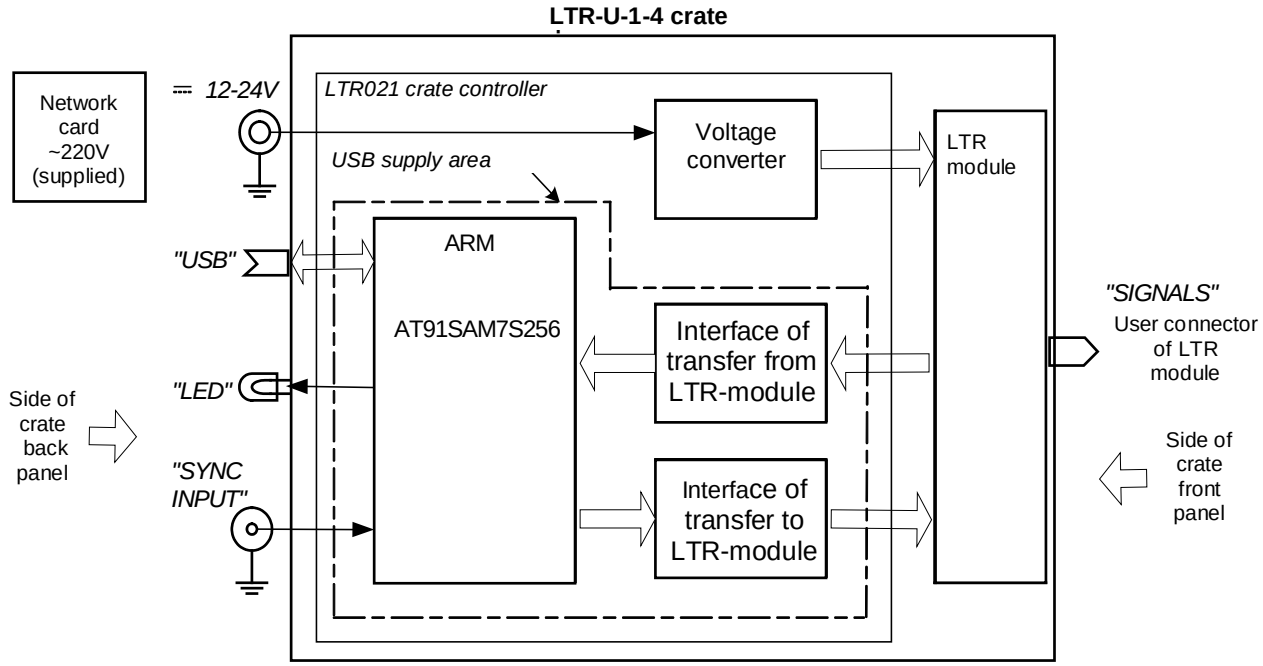


Fig. 4-3. Arrangement of LTR-U-1-4 crate

Functionally, it does not matter in what order the USB and external power cables are connected to LTR-U-1-4, but to ensure the full operability of LTR-U-1-4, both these connections are required.

"SYNC INPUT" is the input of external TTL signal "START TAG" (similar to the synchronization signal of LTR43 module configured for the input) through which the crate controller inserts a synchronization packet in a special (distinctive) format into the data stream going from the LTR module, and on the top program level it becomes possible to "tie" with a certain accuracy the time position of the current data sample relatively to the synchronization signal by the position of this synchronization packet in the general data stream going from the module. Unlike LTR43, in LTR-U-1-4 controller the "START TAG" can only be configured for input.

Functionally, the signal from the "SYNC INPUT" is directly translated to the interruption input of AT91SAM7S256 controller, so the time of controller response to the interruption and the speed at which the synchronization tag is inserted into the data stream (the accuracy of the synchronization tag time referencing) depends on the properties of AT91SAM7S256 controller firmware.

LTR-U-1-4 is similar to LTR crate by data exchange protocol and by LTR module and USB interfaces, and is therefore software-compatible with it.

4.3.1 Limits of the current implementation of LTR-U-1-4 with USB 2.0 full-speed interface

4.3.1.1 Speed limits.

Today, L-Card manufactures LTR-U-1-4 crate with USB 2.0 *full-speed* interface, while other LTR crates with USB interface support *full-speed* and *high-speed* USB interfaces.

! The current implementation of LTR-U-1-4 with USB 2.0 *full-speed* interface provides for limiting of data transmission speed above 800 KB/s.

Since LTR uses the 32-bit data format, the limits of the current implementation will lead only to limiting the maximum frequency of LTR11 ADC (up to 200 kHz inclusively), LTR22 ADC (up to 52 kHz inclusively) modules, LTR34 DAC output speed (up to 200 kS/s) in the stream output mode (the output speed will remain up to 500 kS/s in the self-excited oscillator mode), as well as the speed of data acquisition from the LTR24, LTR25, LTR210 modules (up to 200 kHz inclusively).

The above mentioned speed limits of the current LTR-U-1-4 are mainly connected with the bandwidth capacity of the USB 2.0 *full-speed* interface and AT91SAM7S256 functionality. On the other hand, the compactness and economic efficiency of the single-slot LTR crate controller architecture based on AT91SAM7S256 are the advantages of the current implementation.

! Note that it can be difficult for the user to change the configuration of modules in LTR-U-1-4, LTR-EU-2-5, LTR-CU-1-4, LTR-CEU-1-4 crates by himself, see sub-paragraphs 3.6.2, 3.6.2.2.

4.3.1.2 Limitations of the timing accuracy of inseting synchronization tags into data stream

"SYNC INPUT" is the input of external TTL signal "START TAG" (similar to the synchronization signal of LTR43 module configured for the input) but unlike LTR43 module, in LTR-U-1-4 the synchronization package is inserted by AT91SAM7S256 software instead of hardware. As a result, the accuracy of the synchronization signal time referencing will be about a millisecond instead of several microseconds.

In the future, L-Card is considering the possibility of releasing a compatible implementation of LTR-U-1-4 with a USB 2.0 *high-speed* interface in which the above speed limits will be eliminated. In addition, the possibility of external synchronization with the use of hardware is considered which will eliminate the above limitations related to external synchronization accuracy.

4.4 Arrangement of LTR-EU crates

Below the arrangement of 2-, 8- and 16-slot LTR crates with Blackfin processor and USB 2.0 *high-speed* and Fast Ethernet interfaces is described. Despite the different design of LTR-EU-2-5 2-slot crate as compared to 8- and 16-slot LTR-EU-8-1 and LTR-EU-16-1 crates, these crates have a similar architecture (internal logic structure), so their description is combined.

It is essential that in LTR-EU crates data paths are similar fig. 4-1. arrangement of ltr010 crate and based on the linear principle of data buffering (in the order as they are received).

The architecture of LTR-EU crates is based on LTR030 or LTR031M crate controller (**Ошибка! Источник ссылки не найден.**, **Ошибка! Источник ссылки не найден.**) installed inside the crate frame. The first controller is used in LTR-EU-8-1 or LTR-EU-16-1 crates and the second one in LTR-EU-2-5 crate. These controllers are of similar design and contain: Blackfin processor, 32 MB RAM, FPGA, optional micro SD card, USB 2.0 external interfaces ("USB" connector) and Fast Ethernet ("ETH" connector), external synchronization interface ("SYNC" connector). There are two 2-color "U" and "E" LED indicators on the panel of LTR-EU crates which indicate the status of connection via the USB 2.0 and Fast Ethernet interfaces, and "R" reset button. The difference is that in LTR-EU-2-5 the reset button is on the rear panel, and in LTR-EU-8-1 and LTR-EU-16-1 it is located on the front panel.

The crate controller interface with LTR modules is implemented through LTR001 motherboard, one in LTR-EU-8-1 and two in LTR-EU-16-1, or the LTR031C motherboard in LTR-EU-2-5
crate. Motherboards also ensure power supply to LTR modules.

In LTR-EU-8-1 and LTR-EU-16-1 forced ventilation is used with fan speed adapting to the temperature inside the crate. In LTR-EU-2-5, fan speed is not regulated.

LTRP2 power supply unit used in LTR-EU-8-1 and LTR-EU-16-1 crates is a standard network power supply unit for PC with a panel. In LTR-EU-2-5, a pulse converter with a wide input voltage range is used as a power supply unit. Its input voltage range is +11…+30 V

Let us continue with considering the block diagram of LTR-EU crate shown in **Ошибка! Источник ссылки не найден.**.

The block diagram is based on Blackfin ADSP-BF537 processor. A physical-level Ethernet controller (Ethernet PHY) which can support a full-duplex 100 Mb protocol at the physical level is connected to the dedicated MII interface. The external memory bus resource is divided between two devices: RAM (SDRAM-based) and USB interface controller. Other peripheral Blackfin interfaces are also used for FPGA loading, data transfer interface and FPGA control, as well as for connection with a 2 MB booTable flash memory and with an optional micro SD memory card.

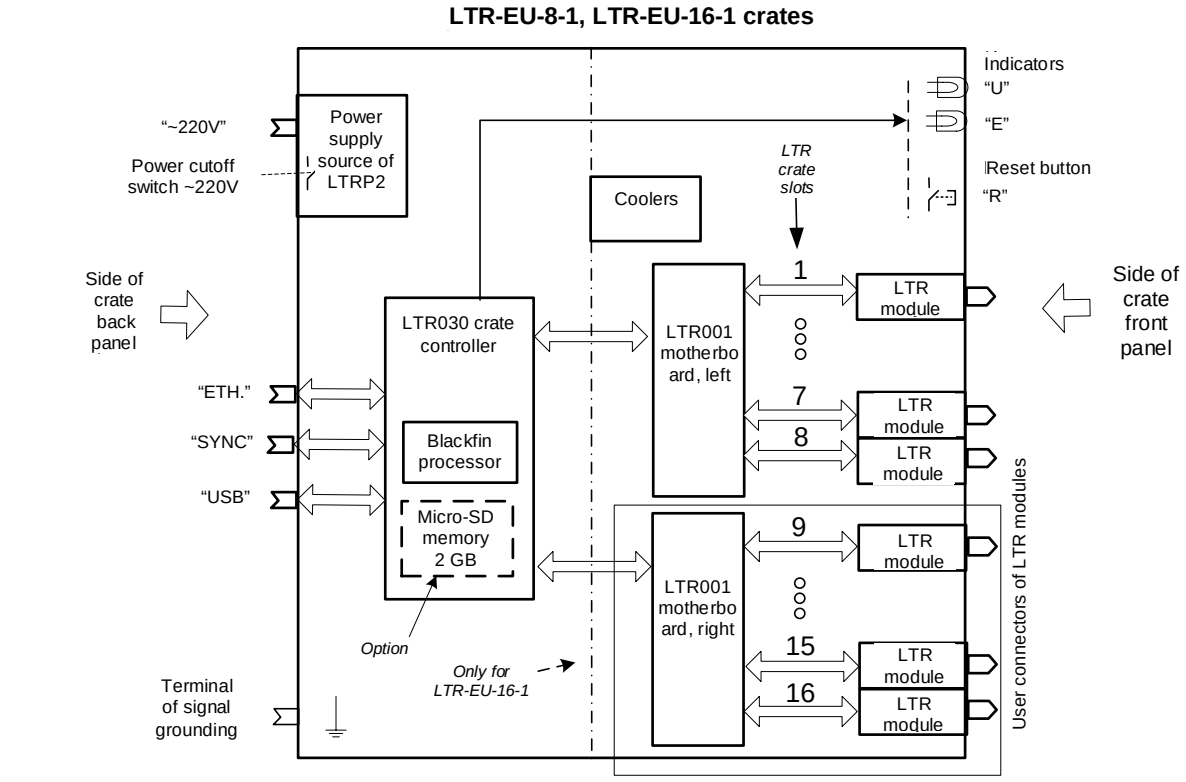


Fig. 4-4. Arrangement of LTR-EU-8-1, LTR-EU-16-1 crates

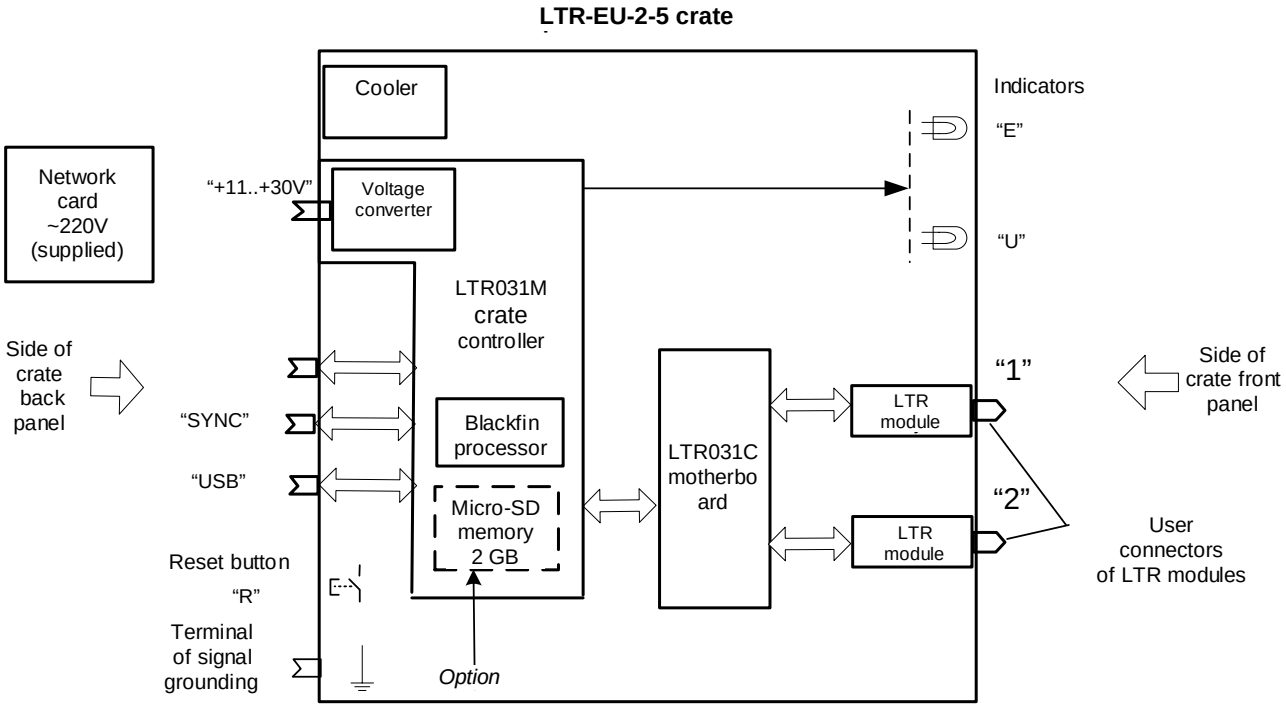


Fig. 4-5. Arrangement of LTR-EU-2-5 crates

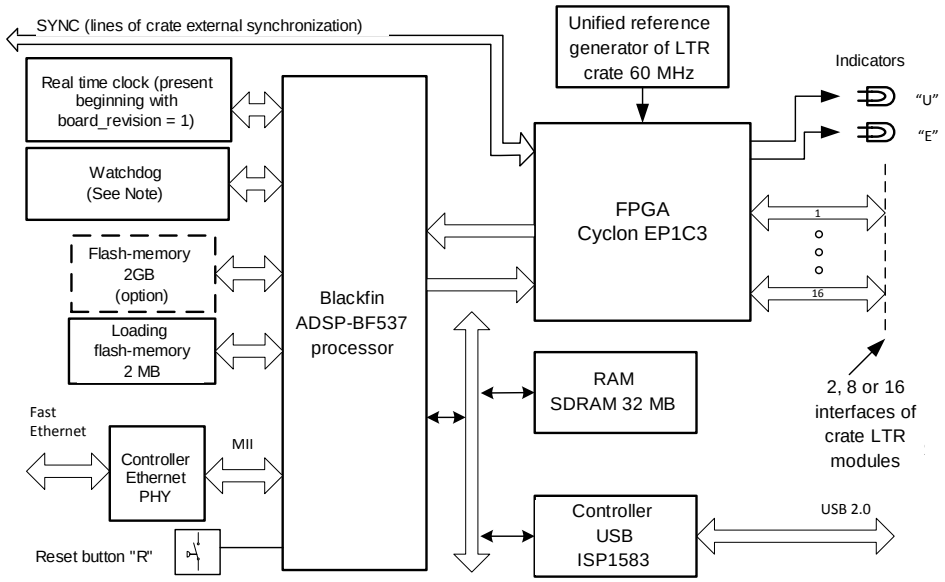


Fig. 4-6. Arrangement of LTR-EU crate controller

FPGA Cyclone performs low-level functions of LTR modules interface. The difference between 2-, 8-, and 16-slot crates is only in the number of interfaces used in LTR modules. FPGA also supports the crate synchronization functions (SYNC interface). In addition, signals controlling "U" and "E" indicators are transmitted from Blackfin through FPGA. It is assumed that FPGA Cyclone is loaded every time after powering up by the firmware stored in the booTable flash memory or by the firmware transferred via USB or Ethernet interfaces.

32 MB RAM based on SDRAM (4 banks, 8 MB each) is the external general-application memory of the processor with the maximum frequency of the memory bus of 133 MHz.

A single 60 MHz reference oscillator is used for LTR-EU crate synchronization and, in particular, for synchronization of LTR modules.

LTR030 controller in LTR-EU-8-1 and LTR-EU-16-1 crates has an adaptive fan speed control system (not shown in the block diagram) consisting of a digital temperature sensor (connected via SPI), a fan rotation speed sensor (based on Blackfin timer), and a fan rotation speed control system (operating via SPI with the use of FPGA). Control feedback of this system is implemented by means of a low priority background task of the processor.

Unlike LTR030, the current implementation of LTR031M controller of LTR-EU-2-5 crate does not have an adaptive fan rotation speed control system (however, it is possible that it will appear in future implementations).

Let us consider the sequence of initialization of LTR-EU crate controller. After the power is turned on (or after the reset button "R" is pressed), the processor will execute the program of initial loading from 2 MB flash memory. In the result of initial loading, USB and/or Ethernet interfaces are initialized, depending on which interfaces are currently connected via external connectors. It can be said that in the result of initial initialization LTR-EU crate controller becomes open for further firmware and software loading via USB or Ethernet.

Note at once that the initial loading program is written by the manufacturer to 2 MB flash memory in two copies for redundancy in case of abnormal situations associated with corruption of loading information. The main copy of the loader software is always used by default. As a fallback option, the user can run the backup copy of the loader program by long pressing (for more than 10 seconds) the reset button "R".

It can be said that as long as at least one copy of the initial loading program is correct, then the resources of LTR-EU crate will remain available to the user, otherwise the LTR-EU crate is subject to re-flashing at L-Card.

It is assumed that normally FPGA firmware (with a volume of up to 64 KB) will also be stored in the booTable flash memory. If the initial loading program finds the correct FPGA firmware in the flash memory, it will boot the FPGA in the result of which all FPGA control functions will "come to life", namely: – indication (indicators will light up), – interface functions of connection with LTR modules, – external synchronization functions of the crate.

In abnormal conditions when the loading program has been executed, USB or Ethernet interfaces have been initialized, but the FPGA firmware has not been found in the booTable flash memory, FPGA will not be loaded, and the crate indication will not light up. However, in this situation the system is open for access to the resources of LTR-EU crate controller via external interfaces which means that in principle FPGA can be loaded externally, and the data in the booTable flash memory can also be corrected.

With the improvement of LTR crates, L-Card intends to release updates of FPGA firmware. When an update is released, the user is provided with an opportunity to download FPGA firmware externally, regardless of which firmware was downloaded to FPGA before.

4.4.1 New functionalities of LTR-EU crate controllers, Board Version attribute.

Since 2010, LTR-EU-2, LTR-EU-8 и LTR-EU-16 crates with extended functionality are produced:

- A watchdog timer has been added.
- A real-time clock with a lithium battery has been added.
- The functionality of DIGINx, DIGOUTx lines has been extended due to the possibility of translating UART TX, UART RX signals of Blackfin processor via DIGINx and DIGOUTx lines (paragraph 4.4.2). In particular, this feature allows to have the third RS-485/RS-422 interface in LTR-EU crates using an additional RS485-UART cable (table 2-5). Currently, this interface can be fully used by the user only in case of low-level programming of user specific task (the further development of RS-485/RS-422 software capabilities supported by L-Card will depend on the consumer demand for these features).
- A program-accessible attribute of the physical presence of a micro SD card has been added.
- A possibility to insert/extract a micro SD card has been added:
  in LTR-EU-8/16 crates a micro SD card can be inserted via a hatch in the bottom cover of the frame (there is the "*Micro SD*" marking there), in the LTR-EU-2 crates it can be inserted through a slot in the side of the frame (there is the "*Micro SD" marking on the upper surface of the frame*).
- A possibility to connect JTAG emulator through a hatch in the bottom cover of LTR-EU-8(16) crate frame has been added (there is the "*JTAG*" marking on the frame).

The last two differences can serve as external attributes of availability of a crate controller with new features in this LTR-EU crate, but there is also a more reliable program attribute Board Version = 1. Accordingly, in previously released LTR-EU crates, the software-readable attribute Board Version is = 0. These software attributes will become available in your crate after the appropriate upgrade of the crate controller software and the LTR server if the current installed versions of this software do not support this option.

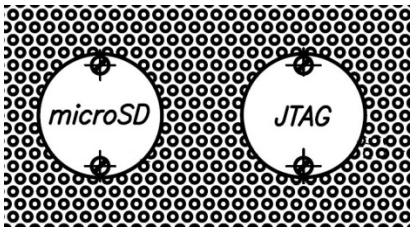


Fig. 4-7. Hatches on the bottom cover of LTR-EU-8(16) crate frame for inserting a Micro SD memory card and a JTAG-emulator

Fig. 4-8. LTR-EU-2 (Board_Version = 1) crate with an option for installation of a Micro SD memory card

4.4.2 Functionalities of external lines DIGINx, DIGOUTx

All LTR-EU, LTR-CU, LTR-CEU crates have the same functionalities of the external digital lines of the SYNC interface shown intable 4-1 – table 4-3.

! It is possible that at the time of reading this manual, not all hardware functionalities described here will be implemented with the use of the standard software supplied by L-Card but in case of low-level LTR-EU programming (chapter 20.), new hardware functionalities will be available.

In LTR-EU crates, a pair of programmable bi-directional ports PF0 and PG13 (PF1, PF3 for Board Version = 0) connected to FPGA are used for external synchronization (by interrupts) on Blackfin side or, possibly, for digital input/output. Accordingly, either Blackfin or FPGA can serve as the master unit on PF0 and PG13 lines. In this case, FPGA controlled by Blackfin can perform the required switching between the internal signals PF0, PG13, external signals DIGOUT1, DIGOUT2, DIGIN1, DIGIN2 and FPGA sync-tags start signals.

Output digital lines DIGOUT1 and DIGOUT2 can be set independently for the following states (table 4-1):

- "Output prohibited" (Z-state).
- Continuous level is "0" or "1" (this state is set by hardware, without using PF0 and PG13 Blackfin ports).
- Translation of the state of one of the input lines DIGIN1 or DIGIN2 (this mode can be useful when connecting a "chain" of synchronization circuits of several LTR crates).
- Translation of synchronization pulses "START TAG", "SECOND TAG". Timing parameters of synchronization pulses are similar to the corresponding synchronization pulses of LTR43 module: the initial state is logical "0", the duration of "START TAG" pulse is 500 ns, the duration of "SECOND TAG" pulse is 470 ms, the active drop (indicating the synchronization event) is from "0" to "1".
- Translation of PF0, PG13 Blackfin state to *DIGOUT1 or DIGOUT2* line, while the PF0 Blackfin port can be configured not only as a digital output port, but also as UART0 TX output, providing the user with a UART transmission channel for LTR-EU (Board Version ≠ 0) crate.

In LTR-EU crates, the state of the digital *input lines DIGIN1, DIGIN2* (table 4-2) can be independently translated to the input of PF0, PG13 Blackfin ports and/or to external FPGA synchronization input for external triggering of "START TAG", "SECOND TAG" synchronization tags. It should be especially noted that, for example, the same external synchronization event can, if necessary, be configured to trigger a synchronization tag and to interrupt Blackfin. When using *DIGIN1, DIGIN2* lines for external triggering of synchronization tags, the time *resolution between two fixed synchronization events for each of these lines will be 1.2 μs* (for example, two signal edges on DIGIN line with an interval of less than 1.2 μs, will, probably, generate only one synchronization tag instead of two ones).

The state of digital *input lines DIGIN1 or DIGIN2* can be independently translated to PF3 (UART1 RX) Blackfin input, proding the user with a UART receiving channel for LTR-EU (Board Version ≠ 0) crate.

Table 4-1. Functionalities of DIGOUTx lines

Line	Status	Description
DIGOUT1 (to the output only)	"Output prohibited"	DIGOUT1 ←"Z"
	"Level 0"	DIGOUT1 ← "0"
	"Level 1"	DIGOUT1 ← "1"
	"PF1" (Board Version = 0) "PF0 (UART0 TX) " (Board Version ≠ 0)	DIGOUT1 ← Blackfin PF1 (Board Version = 0) DIGOUT1 ← Blackfin PF0 (UART0 TX) (Board Version ≠ 0)
	"PG13"	DIGOUT1 ← Blackfin PG13
	"DIGIN1"	DIGOUT1 ← DIGIN1
	"DIGIN2"	DIGOUT1 ← DIGIN2

Line	Status	Description
	"START TAG"	DIGOUT1 ← "START TAG"
	"SECOND TAG"	DIGOUT1 ← "SECOND TAG"
DIGOUT2 (to the output only)	"Output prohibited"	DIGOUT2 ←"Z"
	"Level 0"	DIGOUT2 ← "0"
	"Level 1"	DIGOUT2 ← "1"
	"PF1" (Board Version = 0) "PF0 (UART0 TX) " (Board Version ≠ 0)	DIGOUT2 ← Blackfin PF1 (Board Version = 0) DIGOUT2 ← Blackfin PF0 (UART0 TX) (Board Version ≠ 0)
	"PG13"	DIGOUT2 ← PG13
	"DIGIN1"	DIGOUT2 ← DIGIN1
	"DIGIN2"	DIGOUT2 ← DIGIN2
	"START TAG" "SECOND TAG"	DIGOUT2 ← "START TAG" DIGOUT2 ← "SECOND TAG"

Table 4-2. Translation of DIGINx lines statuses to Blackfin ports

Line	Translation	Description
DIGIN1 (to the input only)	"Without translation"	
	"Translation to PF1 Blackfin input (Board Version = 0)" "Translation to PF0 Blackfin input (Board Version = 1)"	Blackfin PF1 ← DIGIN1 (Board Version = 0) Blackfin PF0 ← DIGIN1 (Board Version = 1)
	"Translation to PG13 Blackfin input"	Blackfin PG13 ← DIGIN1
	"Translation to PF3 (UART1 RX) Blackfin input"	Blackfin PF3(UART1 RX) ← DIGIN1
DIGIN2 (to the input only)	"Without translation"	Blackfin PF1 ←DIGIN2 (Board Version = 0)
	"Translation to PF1 Blackfin input (Board Version = 0)" "Translation to PF0 Blackfin input (Board Version = 1)"	Blackfin PF1 ← DIGIN2 (Board Version = 0) Blackfin PF0 ← DIGIN2 (Board Version = 1)
	"Translation to PG13 Blackfin input"	Blackfin PG13 ← DIGIN2
	"Translation to PF3 (UART1 RX) Blackfin input"	Blackfin PF3(UART1 RX) ← DIGIN2

Table 4-3. Modes of external sync-tags triggering at DIGINx signals

Line	Triggering mode
DIGIN1 (to the input only)	"no external triggering" "External START TAG" (on edge or on drop) "External SECOND TAG" (on edge or on drop)
DIGIN2 (to the input only)	"no external triggering" "External START TAG" (on edge or on drop) "External SECOND TAG" (on edge or on drop)

In LTR-CU, LTR-CEU crates, similar functions of DIGINx and DIGOUTx synchronization lines are supported by software of the built-in ARM controller.

4.5 Arrangement of LTR-CU-1-4, LTR-CEU-1-4 crates.

The architecture of LTR-CU-1-4 and LTR-CEU-1-4 crates is similar to the architecture of LTR-EU crates with the only difference that it is based on dual-core ARM controller LPC4337, fig. 4-9.

ARM controller supports interface functions which are software-compatible with LTR-EU crates.

LTR-CU-1-4 crate is the minimum design option having only a USB interface and no real-time clock (based on Q-crystal and BAT clock battery).

LTR-CEU-1-4 crate is the maximum design option with both USB and Ethernet interfaces and a real-time clock (based on Q-crystal and BAT CR2032 lithium battery). LTR-CEU-1-4 crate is supplied with the lithium battery pre-installed into the holder located at the bottom of the controller board. To replace the lithium battery, the user will have to disassemble the crate observing the precautions listed in paragraph3.6.2.2, page 52.

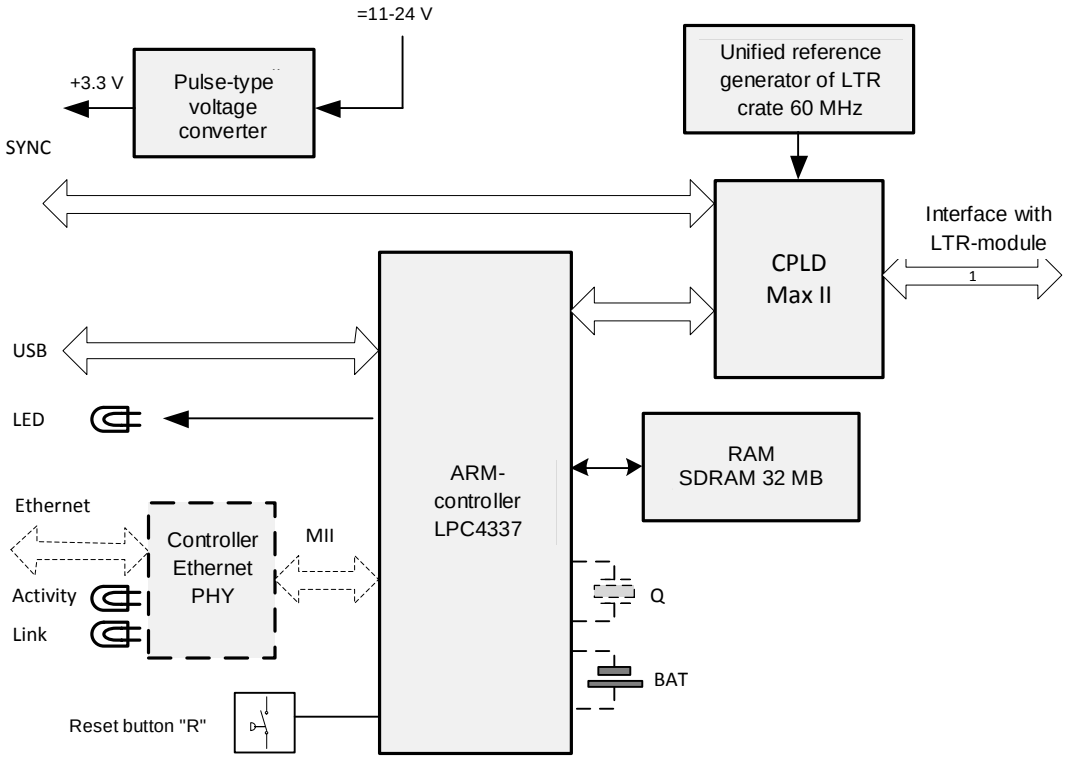


Fig. 4-9. Arrangement of LTR-CU-1-4, LTR-CEU-1-4 crates controller.

4.6 LTR interface protocols

In the LTR system, there are three types of control subjects among which an interface is arranged:

- *host computer,*
- *LTR crate controller,*
- *LTR modules.*

4.6.1 Word formats at the levels of host computer, crate controller and module

The host exchanges information with the crate controller in 32-bit words <31...0>

DDDD DDDD	**DDDD DDDD**	**CYFT MMMM**	**NNNN NNNN**
<31…24>	<23…16>	<15...8>	<7...0>

The data are buffered inside the crate controller in the same format.

CYFT MMMM byte of the 32-bit format shown above carries only the crate controller level information, so it is always processed by the crate controller and, except for **C** bit, is not transmitted to LTR- modules (in case of transmission from modules, the byte is added by the crate controller); the remaining bytes of the 32-bit format are translated directly to the module or from the module.

MMMM field contains the address of the module in the crate, depending on which the crate controller re-directs the data to the address of the corresponding module's location, and when transmitting the data in the opposite direction, the crate controller writes up the corresponding module address.

So, a 4-byte word sent by the host computer

DDDD DDDD	**DDDD DDDD**	**C000 MMMM**	**NNNN NNNN**
<31..24>	**<23..16>**	**<15..8>**	**<7..0>**

will be transmitted to the module, the slot **MMMM** is defined, in the *3-x bytes + 1 bit format:*

WITH	**NNNN NNNN**	**DDDD DDDD**	**DDDD DDDD**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

the response information from the module will be returned to the host in the original format:

DDDD DDDD	**DDDD DDDD**	**C000 MMMM**	**NNNN NNNN**
<31…24>	**<23..16>**	**<15..8>**	**<7..0>**

Bit **C** is translated to the modules and is recognized by the module hardware: if **C** = 1, this is a command, and if **C** = 0, this is data (for the terms and definitions, see paragraph 4.6.2).

It is essential that the first word addressed to the module must always be a command, since the **C** = 1 attribute is also a condition for the initial set-up of the byte counter in the packet on the receiving side.

Similarly, data are transmitted from the modules to the controller in the *3 bytes + 1 bit* format, and the controller writes-up them to a 32-bit word.

In Table 4-4, possible values of **CYrr MMMM** byte are indicated which define the context of the entire 32-bit word.

Table 4-4. Cyrr MMMM byte values

Byte value CYFT MMMM	Context of the 32-bit word
00rr MMMM	Data (samples) between the computer and the LTR- module, **rr** are reserve bits which have zero values by default, **MMMM** *is* the number of the module's slot in the crate.
10rr MMMM	The command between the computer and the LTR-module, **rr** are reserve bits which have zero values by default, **MMMM** is the number of the module's slot in the crate.
11xx xxxx	The service command between the computer and LTR crate controller, **xx xxxx** defines the context of the service command

4.6.2 Agreement on using data and command formats

! The 32-bit *data word* (with **C** bit = 0) must always carry a sample of user data to an output or input according to the main purpose of the data collection/output module, for example: data sample of ADC, DAC, I/O module, etc. The *command word* (i.e. the 32-bit word with **C** bit = 1) must be used to transmit all other information that is not the user data, but serves for control and signaling within the system and for configuration purposes. For example, command words are used to program the micro controller in a LTR- module, send control commands and receive confirmations.

4.6.3 LTR- module protocol

As it was said (paragraph 4.6, page 82), information is transmitted to and from the LTR-module in the **3 bytes + 1 bit format**:

Uniform module interface format			
C	**NNNN NNNN**	**DDDD DDDD**	**DDDD DDDD**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

- **C *is*** a hardware bit serving as the command attribute (**C** = 1) or as the data attribute (**C** = 0).
- **N *is*** control information at the level of LTR- module. In case that a command (**C** = 1) is transmitted to the LTR- module, the bits **N** <23> and **N** <22> are received by the LTR-module hardware and define the command code while the remaining **N** bits may be used to encode the module channel number (if the bits <21..16> are not used, they must have zero values).
- **D *is*** context-dependent information.

! Hereafter, everywhere in the description of formats at the LTR- module level, the 3 bytes + 1 bit format will be used. It should be taken into account that in the host computer this information is represented in the format extended to 32-bit with a 16-bit field in the major part, as explained in paragraph 4.6, page 82.

Next, the format of STOP, RESET, PROGR, INSTR commands, DATA data format and interface protocol at the LTR module level will be considered.

! STOP, RESET, PROGR *are* common interface commands for all LTR- modules, which are executed by the module hardware without the participation of the module firmware. The INSTR command and DATA data formats are used for translation of commands and data in both directions in the program mode of the LTR-module.

4.6.3.1 STOP command.

The meaning of STOP command:

- Full module stop.
- Interruption of the response information flow from the LTR-module (in particular, from the controller or DSP module).
- Module switch-over from the program mode to the hardware mode.

STOP command.			
1	**00xx xxxx**	**xxxx xxxx**	**xxxx xxxx**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

- **x** – the bit values depend on the context (may be not used)

STOP command has no module response.

4.6.3.2 RESET command.

The meaning of RESET command:

- Resetting AVR (DSP) in the module (must be followed by STOP command to exit the module from the reset mode).
- Receiving the module ID in response (purely hardware function).

RESET command.			
1	**10xx xxxx**	**xxxx xxxx**	**xxxx xxxx**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

- **x** – these bit values depend on the context (may be not used)

Response word of RESET command.			
1	**10ee eeee**	**iiii iiii**	**iiii iiii**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

- **e** *is* an echo of the input command (bits <21 ... 16> of the input command)
- **i** – LTR module identifier which, depending on the module type, takes on the following values:

LTR module	LTR module identifier value **iiii iiii iiii iiii** of the response word of RESET command (hex)
LTR11	**0B0B**
LTR22	**1616**
LTR27	**1B1B**
LTR34	**2222**
LTR35	**2323**
LTR41	**2929**
LTR42	**2A2A**

LTR module	LTR module identifier value **iiii iiii iiii iiii** of the response word of RESET command (hex)
LTR43	**2B2B**
LTR51	**3333**
LTR210	**D2D2**
LTR212(M)	**D4D4**

4.6.3.3 PROGR command.

The meaning of PROGR command:

- AVR programming or loading of DSP module (after the last PROGR command, a canceling STOP command must be issued).
- Receiving response words in the form of an echo from input information.

PROGR command.			
1	**01xx xxxx**	**pppp pppp**	**pppp pppp**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

- **x** – the bit values depend on the context (may be not used);
- **p** *is* loading information. Byte <15..8> is loaded first and byte <7..0> is loaded second.

Response word of PROGR command.			
1	**01ee eeee**	**kkkk kkkk**	**kkkk kkkk**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

- **e** *is* an echo of the input command;
- **k** *is* an echo from AVR in the module. In case of a module with DSP, there is no response word for PROGR command.

4.6.3.4 INSTR command.

INSTR command *is* a command for LTR module controller (DSP)-. The sequence of INSTR commands transmitted to the controller (DSP) forms the working (program) cycle of the module: initial module set-up, start of data collection, stop of data collection. The module exits the working cycle at STOP command. The number and meaning of the working cycle commands can vary depending on the type of module.

INSTR command format:

Response word of INSTR command.			
1	**11xx xxxx**	**xxxx xxxx**	**xxxx xxxx**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

- **x** – the bit values depend on the instruction context;

The optional response word of INSTR command depends on the meaning of the instruction and LTR module type. In fact, this is an optional response command:

Response word of INSTR command.			
1	**xxxx xxxx**	**xxxx xxxx**	**xxxx xxxx**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

- **x** – the bit values depend on the context of commands of the particular LTR module. For all LTR modules (except for LTR34), see this information in the description of the command

system for a particular LTR module in the *Programmer's Manual* [1]. Unlike the other ones, LTR34 DAC module is purely a hardware device (without a controller and DSP), so the description of its command system is given in this manual (paragraph 14.4.1, page 233).

4.6.3.5 *Data flow for modules configured for input.*

An instruction transmitted to the module can call a response data stream in the following format:

DATA data.			
0	**SSNN NNNN**	**DDDD DDDD**	**DDDD DDDD**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

- **D** *is* data,
- **N** *is* channel level information (channel number, etc.),
- **SS** *is* a circular packet counter[1].

SS packet counter field is assigned on the transmitting side and is intended for monitoring the connectivity of the data stream (including the detection of faulty situations).

In LTR, dual-format packets are supported when the data source is in 32-bit format (for example, 24-bit ADC format, extended to 32- bits).

For example, a double packet carrying 32 bits of **D** data has the following form:

0 S0NN NNNN DDDD DDDD DDDD DDDD 0 S1NN NNNN DDDD DDDD DDDD DDDD

Notes:

INSTR response commands can be inserted into the data stream from the module to the crate controller.

The DATA data stream should only be used to transmit user information (data samples) of the module according to its main purpose.

4.6.3.6 *DATA stream for modules configured for output.*

A sequence of data intended for output can be inserted between INSTR input commands for output modules (for example, DAC):

DATA data.			
0	**nnnn nnnn**	**dddd dddd**	**dddd dddd**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

d ***is*** data intended for output,

n ***is*** information on the channel number etc.

Note:

The DATA data stream should only be used for output data of the module according to its main purpose.

[1] The markup boundary and bit depth in the high byte of the DATA packet may vary depending on the LTR module type.

4.6.3.7 Rate of data transmission of LTR- modules interface

All LTR crate controllers have the functionality to control the transmission rate via LTR module interface. Let us consider this in detail.

The interface from each LTR module to the crate controller has the single data transmission mode with a rate of up to 1.6 MB/s.

The interface from the controller to a separate LTR module has the following data tramsnission modes:

- *Fast transmission* (up to 1.6 MB/s).
- Slow transmission (up to 80 kB/s).
- Technological *ultra-slow transmission* (mode of FUSE-bits programming in AVR controllers of LTR modules).

Most LTR modules (LTR11, LTR22, LTR27, LTR51, LTR41, LTR42, LTR43) have an AVR controller that can process commands or data received from the controller at a relatively low speed which does not exceed 80 kB/s, so the crate controller must operate in the *slow transmission mode* for sending information to these modules. For relatively slow LTR212 module with DSP, the *slow transmission mode* is also used.

LTR34 DAC module, unlike the other modules, operates to receive data in the *fast transmission mode*. Therefore, the DAC module has channels working in both directions with the technical data transmission rate of 1.6 MB/s. During the initialization of LTR modules in the crate, LTR34 module can also receive commands from the crate in the *slow transmission mode*.

Let us note once again that *all* LTR modules configured for data transmission to the crate have the *single* technical transmission speed mode of up to 1.6 MB/s.

Ultra-slow transmission is a technological (non-user) mode that is applied by the manufacturer during flashing FUSE-bits of AVR LTR modules.

4.6.3.8 The sequence of commands transmission to -LTR modules.

The protocol of host computer- interaction with a- LTR module is determined by the sequence of four main commands: STOP, RESET, PROGR, INSTR.

The first command coming to the module must always be STOP. The permissible sequence of commands sent to the a LTR- module must correspond to the directed graph (Fig. Fig. 4-10). In the graph, the SPEED (i) vector is used to describe the speed mode of transmission (paragraph 4.6.3.7) to the interface of each (i-th) slot of the LTR module, and AVRFUSE variable is used to indicate the technological *ultra-slow transmission* mode. Let us further explain the meaning of this graph.

The first action that the crate controller must perform to start the initialization of a LTR-module *is* to switch over to the *slow transmission mode* and send the STOP command.

The *STOP command* initializes the hardware interface part of the LTR- module, cuts the response data stream from the LTR- module in case the module was started previously (naturally, the response flow from the module will be exhausted when the FIFO in the crate controller is emptied).

To send the subsequent RESET command, the host computer must receive the identifier from the module. *Having received the module identifier, the host must determine* in which speed mode this module operates (fast (1.6 MB/s) or slow (80 KB/s).

Depending on the decision made, there will be *5 options for continuing the command* sequence (see the corresponding graph branching from left to right)*:*

- AVR FUSE-bits programming *is* a special technological mode of programming AVR fuse-bits (it is most likely that the user will never need to work in this mode).
- AVR programming in the LTR module with subsequent transition to the beginning of the graph (the user will apply this mode when updating the firmware of LTR modules with AVR)
- ADSP loading, after which the LTR- module will operate normally (this is the standard loading mode for LTR212 module with ADSP);
- Further LTR34 DAC initialization after switching over to the *fast transmission mode* with subsequent normal operation.
- Initializing another LTR- module (LTR11, LTR22, LTR51, etc.) with AVR at a slow speed, followed by normal operation.

The first INSTR command received from the host- computer will switch the LTR- module into the *operating cycle*. The operating cycle- of the LTR module *is* a state in which the module hardware permits the program control of the module: perception of incoming INSTR commands and sending response INSTR commands and DATA data. During the LTR- operating cycle, the module must support necessary program commands according to the main module application: LTR- configuration commands, start/stop of data acquisition, etc. The first incoming STOP interface command will immediately interrupt the operating cycle of the LTR- module: the channel of response information transmission from the LTR- module is blocked by the hardware and the module goes into a purely hardware mode of responding the RESET, STOP and PROGR commands.

It is essential that the described permissible sequence of commands (if not to take into account the technological modes of AVR programming in the LTR- module) can be implemented independently and in parallel for each LTR- module; at least, LTR hardware allows for this[1].

[1] software issues of ensuring parallel initialization and operation of LTR modules are not considered in this manual.

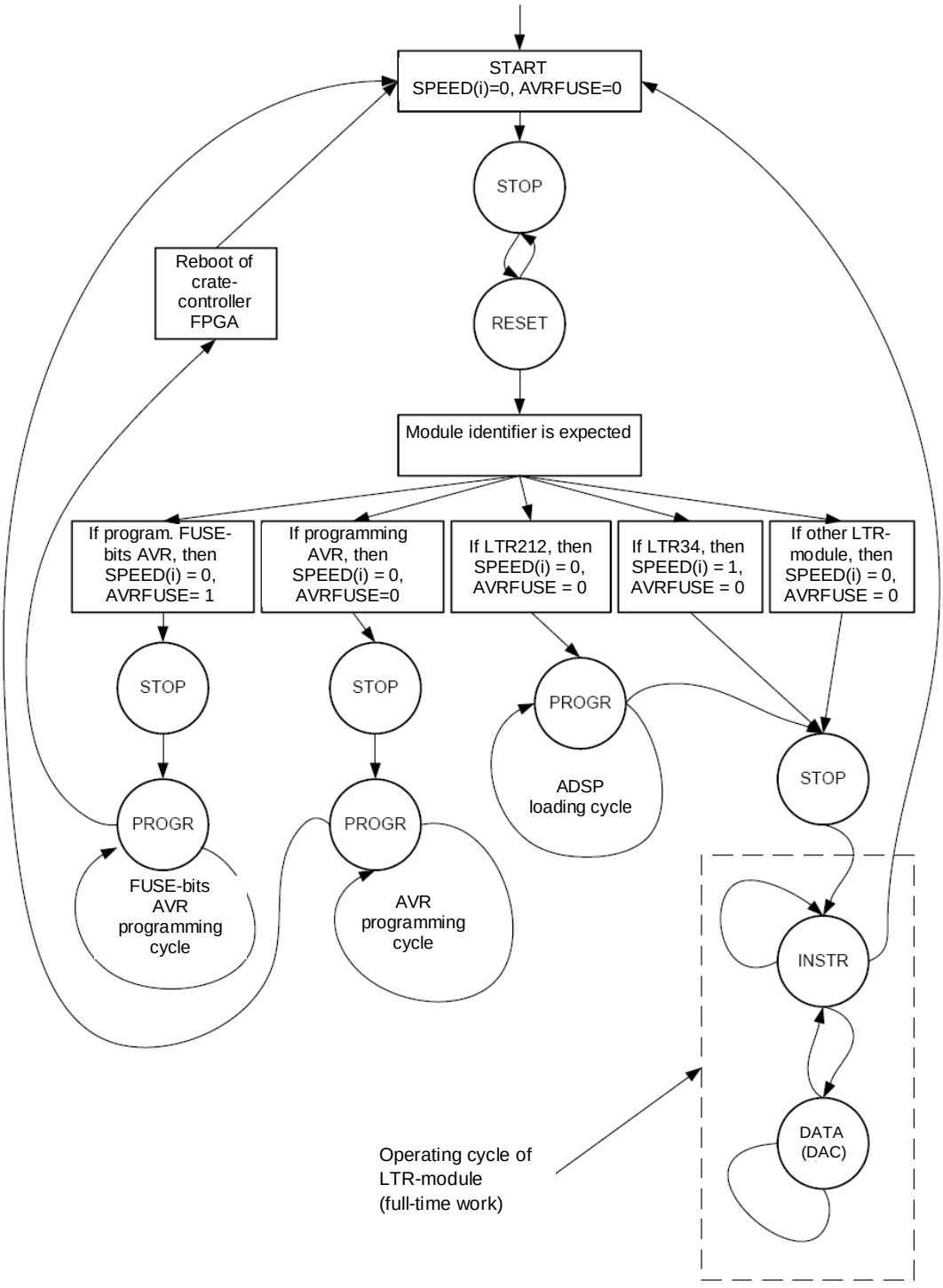


Fig. 4-10. Graph. Permissible sequence of commands

4.6.4 Physical level of LTR-module protocol

Format of the package transmitted between the crate controller and LTR-modules (see paragraph 4.6.1, page 82), **C NNNNNNNN DDDDDDDD DDDDDDDD** contains three 9-bit bytes:

CNNNNNNNN, 0DDDDDDDD, 0DDDDDDDD

Each 9-bit byte is transmitted separately according to the following UART-like protocol:

<start-bit> – <control bit> – <8 data bits[1]> – <stop-bit>

The control bit is **C** only in the first byte of the packet, in the second and the third bytes the control bit is always zero. Therefore, the receiving side, receiving the single control bit after the start- bit (assuming the normal subsequent stop-bit receiving), makes the following decisions:

sets the byte counter to zero;

makes a decision on the start of receiving the command packet.

If a data packet is received, then in all three bytes the control bit is zero and the data packet is received with the byte counter on the receiving side. Therefore, *to synchronize the receiving sides of the interface of the crate controller and the LTR -module, it is necessary that the command packet is sent first after the system initialization.*

It is normal that after the stop-bit of the previous byte and the start-bit of the next one, there may be asynchronous pauses that determine the real data transmission rate. Therefore, the single data format of the LTR module consists of 33-bit physical layer intervals in which 24 bits of data carry the information and 1 bit defines the command.

4.6.5 Format of synchronization tags in LTR

As an important specific case of LTR interface formats described in paragraph4.6.1, below are listed the formats of the synchronization labels at the level of the LTR crate controller.

Tag from LTR41/42/43 module:

00ts 0000	0000 0000	1000 MMMM	0000 0000
<31…24>	<23..16>	<15..8>	<7..0>

Tag from LTR-EU crate:

00ts 0000	0000 0000	1111 1111	0001 0000
<31…24>	<23..16>	<15..8>	<7..0>

Symbols: **t** is the attribute of the second tag, **s** is the attribute of the start tag (zero bit value means no corresponding sync event, single value means its presence), **MMMM** is the code of the slot number (from 0 to 15).

4.6.5.1 New format of synchronization tags (project).

Below you can find the preliminary information about our future plans to implement a system for representation of time tags in Unix Time format into the LTR system with referencing to LTR crate real-time clock.

In the future, it is planned to implement the following advanced format of synchronization tags which will include the information about date and time of second tag birth according to the real-time clock in the crate controller:

Extended format of synchronization tag				Formats description
<31…24>	<23..16>	<15..8>	<7..0>	
00ts 0000	0000 0000	1111 1111	0001 0000	Standard tag format (one word)

[1] high-order bit and high-order byte first

01ts TTTT	TTTT TTTT	1111 1111	0001 0000	**the 1-st word** of the tag of extended format with the field TTTT TTTT TTTT <11:0>
1000 TTTT	TTTT TTTT	1111 1111	0001 0000	**the 2-nd word** of the tag of extended format with the field TTTT TTTT TTTT <23:12>
1100 TTTT	TTTT TTTT	1111 1111	0001 0000	**the 3-rd word** of the tag of extended format with the field TTTT TTTT TTTT <35:24>

Notes:

1. For the mode in which the "second tag" is used without reference to the real-time clock, the one-word tag format is used.

2. If the "start tag" does not come simultaneously with the "second mark" in the extended format, then one of them is always transmitted in the one-word (old) format.

3. The LTR tag in the extended format is always transmitted with a strict sequence of words from the 1st to the 3rd word (insertion of the words of other data/LTR commands between the words of the tag is logically excluded).

4. Time and date inserted in the extended format corresponds to the new second started after the arrival of the current second pulse from the real-time clock of the LTR crate controller.

5. The time format in the 36-bit T ... T format corresponds to the Unix Time format, cut to 36 bits.

4.7 Principles of synchronization of data acquisition in the LTR system.

Let us first outline the synchronization principles in the form of theses:

- All data from LTR-modules in LTR-EU are accumulated in the single FIFO buffer in the order of their arrival together with the synchronization tags and in the same order these data are sent to the computer (except for operating in the autonomous mode).
- Synchronization tag is a special distinguishable format indicating the occurrence of a synchronization event.
- Two types of synchronization tags are supported independently, which arise from two independent synchronization events.
- In LTR-EU, there is a possibility of preliminary configuring for several synchronization events:
  1) *External synchronization*: from edge/fall at one of DIGIN1, DIGIN2 inputs of LTR-EU crate.
  2) *Internal synchronization:* program synchronization (via LTR-EU Blackfin), or by periodic second intervals (hardware timer).
  3) *Internal synchronization with translation on DIGOUT1, DIGOUT2 line of LTR-EU crate*: the same as *internal synchronization*, but with the difference that synchronization events in the front form are also translated outside to DIGOUT1, DIGOUT2 line, for example, for multi-frame synchronization.
- At the upper software level, the LTR server receiving the data and tag stream (in the same order in which it was arranged in the LTR-EU FIFO) via the interface separates the synchronization tags from the data, conditionally splitting the data stream into sections before and after the synchronization tag arrival, thus referencing the data to the time

of synchronization tags arrival. The reference accuracy ensured by this method is up to the 1st data collection period from the fastest LTR module, which added the data to the buffer.

- The synchronization principle of LTR-EU crate as such does not require a synchronous start of the data stream from different LTR-modules, while some LTR modules have also their own synchronization inputs depending on their specifics, which in some cases provides additional synchronization capabilities at the module level.

Let us consider a typical example of use of external synchronization in LTR-EU which is the examination of vibrations in a rotary machine. Pulse synchronization signals are sent to DIGIN1, DIGIN2 from rotational speed sensors and rotor angle. Vibration signals from different units of the machine are transferred to ADC. This is a synchronous multi-channel data acquisition system with the synchronization accuracy of up to 2.5 μs (if at least one LTR11 is used at the data collection frequency of 400 kHz).

For support of special synchronization commands (tags) in LTR, a special command format is used, as shown in 4.6.5.

The general idea of synchronization in LTR is to create packets containing time tags in the I/O device of the crate, and to insert them into packets coming from all other modules in a centralized manner, by means of the LTR server software. The function of such I/O devices can be performed by LTR41, LTR42, LTR43 modules and by the built-in synchronization device in LTR-EU, LTR-U-1-4[1] *crate controllers.*

LTR-EU crates have universal digital inputs and outputs (paragraph 4.4.2, page 78), which, in particular, can be used as synchronization inputs and outputs. This provides the full synchronization functionality in the crate without LTR41, LTR42, LTR43 modules installed in it (this is especially important for double-slot LTR-EU-2-5 crate).

Let us consider in more detail the principles forming the ideology of synchronization of data - acquisition in LTR.

The entire LTR crate including the crate controller and LTR- module interface is synchronized in relation to the frequencies calculated by dividing the full frequency of the *single reference generator* (60,0000 MHz) by an integer[2].

The whole process of data acquisition in LTR modules is synchronized in relation to the frequencies calculated by dividing the full frequency of the *single reference generator*[3] by an integer.

Progressive approximation ADC modules (LTR11) have no significant internal data delay, since they do not have a data buffer, and sigma-delta ADC modules (LTR212 (M), LTR22, LTR24) have a constant pipeline delay (the pipeline delay value depends on the initial settings of these modules). Data packets from all crate modules are accumulated in one *large output FIFO* buffer of the crate controller (it does not matter that in different LTR crates this FIFO is arranged by different means) *in the order of packets arrival* and transferred from there on the "first-in-first-out" basis via the USB to the PC. Therefore, by inserting into the common data stream special synchronization packets *(time tags)* occurring at known moments of time, and then by parsing the data and selecting

[1] In a single-slot crate, the synchronization function has limitations, see paragraph 4.3.1.2, page 64.

[2] The parameters of the single reference LTR crate generator are given in Appendix A.16, page 210.

[3] Exceptions: - ADC external synchronization mode (for example, in LTR11); - an exotic ADC specifically configured for a narrow synchronization frequency range (LTR212), which requires installation of an individual crystal oscillator in the module.

the tags on the PC side, information stream is *broken down by time with the time tags recording accuracy*.

In LTR, a *second tag* and a *start tag* can be generated either by LTR41(LTR42, LTR43) module[1] or by LTR-EU crate controller. Internal *second tags* of these devices which ***is*** calculated by dividing the frequency *of the single reference crate generator* ***are*** inserted into the data stream with a second interval. The "start tag" can be sent at any time. For example, it can be used to indicate the beginning of data acquisition in the system or can have another meaning at the user's discretion.

For global tasks, LTR supports *multi-crate synchronization* and external synchronization, for example, from an external *time standard system*. For these purposes, in LTR41 module (LTR42, LTR43) or in LTR-EU rack controller, each of the internal signals *"second tag"* and *"start tag"* can be translated to the output or configured for input.

If the start of data acquisition- in the LTR input module (ADC) is not referenced to a *second tag* or to a *start tag*, then the position of the current data packet on the time axis can be estimated relatively to the *second tags* **with an accuracy up to the period of data acquisition** via the corresponding channel. This means that the slower is the data acquisition, the less accurate is the *time* reference.

If the *start of data acquisition in the LTR- input module is referenced to a start tag* (for example, the start tag signal of LTR43 is connected to the signal of start of data acquisition of the LTR- input module) and the LTR -module is internally synchronized, then we have a system synchronous relatively to the *single reference crate generator* in which the time referencing - accuracy *is determined* by the hardware accuracy of packets getting into the *large output FIFO buffer* of the crate controller. **The time referencing accuracy in this case is ± 1 µs.**

If the LTR- module uses independent external synchronization of data sampling and requires temporary marking, then in order to ensure the maximum accuracy it is desirable that time tag signals and start data collection signals be external. Otherwise, if one of these signals is external and the other is internal, phases of independent frequencies will disperse and the accuracy of the time referencing at large time intervals will be deteriorated.

In the ideology *adopted in the LTR, synchronous LTR-data output modules (DACs)*, unlike ADCs, must have a large data buffer to ensure the continuity of the output stream. In addition, DACs must have an *external triggering signal*, which can be combined with the start tag signal (for example, in LTR43), which will make the time referencing possible.

4.7.1 The mechanism of simultaneous start of data acquisition in LTR-modules (project).

Along with the existing mechanism for synchronizing data coming from different LTRs using synchronization tags inserted into the data stream (when the start of data acquisition in different modules was not time-referenced), we also intend to introduce for LTR-EU crates a possibility of synchronous triggering of data acquisition inside LTR modules based on external or internal synchronization events. This feature is implemented by modifying the firmware of the LTR-EU rack controller and by providing additional support at the level of new API-functions.

As this project is implemented, information on new synchronization features will be added.

4.8 The switched-off and operating state of a LTR module

For galvanic isolation of power supply circuit in LTR- modules, a system for generating pulsed supply voltage is implemented in all LTR crates, and galvanically isolating transformers are

[1] If there are several LTR41, LTR42, LTR43 in a crate, then one of them.

installed in LTR- modules. In a few seconds after crate powering on, the power will be supplied to all LTR modules. In fact, after the power supply the state of the modules is changed from the *switched-off* to the *operating* state, which may change some of the electrical characteristics of the signal lines of a particular LTR module in the crate. From this follows the need to introduce the concepts of the *operating* and the *switched-off* state of the LTR-module, which will be used later in describing the characteristics of the LTR-module. Let us clarify these notions:

The LTR- module is in the *switched-off state* when it is not powered. In practice, this can *be* observed when the LTR crate is turned off OR the module for some reason has not been defined in the system yet, OR it is not defined for any reason OR it has already disappeared from the list of visible LTR- modules.[1]

Hereafter, when speaking about the *operating state* of the LTR- module we will assume that it is seen by the LTR- server.

[1] The list of currently visible modules is supported by the LTR server in the real time, see LTR Crate System. Programmer manual [1]

Chapter 5. LTR11 ADC module

5.1 General description of LTR11.

Fig. 5-1. LTR11 view

5.1.1 Device assignment

LTR11 ADC module is intended for creation of multi-channel data acquisition systems for industries and laboratories.

5.1.2 General information about LTR11

- LTR11 contains one 14-bit ADC with a maximum data acquisition frequency of up to 400 kHz and an input switch allowing for multi-channel data acquisition: *up to 32- channels for acquisition of single-phase signals with common ground, or 16-channel differential mode*. There are *4 programmable input signal sub-ranges ± 10 V, ± 2.5 V, ± 0.6 V, ± 0.15 V* set independently for each channel.
- *LTR11 inputs are galvanically isolated* from the ground, LTR crate and other LTR modules (there is no galvanic isolation between the inputs).
- ADC synchronization triggering signal and the data acquisition start signal can be both internal or external (which is programmable, and is set independently "on edge" or "on drop" for external signals). General principles of synchronization in LTR are described in paragraph 4.7, page 91.
- There is *a test mode for checking input lines for breakage and short circuit* (paragraph 5.3.4, page 100).
- It is assumed that data correction task calculating calibration factors with the help of line correction method must be performed by user computer (library functions are available).
- The architecture of LTR11 ADC module (input switch - single-channel amplifier - single-channel ADC) allows to obtain a product with relatively *low cost* recalculated for one

channel, but this requires the user to observe *important LTR11 connection rules for multi-channel mode* (п. 5.4.4, стр. 104).

5.1.3 LTR11 module configuration

Basic configuration of LTR11 is described in paragraph 2.4, page 29.

It should be noted that L-Card does not supply top-level software for monitoring LTR11 signal input circuits (paragraph 5.3.4, page 100).

5.2 Installation and set-up

During LTR11 installation in crate, observe the module installation rules common for LTR system set forth in paragraph3.6.2 , page 51.

On LTR11 module board there can be one or two technological 6-pin connectors. Do not put jumpers on process connectors and carry out any external connecting to them!

5.3 Overview of LTR11 hardware components and operation principles

5.3.1 Block diagram

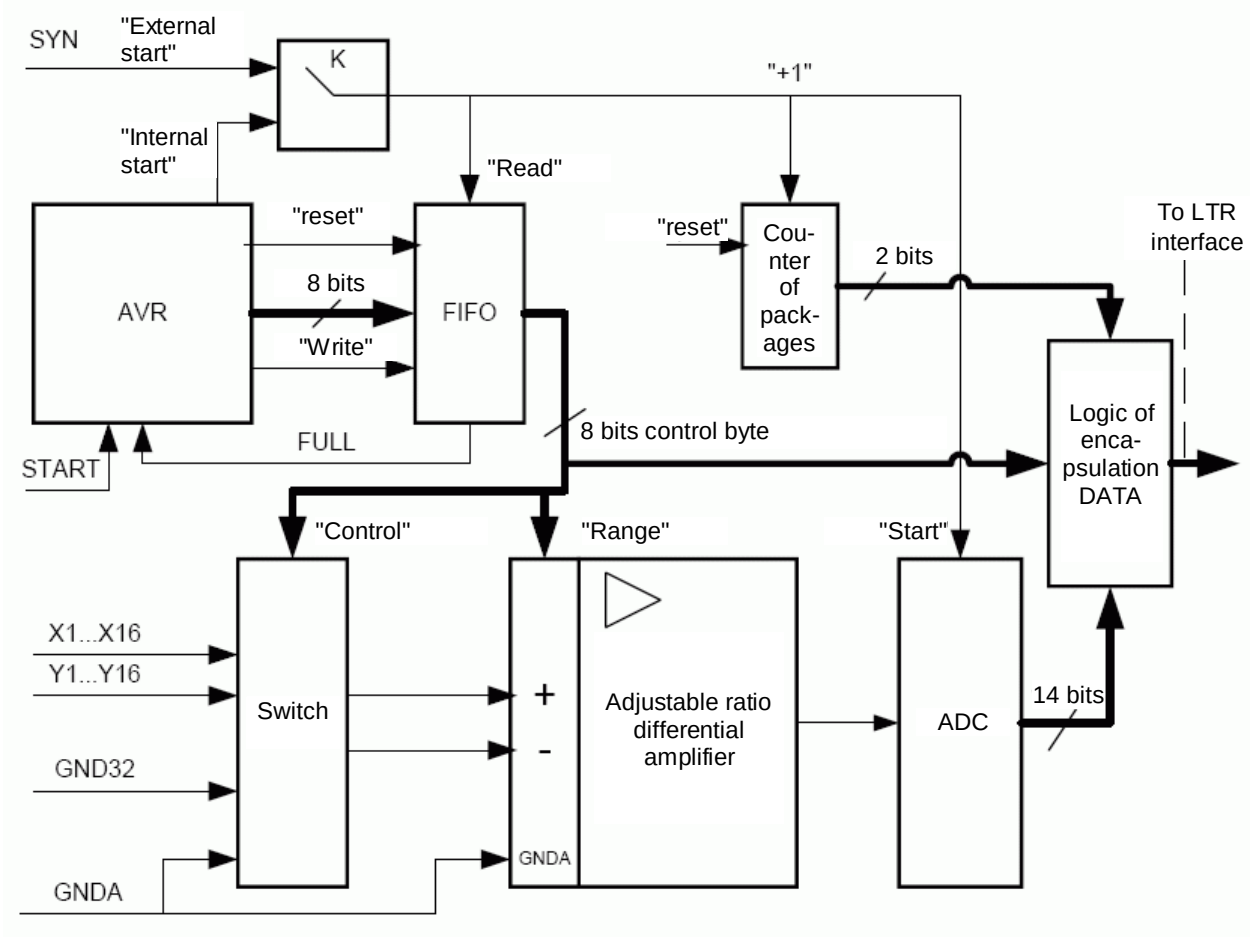


Fig. 5-2.
LTR11 module block diagram

The block diagram for LTR11 hardware engaged in data collection is shown in Fig. Fig. 5-2.

The switch, differential amplifier and input circuits of the ADC form the analog LTR11 path.

Input signals X1, ..., X16, X1, ..., Y16, GND32, after passing through the controlled switch, get to the differential amplifier with a controlled transmission factor. The signal from the amplifier output scaled in accordance with the set range and separated from the in-phase noise is fed to the input of a progressive approximation ADC. The ADC output is directly (without buffering) is connected with the logic of the output data packet formation and the interface with the crate controller.

Control of selection of channels, 16- or 32-channel mode and range is carried out by the control byte coming from the AVR[1] via the buffer FIFO. The sequence of these bytes that control

[1] ATmega8515 micro controller

the ADC data acquisition frame is written to *the control Table* (in the AVR memory) via the LTR interface during the initial initialization of the LTR11 module.

In the process of data acquisition, AVR sends a control byte to the analog path for each ADC sample, cyclically reading the control Table . The control Table , the size of which can be preset from 1 to 128 bytes, allows for flexible specifying the sequence of polling channels in the frame.

Technically, to compensate for the temporal asynchrony of issuing control words, the AVR preliminarily writes control words into the hardware FIFO, while reading from the FIFO occurs absolutely synchronously at the ADC start signal.

The ADC start signal programmed by the K switch can be both external (external synchronization mode) or internal issued by the internal frequency divider (internal synchronization).

All internal synchronization frequencies from 5 Hz to 400 kHz are the products of division of the full frequency of the *single 60,0000 MHz*[1] *generator (oscillator) located in the LTR crate controller by an integer*.

Frequencies of ADC internal synchronization can be set from the following series (in Hz):

400000, 375000, 312500, 300000, 250000, 234375, 200000, 187500, 156250, 150000, 125000, 120000, 100000, 93750, 78125, 75000, 62500, 60000, 50000, 46875, 40000, 37500, 31250, 30000, 25000, 24000, 20000, 18750, 15625, 15000, 12500, 12000, 10000, 9375, 8000, 7500, 6250, 6000, 5000, 4800, 4000, 3750, 3125, 3000, 2500, 2400, 2000, 1875, 1600, 1500, 1250, 1200, 1000, 960, 800, 750, 625, 600, 500, 480, 400, 375, 320, 300, 250, 240, 200, 150, 125, 120, 100, 75, 60, 50, 40, 30, 25, 15, 5.

The SYN signal frequency (for ADC external triggering mode) can be equal to any of the above, but not more than 400,000 Hz. The SYN signal may be not periodical, the main condition **is that the time interval between active ADC triggering differentials is not less than 2.5 µs**, otherwise it may lead to a failure of the data flow from the module, in which case a restart of data acquisition from the module will be required. *The active transition of the SYN synchronization signal* can be either a front or a fall, which is programmable.

During the internal synchronization, ADC is triggered for the first channel in the order written in the control Table , and then the periodic data acquisition is performed with the set frequency of the ADC start for the following channels in accordance with the control Table .

During the external synchronization, ADC is triggered upon receiving each incoming external triggering pulse (SYN signal), and the **delay in the ADC triggering relatively to the SYN signal is negligible (about 20 ns) and** does not depend on the data acquisition frequency. Similar to the internal synchronization, the channels are polled in this case according to the control Table .

Unlike the SYN signal processed by hardware, the START signal (external data acquisition start) *is* an AVR interruption signal, which is processed by the AVR controller program in the external triggering waiting mode is this mode is set. This is a signal for AVR to start the data acquisition. The START signal should be used when the start time of the data acquisition relatively to the front (or to the fall) of the external TTL -signal must be known with an accuracy of up to several microseconds. **The delay in starting the data acquisition relatively to the SYN signal, unfortunately, depends on the set data acquisition frequency** (this is connected with the specifics of PWM- controller programming in the AVR) **but it is determined by a known constant delay** which is indicated in the document "LTR Crate System. Programmer manual [1]

All performance characteristics of LTR11 module are summarized in Appendix A.1, page 324.

[1] For stability of frequency of the reference oscillator, see Appendix A.16, page 210

5.3.2 Time diagram of the data acquisition process

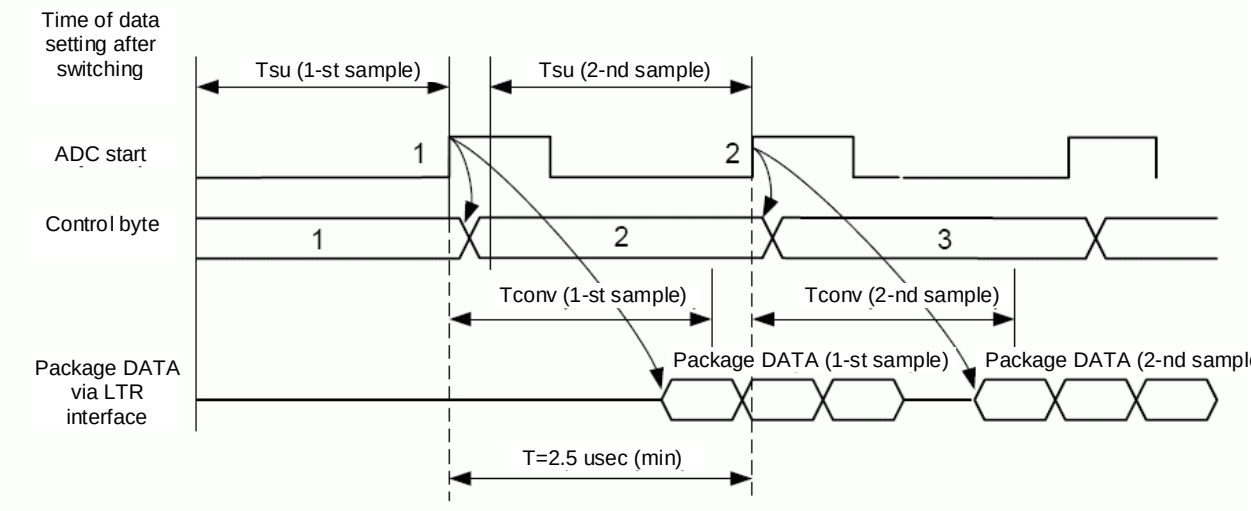


Fig. 5-3.
Time diagram of the process of ADC triggering and data output to the crate controller

In this section, the block scheme of LTR11 (paragraph 5.3.1, page 97) is further considered; in addition, here we will examine the time diagram for the processes run in the data acquisition hardware.

The ADC triggering signal shown in the diagram can be either internal or external. The timing for setting the T_{su} signal (about 2 μs) is necessary for the termination of the transient process in the analog path. At the moment of ADC triggering (conditionally shown on the front of the - corresponding signal), the following events occur in the data acquisition hardware:

- the internal ADC data sampling and storage device is triggered, "locking" the input data, and ADC starts the internal conversion process, the duration of which is T_{conv} (about 2 μs);
- the hardware starts issuing a DATA packet via the LTR interface. The last two bytes in the packet are the digitized ADC sample that is read from the ADC after the end of the conversion process, the duration of which is T_{conv};
- reading of the control byte related to the next sample from the FIFO.

5.3.3 LTR11 module control

5.3.3.1 Basic commands of LTR- interface in application to LTR11 module

Protocol of LTR- modules is described in paragraph4.6.3, page 83. Herein , the device-dependent part of this protocol in the context of LTR11 is detailed. The full description of LTR11 commands is given in the document *"LTR Crate System. Programmer's Manual"* [1].

As well as for the rest modules, STOP, RESET, PROGR commands are purely hardware commands at which the micro controller in LTR11 module is passive. When host-computer sends the very first INSTR command, LTR11 switches-over to the *operating cycle* in which the micro controller is activated and implements all data collection and control processes in LTR11.

Since LTR11 *is* ADC, it does not support data stream to output and *DATA data packets may not be sent to LTR11*.

Let us consider in detail the DATA data packet format in the context of LTR11 module.

LTR11 ADC data packet			
0	**NNMM CCCC**	**sssd dddd**	**dddd dddd**
<24>	**<23..16>**	**<15..8>**	**<7..0>**

Here, **NNMMCCCC** is the control byte, and **sssddddddddddddd** is the ADC sample extended to 16- bits, in which **sss** is the extended character of the additional code (this is a 2-byte integer format with a range of values limited from +8191 to- 8192).

In **NNNVVVCC** control byte the fields are interpreted as follows: **NN**- is ADC sequence rolling sample counter value, and **CCCC**, MM are the channel number code and the channel switching mode, respectively, according to Table 5-1.

Table 5-1. Modes of LTR11 channel switching

MM	Channel switching mode
0 0	Differential 16-channel mode Numbers of LTR11 channels from 1 to 16 are encoded in CCCC field (code from 0 to 15, respectively)
0 1	The mode of measuring the intrinsic zero-point voltage (is independent of the CCCS field)
1 0	Single-phase 32-channel mode. Numbers of LTR11 channels from 1 to 16 are encoded in CCCC field (code from 0 to 15, respectively)
1 1	Single-phase 32-channel mode. Numbers of LTR11 channels from 17 to 32 are encoded in CCCC field (code from 0 to 15, respectively)

LTR11 hardware assigns zero value to the sequential ADC rolling sample counter when module is initialized by RESET command. The counter is incremented every time when DATA packet is sent from LTR.

5.3.4 Test modes for checking the input circuits of LTR11 module

To check the integrity of the input circuits in LTR11 module, there are special test modes under which current is supplied from the internal reference voltage source to the input signal circuit of the selected channel in the single-phase or differential mode.

In the normal operation mode, the input current of LTR11 and leakage currents are negligibly small, therefore, the through resistance of the input channel switch can be neglected. For this case, the equivalent diagram of the input circuits in the differential and single-phase modes is given below.

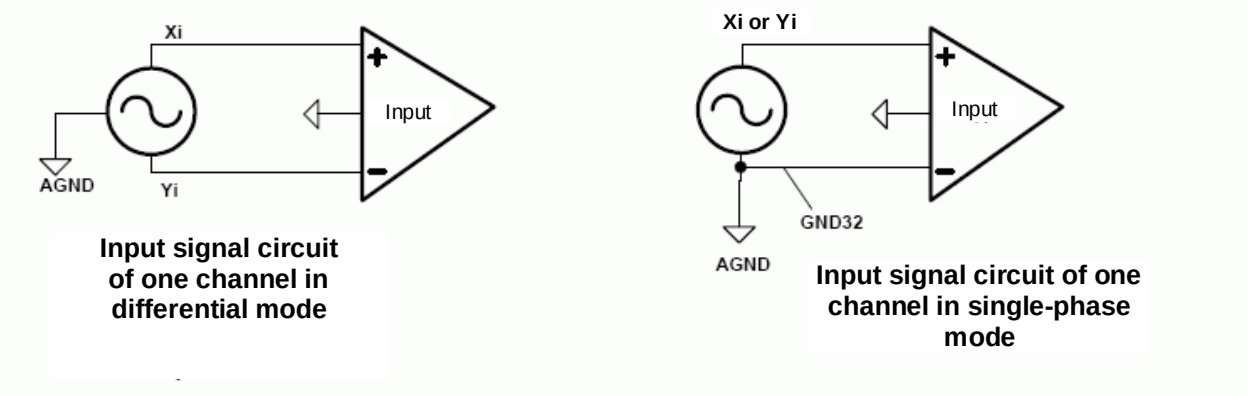


Fig. 5-4. Diagram of the input circuits of LTR11 module

To check the integrity of the input circuits (for breakage or short circuit) of LTR11, there are - four circuits for current supply to the signal circuit for the differential mode and, similarly, four circuits for the single-phase mode. Current is supplied from one of two 67 mV or 2.5 V reference sources only to the selected channel. In the unselected channel, the signal circuit current remains

zero. In Fig. Fig. 5-5 the electrical equivalent input circuit diagrams are shown for all eight cases of using the test modes.

The most common failures of the input lines are ground short circuits of the signal source or line breakage. In Table 5-2, the estimated readings of the calibrated LTR11module are presented for the extreme cases of dead short circuit (short circuit of all lines to the AGND circuit) and the complete breakage (all signal lines are broken)

Table 5-2. LTR11. Control readings in the test mode (typical values)

Test mode	Readings in case of dead short circuit	Readings in case of complete breakage
"0" differential	57 mV	67 mV
"1" differential	-57 mV	-67 mV
"2" differential	-879 mV	-5000 mV
"3" differential	879 mV	5000 mV
"0" single-phase	57 mV	67 mV
"1" single-phase	0 mV	-67 mV
"2" single-phase	0 mV	-5000 mV
"3" single-phase	879 mV	5000 mV

Since in real applications of the LTR11 module the internal resistance of the signal sources as well as the potentials on the input lines can be different at the time of testing, the general description of the input circuits models for generalized differential and single-phase signal sources would be quite cumbersome. Therefore, you have an opportunity, using the equivalent diagrams of input circuits shown in Fig. Fig. 5-5, consider different cases of input circuit failures for your specific connection of LTR11 module and build on this basis your own signal circuit models and the algorithms for their testing.

! L-Card does not provide ready upper-level software for calculating the resistance of user signal circuits. In fact, the user is provided with equivalent electrical diagrams of the LTR11 input in the test modes, and the software functionality to set these test modes. The user shall make all other calculations and write the software for monitoring the input lines.

When building an algorithm for checking the input lines, it should be noted that a particular test mode is set in LTR11 after the issuing of a corresponding command to LTR11 module, and therefore, to speed-up the algorithm before setting the current test mode, the user has to set at once the channels that are to be tested in this test mode in the module's control Table and then run this test mode for all necessary channels.

Particular attention should be paid to the *accuracy of the given input circuits model.* The above equivalent diagrams contain elements of different accuracy. The most inaccurate element in this measuring diagram (the 45 Ohm resistor) has an error of ± 50%, which is due to a large possible spread of the open channel resistance of the analog switch, the 180 Ohm resistor has an error of ± 15%, since it is partially formed from the switch resistance, and the total error of the remaining elements of the circuit is about ± 5%. These accuracies should be kept in mind when selecting the test modes and fault finding algorithms for the input lines.

5.4 Connection of signals

Read the general rules for signal connection, paragraph 3.6.6, page 58.

LTR11 module has DRB37M- panel-mount connector for connection of input signals. External connections to LTR11 must be implemented by connecting signal circuits to the cable part of the connector (DB-37F type). Signal applications are given in Table 5-3 and the view of the panel-mounted connector is presented in Fig. Fig. 5-6, page 108.

Table 5-3. Application of signals of LTR11 user connector

Signal name	Common point	Direction	Description
AGND	–	–	Analog ground
GND32	AGND	Input	– In the single-phase mode: common inverting input for channels 1...32 – In the differential mode, must be connected to AGND to enhance the noise immunity – For all modes, the operating voltage range is ±10 V
X <1...16>	AGND	Input	–Non-inverting voltage input for channels 1...16 for the differential and single-phase modes – Operating voltage range: ±10 V – It is recommended to connect non-used X <1...16> inputs to AGND
Y <1...16>	AGND	Input	– Inverting voltage input of channels 1 ... 16 for the differential mode – Input of channels 17...32 for the single-phase mode – Operating voltage range: ±10 V – It is recommended to connect non-used Y <1...16> inputs to AGND
SYN	AGND	Input	ADC synchronization input in the external synchronization mode of LTR11. It is compatible with output logic level TTL/CMOS- of elements with +5 V power voltage. If it is not required to use the external synchronization input, it can be not - connected. The input has 20 kOhm pull-up resistor to +5 V internal module circuit.
START	AGND	Input	Data collection start input in LTR11. Compatible with output logic level TTL/CMOS -of elements with +5 V power voltage. If it is not required to use the external synchronization input, it can be left unconnected. The input has 20 kOhm pull-up resistor to +5 V internal module circuit.

5.4.1 Characteristics of signal line inputs and outputs

When connecting LTR11 module to your system, strictly observe the parameters specified in Table s of this section.

! The manufacturer shall not be warranty liable for a LTR11 failure caused by a violation of maximum permissible operation conditions.

The following symbols are given in Table s of this section:

AI – analog input,

DI – digital input.

Note that the impedance of input lines is significantly higher in LTR11 *operation mode* than in the *switched-off module state*. For *further information on module switched-* off state see paragraph 4.8, page93.

The characteristics of galvanic isolation in LTR are given in Appendix A.18, page362.

5.4.2 LTR11 operating mode

LTR11 module installed in LTR crate has the following characteristics of input and output signal lines after LTR crate is powered on:

Table 5-4 Maximum permissible conditions when module LTR11 is on.

Signal	Type	Input impedance	Maximum permissible conditions at input	Pull-up resistor
GND32, X <1...16>, Y <1...16>	AI	– Not less than 10 Mohm for single-channel mode. – Variable resistive-capacitive for multi-channel mode	±27 V at inputs X <1...16>, Y <1...16>, GND32 relatively to AGND circuit	absent, **see the important note (!)** after the Table
SYN, START	DI	20 kOhm	-0.5...+5.5 V relatively to AGND	20 kOhm[1]

! No certainty of the state of the unconnected inputs X, Y, GND32 is guaranteed.

The potential at unconnected high-resistance inputs X, Y, GND32 is determined by nano-ampere leakage currents which may be different in different modules.

For the *multi-channel* mode, the input impedance of the channel is less than 5 MOhm and has a variable resistive-capacitive nature due to the effect of recharging the *capacity of the input switch of* LTR11. This transient process starts at the moment of the channel switching and terminates at the time which depends on the internal resistance of the signal source. From the above it follows that the inter-channel passage and the dynamic error in the multi-channel mode depend on the source signal resistance, the ADC frequency and the set range of the LTR11 module.

The typical values of inter-channel passage of 1 kHz sinusoidal signal depending on the range, the frequency of ADC triggering and the internal resistance of the signal sources (50 Ohm, 5 kOhm, 20 kOhm) are given in the relevant sections (0– Specification, page 324).

[1] starting from version 4 of the LTR11 module and older (the LTR version numbers are described in paragraph 3.5, page 30), the pull-up resistors on the SYN and START lines are made to zero, while in versions 3 (and under) these lines were pulled to one. The version number of the module is the first digit of its serial number

5.4.3 LTR switched-off state

For *further information on module* switched-off state, see paragraph 4.8, page 93.

In this mode, LTR11 module is de-energized and impedance of analog and digital input lines is low in comparison with the operating mode.

Table 5-5.
Maximum permissible conditions of signal lines for LTR11 which is powered off

Signal	Type	Input impedance	Maximum permissible conditions at input	Pull-up resistor
GND32, X <1...16>, Y <1...16>	AI	min. 1 kOhm	±16 V at inputs X <1...16>, Y <1...16>, GND32 relatively to AGND	
SYN, START	DI	Not less than 200 Ohm relatively to AGND	-0.5...+5.5 V relatively to AGND	

5.4.4 Additional important requirements to LTR11 signal sources for the multi-channel mode

Because the analog switch is installed directly at X, Y and GND32 inputs, *the user must observe the additional rules for connection of LTR11, if the multi-channel mode is to be used.*

In the multi-channel mode, the switch operation is dynamic, and channels are switched with a frequency equal to the programmed ADC frequency. For example, for the ADC frequency of 400 kHz, the time from the switching to the ADC sampling and storage device triggering is 2.5 μs. The inter-channel passage will be small if during this time the transient process[1] in the input circuits of LTR11 is completed. The transient process duration depends directly on the impedance of the signal source relatively to LTR11 inputs, as well as to the length of the lines. Thus, *for the ADC frequency of 400 kHz in the bands ± 10 V or ± 2.5 V, the length of wires to the signal source must not exceed 1.5 meters, and the si-gnal source resistance in the frequency band to 2 MHz should not exceed 1 kOhm for inter-channel signal passage less than -75 ... 80 dB* in the differential mode. For smaller ADC frequencies, the allowable wire lengths and the output resistance of the signal source will be greater to obtain the same inter-channel passage.

For less input ranges, the inter-channel passage will also increase due to an increase in the time required for transient process setting in the analog path at higher gain factors.

There is another *negative factor that can dramatically affect the inter-channel passage and lead to the signal distortion. This is the case when the set input range is exceeded*. Imagine that an input 10 V signal is sent to the input of a channel with a set range of ± 2.5 V. Having received such a signal, the amplifier will enter to a limitation (i.e., a non-linear mode) mode, and the output from such a state requires additional time. This can create additional distortions in the next (according to the polling order) channel.

Below **are the necessary steps to obtain the minimum inter-channel passage and prevent signal distortion:**

- Ensure the lowest impedance of the signal source, if this is possible for your task
- Ensure the shortest wire length to the signal source and the smallest source capacity
- Select the lowest ADC frequency, which is accepTable for your task
- Select the largest input range that is suiTable for your task

[1] caused by the phenomenon of charge injection in an analog key at the moment of switching

- Do not exceed the set signal range
- Exclude polling of a channel which lines are not connected
- If there is a choice between applying differential or single-phase connection, always select the differential connection
- Apply the special case of connecting *current* input signals (Fig. 5-8, page 109), if this is possible for your task

In Appendix A.1.2, page 325, quantitative characteristics are given that allow for assessing the effect of switching noise in the multi-channel mode on the inter-channel passage. It should be noted that these characteristics relate to the case of a short LTR11 connection to the signal source in the differential mode (the source resistance is purely active in the wide frequency band, the wire length to the signal source is small and can be neglected).

In case of multi-channel signal input, the input capacitance of the analog path switches C_{in} ~ 100 pF must be taken into account.

The switching error of the analog path causing the parasitic inter-channel passage will not exceed the inherent ADC error if the following criterion is met[1]:

$$R_1 \cdot C_{in} \leq 0.1 \cdot \tau_{ADC}$$

where:

- $R_1 = R_s + R_z$, R_s *is* the output resistance of the signal source, R_z = 1 kOhm is the input protective resistance of the module
- τ_{ADC} *IS* the ADC operating interval

The typical values of inter-channel passage of 1 kHz sinusoidal signal depending on the range, the frequency of ADC triggering and the internal resistance of the signal sources are given in Appendix A.1.2, page 325.

It should be taken into account that the given values of the inter-channel passage are measured for the case of a purely active internal resistance of signal sources. But in practice**, the factor of internal resistance of signal sources at high frequency** is of great importance for the multi-channel mode, since the switching processes on LTR11 analog inputs are run with high frequency.

! When working with the module, it should be taken into account that the bandwidth of the analog input LTR11 channel is significantly higher than the maximum frequency of the ADC operation.

Therefore, to ensure the spectral accuracy of the signal conversion, the input signal band must be limited, if possible, in accordance with the Nyquist criterion, starting with a frequency of 0.5 • f_s[2] and higher. Otherwise, all noise and interference with a frequency above 0.5 • f_s will be superimposed on the useful signal in the operating frequency band and, most likely, it will be impossible to separate them in the subsequent processing.

5.4.5 Examples of input signal connections

Two most typical connection diagrams for input analog signals are given in Fig. 5-7, page 109[3].

[1] For cases of a large input signal level falling outside the range established for LTR11, and also in case of switching channels with a different set range, a more stringent criterion should be applied taking into account the increase in the inter-channel passage in these cases.

[2] f_s is ADC sampling frequency

[3] The issues on measuring units connecting are described in detail in the article [2]

There is a special case of connecting input circuits, when the length of the input wires does not have a significant effect on the inter-channel passage. In this case, input signals are connected as current sources. In Fig. 5-8, page 109, two cases of such connection for 16- and 32-LTR11 channel mode are shown. In these examples, resistors should have the resistance of 75...500 Ohms (the closer to the wave impedance of the line, the better). In this case, the signal source must ensure the output current necessary for driving the input voltage on the required input range of LTR11. The wire length L does not have a significant effect on the duration of the transient process at the LTR11 input, since the actually low impedance of the signal source is ensured.

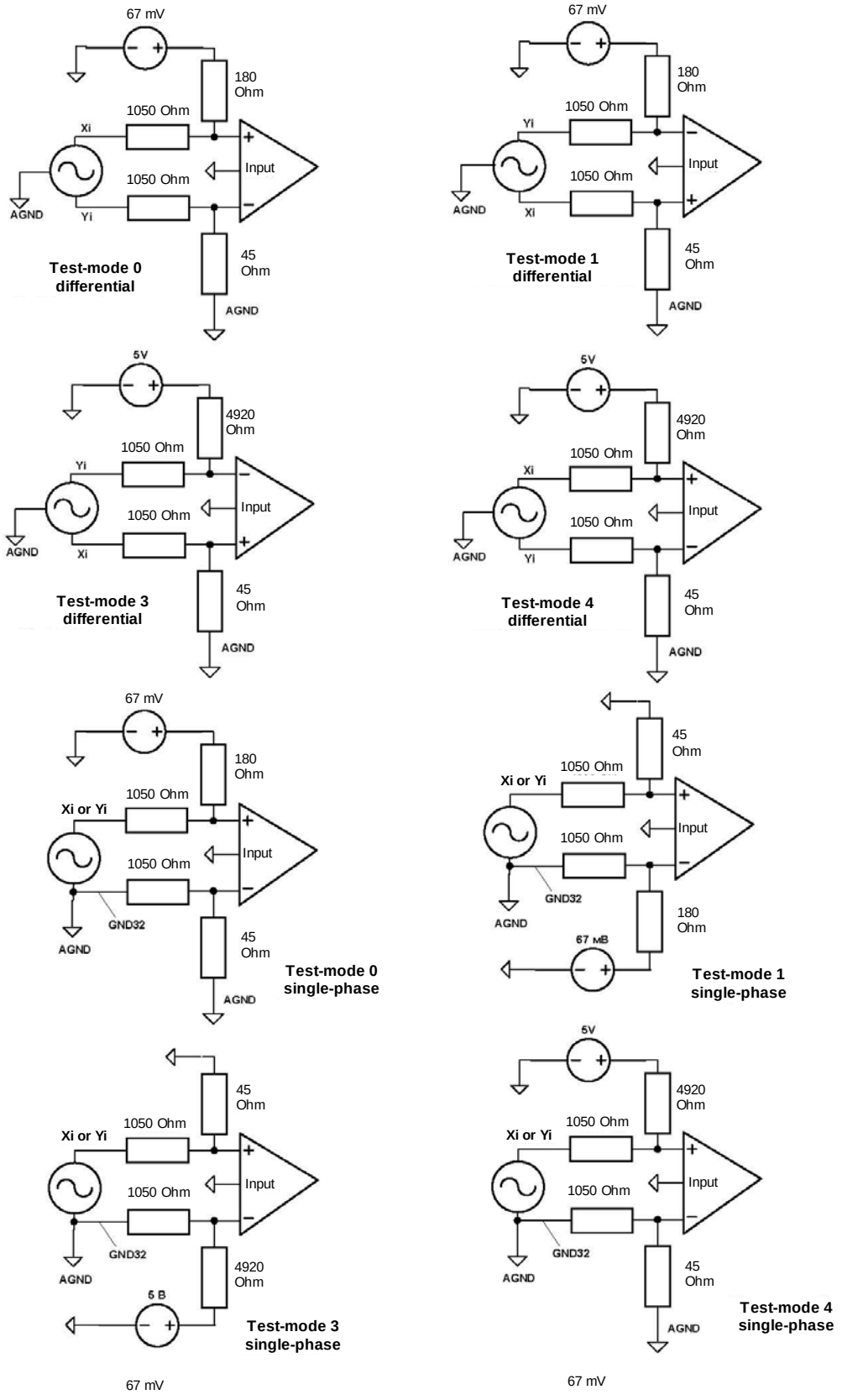


Fig. 5-5. Equivalent diagram of the input circuits of LTR11 module in the test modes for checking the input lines

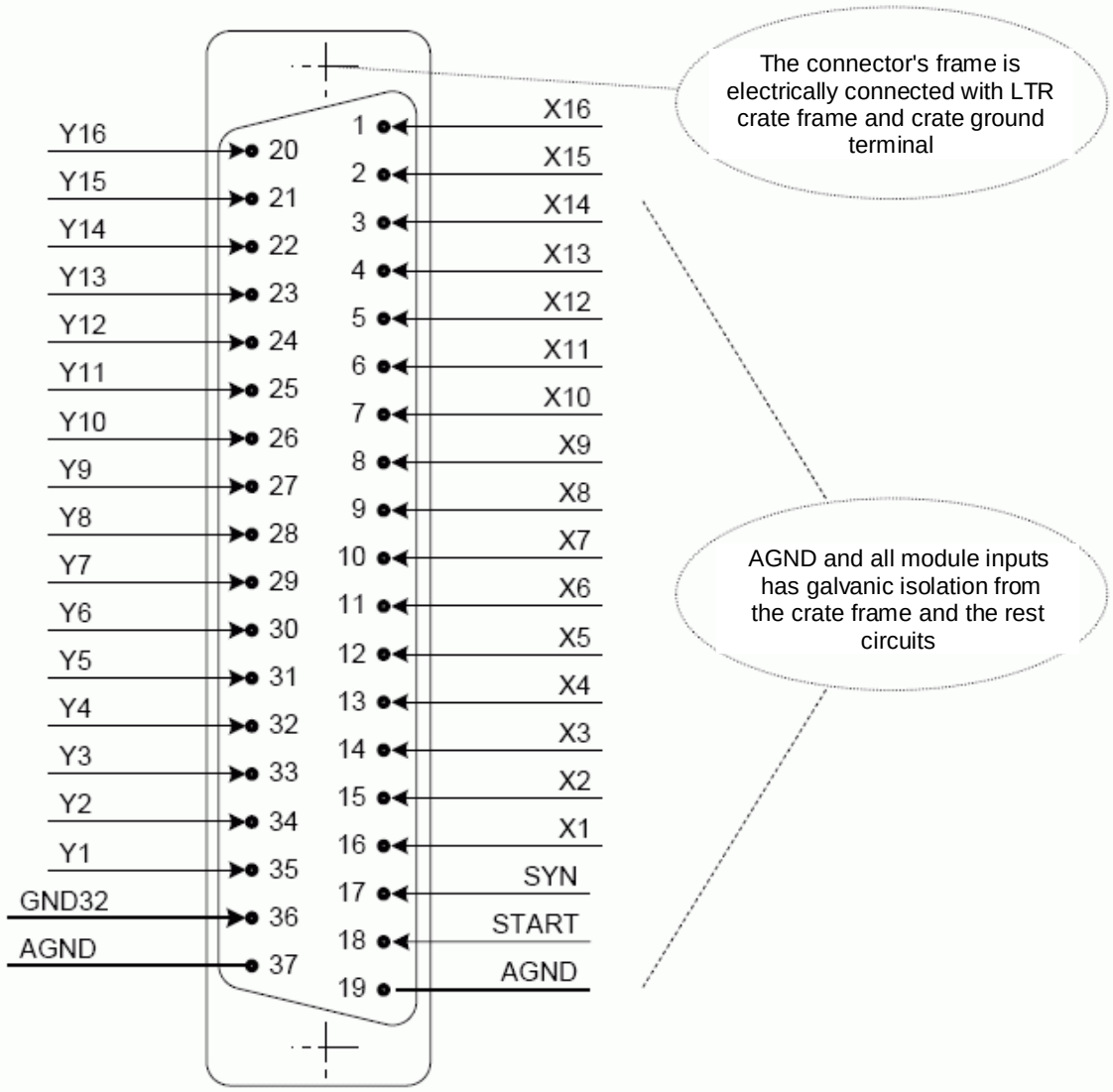
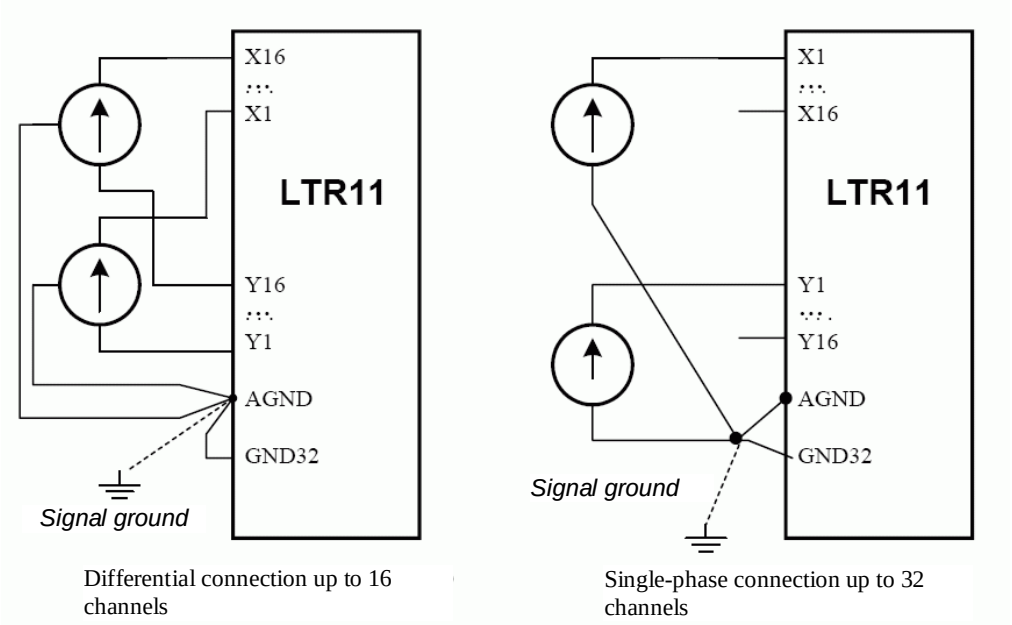


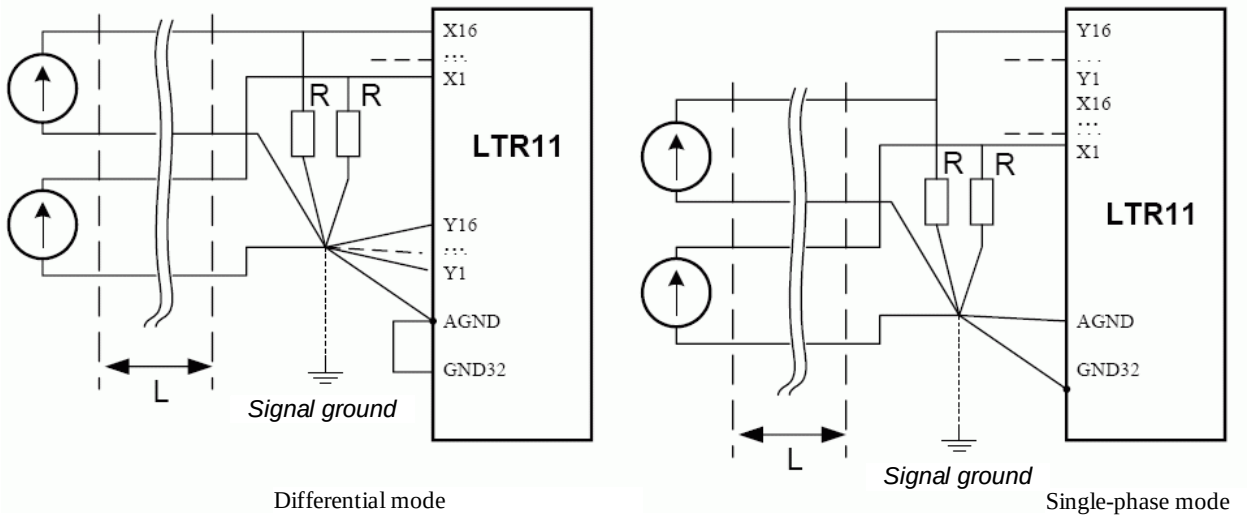
Fig. 5-6. Input signals at LTR11 module connector



Differential connection up to 16 channels

Single-phase connection up to 32 channels

Fig. 5-7
Typical connection diagram for connecting signal sources to LTR11



Differential mode

Single-phase mode

Fig. 5-8
Special case of connecting current input signals

Chapter 6. LTR212, LTR212M-1, LTR212M-2, LTR212M-3 strain-gauge modules

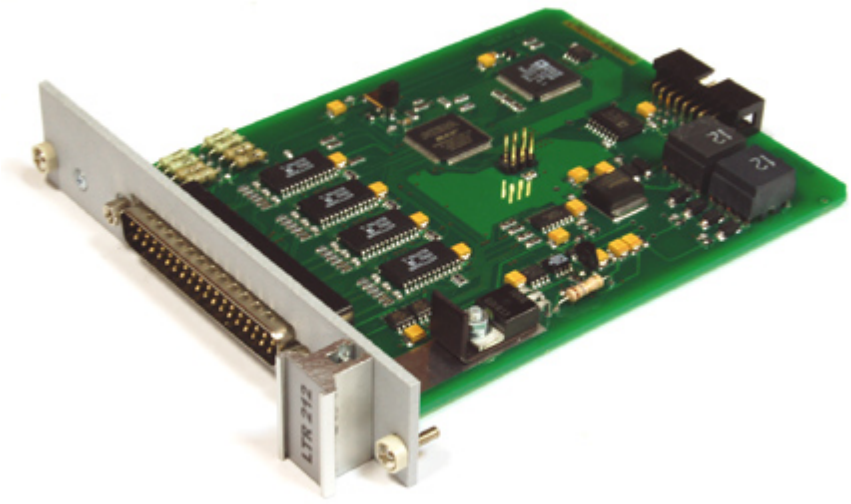


Fig. 6-1. LTR212 view

6.1 General description of LTR212

6.1.1 Device assignment

LTR212 module is designed for use in precision strain-gauge applications. The LTR212 module can be used in various connection diagrams for up to 8- strain gauges with a resistance of 100...1000 Ohm for static and dynamic measurements.

6.1.2 General information about LTR212

- LTR212 supports up to 8 strain-gauge channels.
- The software-switched reference voltage source (+5 V or +2.5 V) allows for connecting up to 8 strain gauges with a resistance of 100 Ohm each.
- Digital filtering in ADSP-2185M signal processor.
- Full compatibility of contacts of the input connector with LC-212.
- This module in terms of functionality is similar to LC-212, but it is implemented on a more modern element base. Unlike the old one, the *new strain-gauge module is galvanically - separated from the crate ground.*

L-Card (based on the results of generalization of users' wishes for the entire history of the release of LC-212 and LTR212 modules) launched the production of new modifications of LTR212M-1, LTR212M-2, LTR212M-3 in 2013. The full list of differences in the module

modifications is presented in a brief tabular form in paragraph 6.1.3. Hereinafter, these differences are considered in more detail.

In the description, the following abbreviated designations are introduced:
"LTR212" is the old modification which was produced until 2013
"LTR212M" are all new modifications of LTR212M-1, LTR212M-2, LTR212M-3
"LTR212(M)" are all modifications: LTR212, LTR212M-1, LTR212M-2, LTR212M-3

6.1.3 Differences between LTR212M and LTR212.

Consumer properties	**LTR212**	**LTR212M -1**	**LTR212M -2**	**LTR212M -3**
Synchronization of ADC conversion frequency with the frequency of the reference generator of LTR crate	–	+	+	+
Possibility of synchronous start of data collection with other LTR modules	–	+	+	+
Compatibility with old BIOS 1.1	+	–	–	+
Compatibility with new BIOS 2.0	+	+	+	+
Compatibility with old upper-level software at the level of API functions	+	+	+	+
Non-volatile memory	256 B EEPROM	0.5 MB Flash memory	0.5 MB Flash memory	256 B EEPROM
Calibration for 5 V RVS	+	+	+	+
Calibration for 2.5 V RVS	–	+	+	–
Test mode for creating a controlled unbalance of quarter bridges	–	+	–	–
Software-distinguished modifications (after downloading new BIOS 2.0):	1) Modification LTR212M-1 2) Modification LTR212M-2 3) Modification LTR212 / LTR212M-3 (see the note below)			

Note: LTR212 / LTR212M-3 modifications are not software-distinguished.

In any case, the identification at the upper software level is possible with referencing to the unique serial number of the module.

Supported connection diagrams	LTR212	LTR212M -1	LTR212M -2	LTR212M -3
Up to 4 full bridges in 4-channel mode (fig. 6-7) in 4- or 6-wire diagram	+	+	+	+
Up to 8 full bridges in 8-channel mode (fig. 6-8) in 4- or partially 6-wire diagram	+	+	+	+
Up to 4 half bridges in 4-channel mode (fig. 6-9) in 3-wire diagram	+	+	+	+
Up to 4 half bridges and 4 full bridges in 8-channel mode (fig. 6-10) in the mixed diagram	+	+	+	+
Up to 4 quarter bridges (see the note below) in 4-channel mode (fig. 6-11) in 3-wire connection diagram	–	+	–	–
Up to 4 half bridges (see the note below) and up to 4 full bridges in 8-channel mode (fig. 6-12) in the mixed connection diagram	–	+	–	–

Note: 200 Ohm or 350 Ohm quarter bridges (must be the same), or 180 ÷ 1000 Ohm quarter bridges (can be different), under the condition of soldering the balancing resistors on the mezzanine board (supplied with LTR212M-1) by the user. For quarter bridges, the test mode of controlled unbalance is supported.

6.1.4 LTR212(M) module configuration

LTR212 basic configuration is described in paragraph 2.4, page 29.

6.2 Installation and set-up

During LTR212(M) installation in crate, observe the module installation rules common for LTR system, see paragraph 3.6.2, page 51.

LTR212(M) board has one process -6-pin connector.

Do not put jumpers on process connectors and carry out any external connecting to them!

LTR212H mezzanine board (paragraph 6.5, page 131) supplied with fasteners can be pre-installed on the main board of LTR212M-1 module.

6.3 Overview of LTR212(M) hardware components and operation principles

6.3.1 LTR212(M) application.

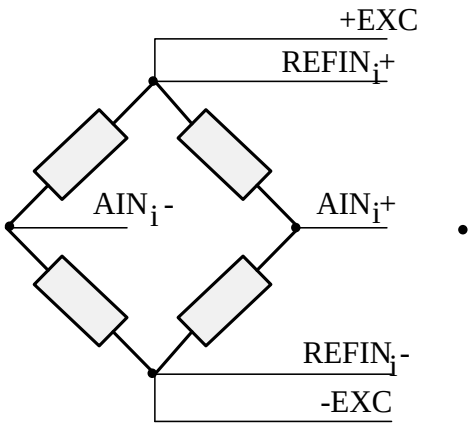


Fig. 6-2. LTR212(M). i-th channel bridge (common case)

LTR212 (M) measures the unbalance of the full bridge (fig. 6-2) connected to the i-th input. Even if the half- or quarter-bridge connection diagram is used, LTR212 (M) measures the unbalance of the full bridge, somehow extended to the full bridge in all the connection diagrams described below. In the figure, + EXC, -EXC circuits are high-current supply circuits of the bridge and the rest are low-current measuring circuits.

The value of the bridge unbalance Δ measured by LTR212 (M) is calculated according to the formula:

$$\Delta = \frac{U^+_{AIN} - U^-_{AIN}}{U^+_{FEFIN} - U^-_{REFIN}} * U_{REF}$$

In this formula:

$U^+_{AIN} - U^-_{AIN}$ is the voltage difference between AIN_i+ and AIN_i– signal outputs of the bridge.

$U^+_{REFIN} - U^-_{REFIN}$ is the difference of applied voltages between the $REFIN_i$+ and $REFIN_i$– bridge power supply points.

U_{REF} is the rated voltage of the bridge power supply equal to U_{REF}5.0 V or 2.5 V. It should be particularly noted that U_{REF} is the "ideal" rated voltage value and not the real measured value$U^+_{REFIN} - U^-_{REFIN}$.

In general, the value of relative unbalance is dimensionless $\frac{U^+_{AIN} - U^-_{AIN}}{U^+_{FEFIN} - U^-_{REFIN}}$ but in this case it is translated into Volts by multiplying by the "ideal" value of the rated supply voltage of the bridge. Specifically, the readings of LTR212(M) device are expressed in Volts.

It is important that the range of compensation for the initial bridge unbalance in LTR212(M) is limited by 1.5% of the bridge supply voltage. In other words, LTR212(M) is able to work with a bridge having an initial unbalance $\Delta_0$within

$$\Delta_0 = \pm 0{,}0075 * U_{REF}$$

On the other hand, if the initial unbalance exceeds the above limits, then external additional resistive bridge elements can be used to "push" the actual initial unbalance into the required limits.

6.3.2 How is LTR212(M) calibrated?

In the non-volatile memory of LTR212(M), the factory calibration bridge unbalance factors Δ are stored for all the measurement sub-ranges used for measuring this unbalance (± 80 mV, ± 40 mV, ± 20 mV, ± 10 mV, 0...80 mV, 0...40 mV, 0...20 mV, 0...10 mV) for each of the 8 measurement channels, in LTR212, LTR212M-3 - only for U_{REF} equal to 5 V[1], and in LTR212M-1, LTR212M-2 for U_{REF} equal to 5 V or 2.5 V.

It follows directly from the physical meaning of the unbalance Δ (paragraph 6.3.1) that Δ it does not depend on the bridge connection diagram (full-, half-, quarter-bridge) used by the user because the measured components of the unbalance voltage $U_{AIN}^{+} - U_{AIN}^{-}$ and $U_{FEFIN}^{+} - U_{REFIN}^{-}$ are applied to REFINi ± and AINi ± inputs.

Based on the above, *factory calibration unbalance factors measured relatively to the voltages at REFINi ± and AINi ± inputs of the given LTR212(M) module are recorded in the non-volatile memory of LTR212(M)*.

In the non-volatile memory of LTR212(M) modules there is also a zone for the user "zero" and "scale" factors that the user can record for specific sensors connection conditions (by the example of scales: "zero" means that the weight is removed from the scales, and "scale" means that the standard weight is put on the scales). These factors are called "calibration constants"[2].

6.3.3 Block diagram of LTR212

LTR212 module is implemented on the basis on four AD7730 *sigma-delta* analog-to-digital - converters (ADC) controlled by ADSP -2185M[3] signal processor (DSP).

DSP loading, all data and command exchange are carried out via LTR- module interface.

In LTR212 block diagram, signal processor is the central unit carrying out control and data processing.

The diagram of LTR212 module measuring circuits is shown in Fig. Fig. 6-3. Here, X1- is the user module connector (for convenience of the representation on the block diagram it is divided into two elements X1:1 and X1:2); DA1, DA2, DA3, DA4- AD7730 converters, R1, ..., R8- precision resistors (1 kOhm- 0.1%- 5 ppm/° C- 0.125 W) forming half-bridge additional circuits that can be powered and used for extension of external strain gauge connection circuits to the full-bridge circuit in the case where external circuits do not form a full bridge; ION (designation on the diagram: REF) *is* 5 V or 2.5 V reference voltage U_{REF} (controlled by DSP); four electronic keys (K1-1, K1-2, K2-1, K1-2) controlled by DA1 which allow for setting constant or alternating voltage value for the ION for measuring circuits. Electronic keys K2-1 and K2-2 are always controlled synchronously in one phase, and keys K1-2, K1-2 are controlled synchronously in phase opposition. In the alternating mode, switching is periodic. When the alternating mode is disabled, K2-1 and K2-2 keys are always closed, and K1-1 and K1-2 keys are always open.

AD7730 ADCs have two differential signal inputs AIN1 ± and AIN2 ±, a differential reference voltage input REF ±, and two internal digital filters. The second filter is a 22-order

[1] Historically, there was no space for calibration coefficients at U_{REF} = 2.5 V in the non-volatile memory of LTR212. In LTR212M-3, this problem has remained in order to ensure the compatibility with the old BIOS 1.1.

[2] In the old LTR212 documentation, this was incorrectly called "user calibration factors".

[3] AD7730, ADSP-2185M *are* components of Analog Devices. Technical data can be found at www.analog.com

feedback filter- and can be disabled. ADC input signal ranges: ±80 mV, ±40 mV, ±20 mV, ±10 mV, 0...80 mV, 0...40 mV, 0...20 mV, 0...10 mV.

ADCs have built-in zero and range calibration functions that are performed at the software level. The calibration parameters are saved in the Flash memory- of the module until the they are changed for the next time.

ADCs have a built-in 6-digit digital-to-analog converter (DAC) designed to shift the level of the input signal by about ± 78 mV (at 5 V bridge supply voltage) or up to ± 38 mV (at 2.5 V supply voltage).

All strain gauges are powered from the ION via a switch. The switch can produce alternating voltage with a frequency equal to half the data acquisition frequency or translate constant voltage from the ION.

The ION with the switch provide the maximum operating current of 400 mA and current protection limiting the output current to about 500 mA.

Output signals of the strain gauges are fed directly to ADC inputs in AD7730. Reference ADC voltage is the measured (at REFIN inputs) voltage supplied to the sensors. It should be noted that both channels in AD7730 have common inputs REFIN1 ± ... for reference voltage measuring. REFIN4±.

It is critically important to understand that AD7730 converter works only with full-bridge sensors, therefore ALL the connection diagrams for half-bridge and quarter-bridge sensors considered below are in fact diagrams of extension to the full-bridge diagram (with internal resistors for full-bridge extension).

The analog-to-digital converter is controlled by ADSP-2185M signal processor via a serial interface. This interface has a synchronization line ensuring the simultaneous start of all four converters.

All performance parameters of LTR212 module are summarized in Appendix A.2, page 327, and its operating modes are described below. In Appendix A.2.2.1, page 328, the frequency-response characteristics are also presented.

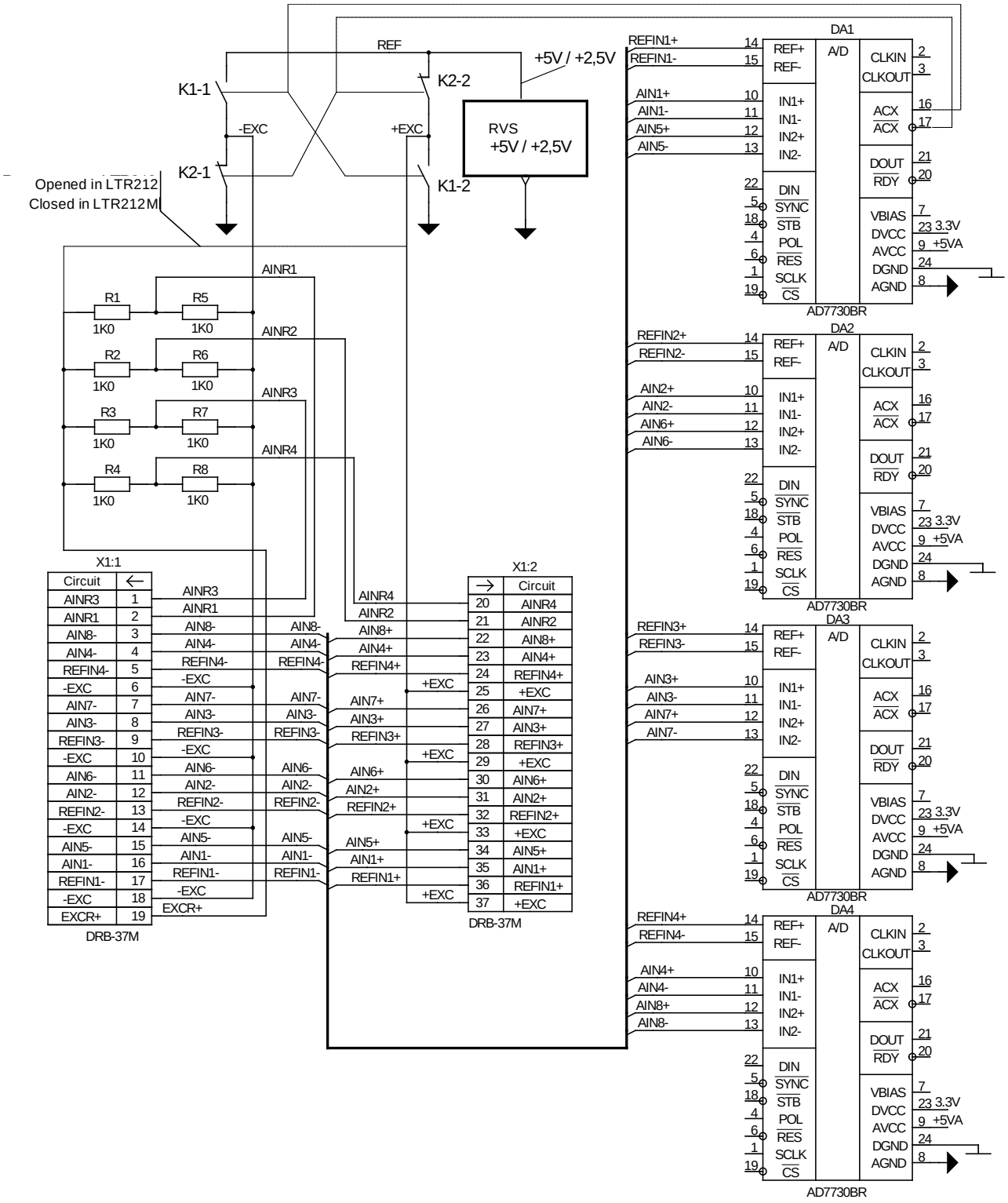


Fig. 6-3. Measuring circuits of LTR212, LTR212M-2, LTR212M-3

6.3.4

6.3.5 Block diagram of LTR212M-2, LTR212M-3

The diagram of measuring circuits of LTR212M-2, LTR212M-3 (Fig. Fig. 6-3) is different from LTR212 with the following:

- +EXCR and +EXC circuits have been combined. + EXC circuit has been connected to pin 19. Therefore, the internal half-bridge circuits R1 ... R8 are permanently connected inside LTR212M-2 and LTR212M-3 (paragraph 6.3.7). In any case, the wiring made for LTR212 would be completely suiTable for switching to LTR212M-2 and LTR212M-3, because even if the internal half-bridges were not in your module, this difference will not affect the measurement accuracy and the operation of the module as a whole.
- The initial accuracy of internal half-bridge resistors has been increased: instead of 1 kOhm – 0.1% – 5 ppm/°C – 0.125 W resistors are used 1 kOhm – 0.05% – 5 ppm/°C – 0.125 W resistors.
- ADC conversion frequency in LTR212M-2, LTR212M-3 is synchronized with the frequency of LTR reference oscillator, and therefore synchronized with the conversion frequencies of the remaining LTR modules, except for the old LTR212.

LTR212M-2 has 0.5 MB internal Flash memory. LTR212M-3 has 256 B EEPROM compatible with the old BIOS.

There are no other differences between the measuring circuits and measuring paths of LTR212M-2, LTR212M-3 from those of LTR212.

6.3.6 Block diagram of LTR212M-1

The diagram of measuring circuits of LTR212M-1 (fig. 6-4) is different from LTR212 with the following:

- +EXCR and +EXC circuits have been combined. + EXC circuit has been connected to pin 19. Therefore, the internal half-bridge circuits R1 ... R8 are permanently connected inside LTR212M-2 and LTR212M-3 (paragraph 6.3.7). + EXC circuit on the pins of connectors 37, 33, 29, 25 is divided, respectively, to sub-circuits + EXC1, + EXC2, + EXC3, + EXC4. - These significant differences, from the point of external connections, are marked on the diagram fig. 6-4 with exclamation marks (!).
- When programmable analog keys K3-1, K3-2, K3-3, K3-4 are closed, the + EXC circuit is connected to the + EXC1, + EXC2, + EXC3, + EXC4 circuits at the connector, and in this case the measurement circuit corresponds to the old capabilities of LTR212 from the point of view of connecting half-bridge and full-bridge sensors.
- When programmable analog keys K3-1, K3-2, K3-3, K3-4 are opened and when K4-1, K4-2, K4-3, K4-4 or K5-1, K5-2, K5-3, K5-4, or K6-1, K6-2, K6-3, K6-4 are closed, LTR212M-1 module is in the quarter-bridge measurement mode for the quarter-bridge resistance of 200, 350, or 180...1000 Ohm, respectively. In these cases, main resistors (R14...R21) used for extension to half-bridge operation are used on the main board of LTR212M-1 (200, 350 Ohm) or on the mezzanine board of LTR212H (180...1000 Ohm "USER" resistors pre-soldered by the user). It is possible to install only the same switching for 4 channels because of the dependence of the control of groups of keys K4, K5, K6.

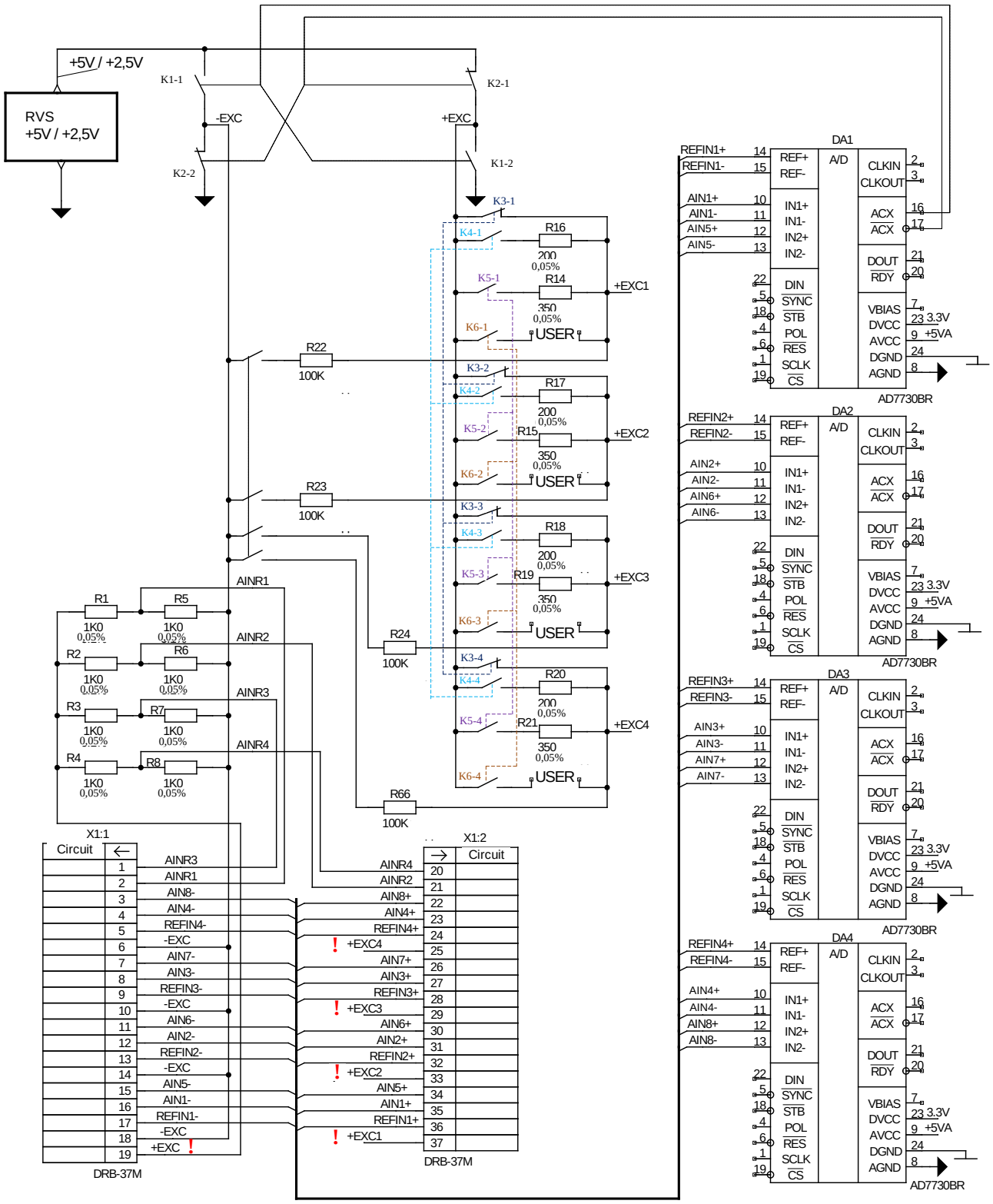


Fig. 6-4. Measuring circuits of LTR212M-1

- Independent software-controlled analog keys K7-K9, connecting resistors R22-R24, R66 with a resistance of 100 kOhm ± 1% to the quarter-bridge of each of the 4 channels are used to implement the test mode of creation of the quarter-bridge unbalance.

- The initial accuracy of internal half-bridge resistors has been increased: instead of
  1 kOhm – 0.1% – 5 ppm/°C – 0.125 W resistors are used
  1 kOhm – 0.05% –5 ppm/°C – 0.125 W resistors.
- ADC conversion frequency in LTR212M-2, LTR212M-3 is synchronized with the frequency of LTR reference oscillator, and therefore synchronized with the conversion frequencies of the remaining LTR modules, except for the old LTR212.

LTR212M-2 has 0.5 MB internal Flash memory. LTR212M-3 has 256 B EEPROM compatible with the old BIOS.

6.3.7 Note concerning the combining of +EXCR and +EXC circuits into LTR212M .

For the user, permanently connected internal half-bridges in LTR212M (in comparison with LTR212) are not just a feature, but an improvement in the quality of the measuring circuit when working with half-bridges due to the elimination of thermal electromotive force and the resistance of the external contact connection of + EXCR and + EXC circuits. This provides better thermal stability and long-term stability of measurements in LTR212M compared to LTR212 for half-bridge circuits.

6.3.8 Converter operating modes

AD7730 converter has a lot of internal settings, but from the point of view of user tasks it is possible to distinguish *three modes of operation*, which are the result of a *compromise* between the following parameters: *measurement accuracy*, *data acquisition frequency*, and *number of channels*.

Operating modes of LTR212(M), being the result of various compromises between these parameters, are described in Table 6-1.

Table 6-1
Operating modes of LTR212(M): relative advantages and disadvantages

Mode	Relative advantages	Relative disadvantages	Notes
Medium - accuracy mode	High data acquisition frequency	Only 4 channels, medium measurement accuracy	In the old LC-212, this mode was called "statodynamics"
4-channel high accuracy mode	High measurement accuracy	Only 4 channels, medium data acquisition frequency	In LC-212 , this mode was called "statics – 4 channels"
8-channel high-accuracy mode	Large number of channels. High - measurement accuracy	Low data acquisition rate, half of the channels can be connected only with a 4-wire diagram. Data acquisition is not absolutely synchronous	In LC-212, this mode was called "statics – 8 channels"

The internal settings of the four AD7730 converter micro chips for modes listed in Table 6-1 are described in Table 6-2.

Table 6-2
Operating modes of LTR212(M) and internal settings of AD7730

Mode	Interruption mode (CHOP)	Fast response mode (FAST)	Second-stage hardware filter (SKIP)	Software delay of enabling hardware filters (Delay)	Alternating reference voltage (AC)	L-CARD software filters or user filters-
4-channel medium accuracy mode	switched off	switched off	switched off	0	switched off	switched off/on – is determined by the user
4-channel high accuracy mode	switched on	switched off	switched on	0	switched off/on – is determined by the user	
8-channel high-accuracy mode	switched on	switched off	switched on	0	switched off/on – is determined by the user	

6.3.8.1 Mean accuracy mode

4-channel *medium accuracy mode* is designed for measurements with the maximum data acquisition frequency and low requirements to zero-offset voltage. In this mode, each AD7730 converter uses one channel, the second stage digital filter is disabled, the main filtering is performed in the DSP, the measuring bridges are supplied with a constant voltage.

6.3.8.2 4-channel high accuracy mode

4-channel high-accuracy mode is used for static measurements with maximum accuracy. Digital signal filtering is performed by the AD7730 converters. This mode provides for a low level of zero offset and its temperature drift due to ADC switching to the mode of AC measurement according to the "modulator-demodulator" scheme. Depending on the status of the AC control bit, the modulation can be performed either at the input of the converter or at the level of power supply to the measuring bridge.

In the first case (AC = 0), zero offset of ADC is compensated and constant voltage is supplied to the measuring bridges.

In the second case (AC = 1), alternating voltage is supplied to the bridges and the effect of possible thermal electromotive forces, which arise when connecting the measuring bridges to the module, is additionally compensated. However, in this case, an additional error may occur due to the transient process in the signal cable.

The frequency of switching the supply voltage of the bridges is equal to half the frequency of data acquisition.

The expediency of using AC = 1 mode for 4-wire and 3-wire connections is questioned, since the influence of thermal EMFs in these circuits will be less than the influence of other factors. It is more reasonable to use AC = 1 mode for 6-wire circuits. However, it is impossible to provide unambiguous recommendations on application of AC = 1 mode because in case that the contact connections of the wires outgoing from the sensors are in the zone of strong heating, then the thermal EMF factor of these connections can become significant.

6.3.8.3 8-channel high-accuracy mode

This mode is a modification of 4-channel high accuracy mode and is used for doubling the number of channels. In this mode, both AD7730 signal inputs are used. The working algorithm is the following:

- In each ADC, parameters of its first channel (inputs AIN1 ±) are set and internal digital filters are reset.
- The converters are started simultaneously. In this case, filters are filled with a frequency of 150 Hz during 22 periods of the internal conveyor.
- After the filters filling, the first sample is produced at the output of the converters, which is read by the DSP.
- In each ADC, parameters of its second channel (inputs AIN2 ±) are set, the filters are reset, and the process is repeated for the next four channels.

The *average frequency* of data acquisition in this mode *is* about 3.4 Hz for each channel, with samples for the first and second quadruples of channels shifted by half the period of this frequency.

! 8-channel high accuracy mode, unlike other modes, is not strictly synchronous, so only the average frequency can be considered.

6.3.9 Modes of measuring circuits switching in LTR212M-1

LTR212M-1 has software-controlled analog keys (denoted as K3...K7 on the block diagram fig. 6-4, page 118), which are designed for implementation of quarter-bridge connection diagrams with internal additional 220 Ohm/350 Ohm resistors or user resistors installed on LTR212H mezzanine board (paragraph 6.5). Presence of input switching of measuring circuits is the main difference between LTR212M-1 and other modifications of this module. These switches (analog keys) can only be set to the desired state if there is no data acquisition (before a measurement session or between measurement sessions).

Independent software-controlled analog keys K7-K9, connecting resistors R22-R24, R66 with a resistance of 100 kOhm ± 1% to the quarter-bridge of each of the 4 channels are used to implement the test mode of creation of the quarter-bridge unbalance.

6.3.9.1 A quarter-bridge connection of the measuring circuit in LTR212M-1 (in detail).

By the example of the first channel, with the same symbols of the block diagram fig. 6-4, page 118, let us consider in detail the components of a quarter-bridge connection diagram (the full connection example is given in fig. 6-11, 129). The measuring circuit (fig. 6-5) consists of an external quarter-bridge strain gauge Rx, internal wire resistances Rc, and internal elements of LTR212M-1 module: completion resistor R16/R14/"USER" (depending on the switching mechanism), a resistor of the test unbalance mode of the bridge R22 (connected with K7, if the test mode is enabled), an internal completion half bridge R1, R5.

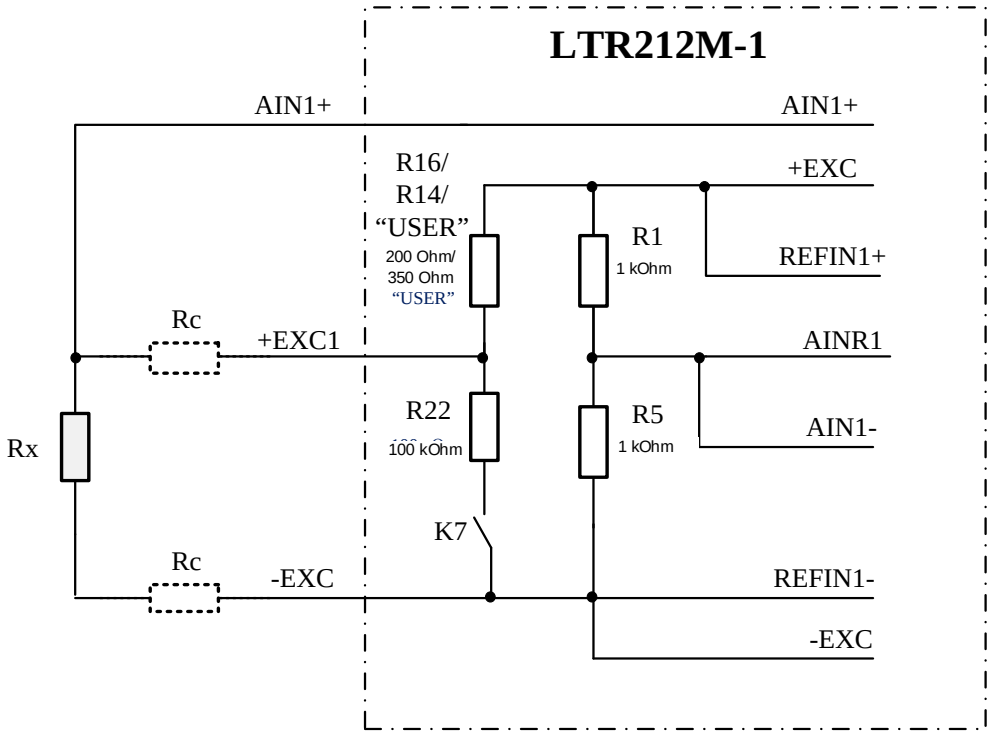


Fig. 6-5. LTR212M-1. Components of the quarter-bridge measuring circuit

Measuring circuit (fig. 6-5), like any other circuits for connecting to LTR212(M), is a circuit for extension to the full bridge. Here, wire resistance Rc enters the "upper" and "lower" arms of the full bridge, and with identical wire lengths (and with the same wires) in the circuits + EXC1 and -EXC, there, theoretically, will occur compensation, i.e. the independence of the the full bridge unbalance from the length of the cable. The wire resistance in the AIN1 + circuit is not taken into account, since the AIN inputs of the module are high-impedance, so we assume that the resistance of the AIN circuit wire makes no effect on the measured bridge unbalance.

The practical advantage of this connection diagram is that it is a 3-wire diagram. This is important for multi-channel vibration testing systems, where the number of wires going to the test object is critical.

The test mode with creation of controlled quarter-bridge unbalance allows for checking the integrity of the connections to the sensor in a state when the sensors are disabled.

The estimated value of the introduced unbalance Δ of the test mode bridge at Rc = 0[1] is

$$\Delta=\left(\frac{100000}{R_X+200000}-0{,}5\right)U_{REF}$$

provided that the state of the bridge was balanced before introducing the test unbalance. Here, the imbalance is brought to Volts relatively to the value of the rated 5.0 V or 2.5 V voltage supplied to the bridge U_{REF} (the physical meaning of Δ is explained in paragraph 6.3.1). Note that, proceeding from the connection diagram and the above formula, the *test unbalance will have a negative value*.

6.3.10 2.5 V and 5 V RVS.

In LTR212(M), there is a reference voltage supply (RVS) for powering external bridge circuits with a software-switched voltage value (U_{REF} 2.5 or 5 V).

[1] The formula for Rc ≠ 0 is much more cumbersome, and at a relatively low wire resistance provides an insignificant adjustment for the value calculated with the use of the given formula.

For almost all strain-gauge measurements, the optimal bridge supply voltage is 5 V. However, there are relatively rare applications when low-power film strain gages are used, which can not be powered by 5 V voltage because their permissible power dissipation is exceeded.

6.4 Connection of signals

Read the general rules for signal connection, paragraph 3.6.6, page 58.

The LTR212 (M) module has a block part of DRB-37M connector for connecting bridge circuits. External connections to LTR212(M) must be implemented by connecting signal circuits to the cable part of the connector (DB-37F type). Signal assignments are given in Table 6-3, and the view of the panel-mounted connector is presented in Fig. Fig. 6-6 .

In LTR212, LTR212M-2, LTR212M-3, the + EXC -EXC circuit is duplicated at the connector pins so that when connected, it is possible to redistribute the power currents of different bridges and minimize the effect of the contact resistance of the connectors on the stability of the bridge supply voltage. If more than one bridge circuit is connected, use different connectors of + EXC, -EXC circuit for voltage supply to different bridges (or different pairs of bridges for 8-channel mode). The difference of LTR212M-1 is the additional division of bridge voltage supply into sub-circuits + EXC, + EXC1, + EXC2, + EXC3, + EXC4, which must be connected according to the connection diagrams below.

When making a cable for connecting bridge circuits, consider the following factors to - improve the signal-to-noise ratio and the measurement accuracy:

- Screening (paragraph 3.6.2.2, page 52).
- Twisting together pairs of wires AIN_{i-}, AIN_{i+}, and $REFIN_{i-}$, $REFIN_{i+}$, or any other actions ensuring pairwise symmetrical position of these wires relatively to the external environment.
- For full- and half-bridge sensors, select the connection point $REFIN_{i-}$, $REFIN_{i+}$ locating as close as possible to the power point of the bridge. For full-bridge sensors this means that the connection diagram is "6-wire" instead of "4-wire", for half-bridge - "5-wire" instead of "3-wire", even if you can implement this principle not over the entire length of the cable, but on the longest part of it.
- Avoiding the use of internal half-bridge elements in LTR212(M) to complete the external bridge circuits, and transition to a purely external classic 4-resistor bridge circuit, in which all the resistors are concentrated in one place. - This principle will help to improve the signal-to-noise ratio.

6.4.1 Application of signals

Table 6-3. Application of LTR212(M) user connector signals.

Signal name	Common point	Direction	Description
AINR1, AINR2, AINR3, AINR4	AGND[1]	–	The midpoints of 4- internal half-bridge circuits– can be used for external connections if the half-bridge circuits are powered (see EXCR + signal)
REFIN1-, REFIN1+; REFIN2-, REFIN2+; REFIN3-, REFIN3+; REFIN4-, REFIN4+	AGND	Input	The pairs of inputs (inverting (-) and non-inverting (+)) form four differential inputs of the reference voltage of DA1, DA2, DA3, DA4 converters
-EXC, +EXC		Output	Negative and positive poles [2]of the reference voltage source for supplying voltage to the external bridge circuits
+EXC1, +EXC2, +EXC3, +EXC4 (In LTR212M-1 only)		Output	Positive pole circuits of the reference voltage source for supplying voltage to the external full- and half-bridge circuits. The circuit supplying a positive voltage potential to the quarter-bridges of channels 1, 2, 3, 4, respectively.
AIN1-, AIN1+	AGND	Input	Differential input of the 1-st channel (1-st channel of DA1 converter)
AIN2-, AIN2+	AGND	Input	Differential input of the 2-nd channel 1-st channel of DA2 converter)
AIN3-, AIN3+	AGND	Input	Differential input of the 3-rd channel (1-st channel of DA3 converter)
AIN4-, AIN4+	AGND	Input	Differential input of the 4-th channel (1-st channel of DA4 converter)
AIN5-, AIN5+	AGND	Input	Differential input of the 5-th channel (2-nd channel of DA1 converter)
AIN6-, AIN6+	AGND	Input	Differential input of the 6-th channel (2-nd channel of DA2 converter)
AIN7-, AIN7+	AGND	Input	Differential input of the 7-th channel (2-nd channel of DA3 converter)
AIN8-, AIN8+	AGND	Input	Differential input of the 8-th channel (2-nd channel of DA4 converter)
EXCR+ (In LTR212 only)	AGND	Input	Power supply input of internal half-bridge circuits. If the internal half-bridge circuits are to be used, then EXCR + and + EXC must be connected on the mating part of the user connector. In this case, the internal half-bridge circuits will be powered from the internal reference voltage supply.

[1] a specific feature of LTR212: The internal AGND circuit which is the common point for the converters, is not output to the contacts of the user connector, since it is not used when connecting external bridge circuits

[2] here and elsewhere in this Table: for the alternating RVS mode, the positive and negative poles of these circuits periodically alternate.

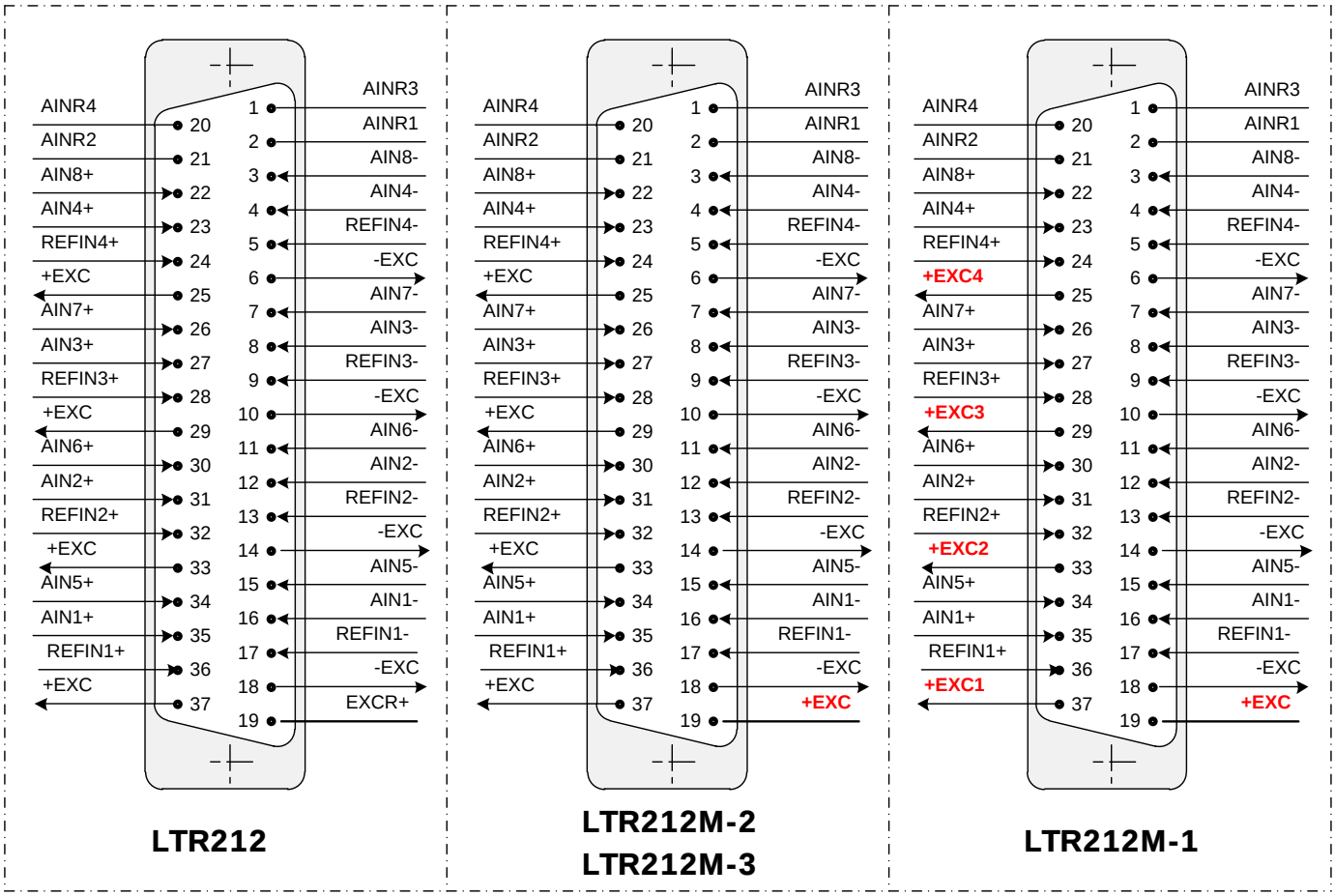


Fig. 6-6. Signals at LTR212, LTR212M modules connector

The differences of signals at LTR212M module connector from LTR212 in the figure above are highlighted in red colour.

6.4.2 Characteristics of signal line inputs and outputs

When connecting LTR212(M) module to your system, strictly observe the parameters specified in Table s of this section.

The manufacturer shall not be warranty liable for LTR212(M) failure caused by violation of maximum permissible operation conditions .

Note that when connecting LTR212(M) module, only the internal voltage *source (+ EXC,- EXC, + EXC1 ... + EXC4 circuits) of this module* should be used to power the external bridge circuits. It is prohibited[1] to use an external power supply of bridge circuits.

The characteristics of galvanic isolation in LTR are given in Appendix A.18, page 362.

6.4.3 Performance limits of LTR212(M) signal lines

LTR212(M) module installed in LTR crate has the following characteristics of input and output signal lines.

[1] there is no use in this mode, and the description of the limit characteristics for this case is rather cumbersome

Table 6-4. Characteristics of signal lines inputs, operating mode

Signal	Type[1]	Input impedance[2]	Maximum permissible conditions
AINR1…AINR4	AI	500 Ohm	voltage range U_{+EXC}…U_{-EXC}
+EXCR	AI	500 Ohm	voltage range U_{+EXC}…U_{-EXC}
AIN±…AIN±	AI	Minimum 10 MOhm	voltage range U_{+EXC}…U_{-EXC}
REFIN1±…REFIN4±	AI	Minimum 10 MOhm	voltage range U_{+EXC}…U_{-EXC}
+EXC…-EXC, +EXC1, +EXC2, +EXC3, +EXC4	–	Minimum 10 MOhm	Continuous current not more than 400 mA. Short circuit time not more than 1 minute. The typical value of short circuit current is 550 mA

6.4.4 Connection diagrams

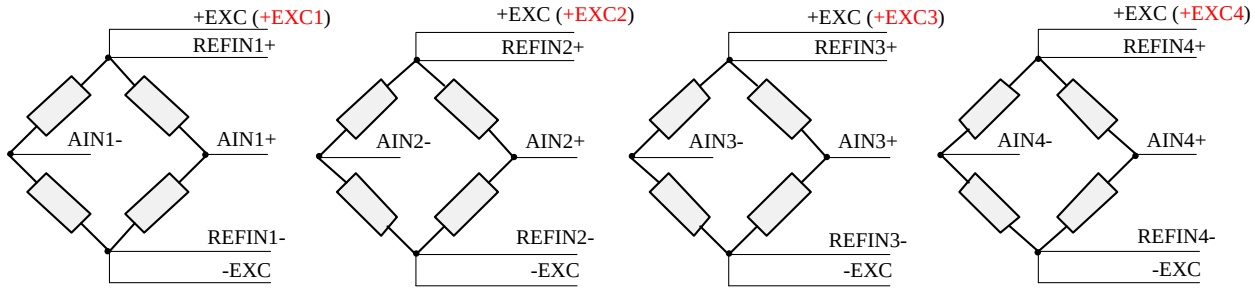


Fig. 6-7. LTR212(M). Full bridges (4-channel mode)

In 4-channel mode, up to 4 full bridges can be connected to all modifications of LTR212 modules, as shown in fig. 6-7.

If LTR212M-1 module is used, the signals + EXC1, + EXC2, + EXC3, + EXC4, which are used only in this module modification (marked in red), can be used. However, if you use a ready cable made for the old module modification, where all or some of + EXC, + EXC1, + EXC2, + EXC3, + EXC4 signals are closed between each other on the cable part of the connector, there is *no need to re-make the cable*, as these connections will not affect the correct operation of the module.

It is most preferable to use full-bridge connections in 4-channel mode with the *6-wire connection diagram*, when + EXC, + REFIN, and -EXC, -REFIN circuits are connected to the bridge by separate wires. In this case, the maximum independence of the result of measuring the bridge unbalance from the length of the cable and the temperature dependence of the resistance of the cable wires is achieved.

However, in case of connection with a relatively short cable, the *4-wire diagram* can be used, in which the corresponding + EXC, + REFIN circuits are combined on the cable part of the connector, and the corresponding -EXC, -REFIN circuits are also combined there.

[1] type **AI** – analog input, power output

[2] relatively to any of the bridge power lines: -EXC or +EXC

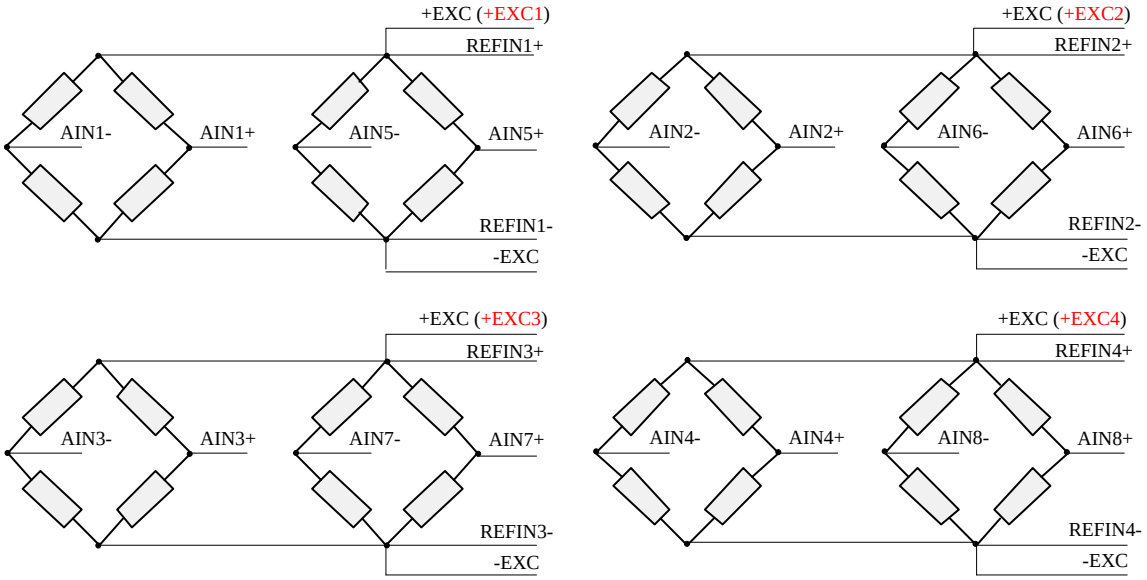


Fig. 6-8. LTR212(M). Full bridges (8-channel mode)

In 8-channel mode, all modifications of LTR212 modules can work with the connection diagram for up to 8 full bridges, as shown in fig. 6-8.

If LTR212M-1 module is used, the signals + EXC1, + EXC2, + EXC3, + EXC4, which are used only in this module modification (marked in red), can be used. However, if you use a ready cable made for the old module modification, where all or some of + EXC, + EXC1, + EXC2, + EXC3, + EXC4 signals are closed between each other on the cable part of the connector, there is *no need to re-make the cable*, as these connections will not affect the correct operation of the module.

It is most preferable to use full-bridge connections in 8-channel mode using a cable, the maximum possible part of which is *6-wire*, i.e. when + EXC, + REFIN, and -EXC, -REFIN circuits are connected with separate wires and their connection is in the immediate vicinity of the bridges. In this case, the maximum independence of the result of measuring the bridge unbalance from the length of the cable and the temperature dependence of the resistance of the cable wires is achieved. In this case, the maximum independence of the result of measuring the bridge unbalance from the length of the cable and the temperature dependence of the resistance of the cable wires is achieved. To implement this connection principle, it is necessary that the pairs of bridges shown in fig. 6-8be physically located in close proximity to each other.

However, in case of connection with a relatively short cable, a simplified diagram can be used, in which the corresponding + EXC, + REFIN circuits are combined on the cable part of the connector, and the corresponding -EXC, -REFIN circuits are also combined there.

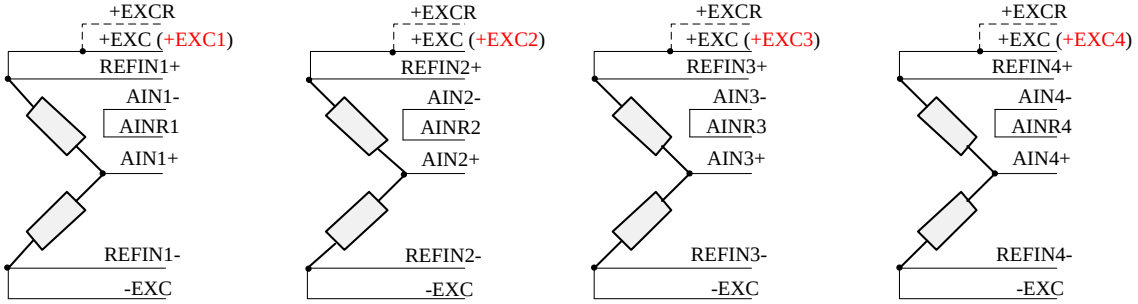


Fig. 6-9. LTR212(M). Half bridges (4-channel mode)

In 4-channel mode, up to 4 half-bridges can be connected to all modifications of LTR212 modules, as shown in fig. 6-9.

If LTR212M-1 module is used, the signals + EXC1, + EXC2, + EXC3, + EXC4, which are used only in this module modification (marked in red), can be used. However, if you use a ready cable made for the old module modification, where all or some of + EXC, + EXC1, + EXC2, + EXC3, + EXC4 signals are closed between each other on the cable part of the connector, there is *no need to re-make the cable*, as these connections will not affect the correct operation of the module.

It is most preferable to use full-bridge connections in 4-channel mode with the *5-wire connection diagram*, when + EXC, + REFIN, and -EXC, -REFIN circuits are connected to the bridge by separate wires. In this case, the maximum independence of the result of measuring the bridge unbalance from the length of the cable and the temperature dependence of the resistance of the cable wires is achieved.

However, in case of connection with a relatively short cable, the 3-*wire diagram* can be used, in which the corresponding + EXC, + REFIN circuits are combined on the cable part of the connector, and the corresponding -EXC, -REFIN circuits are also combined there.

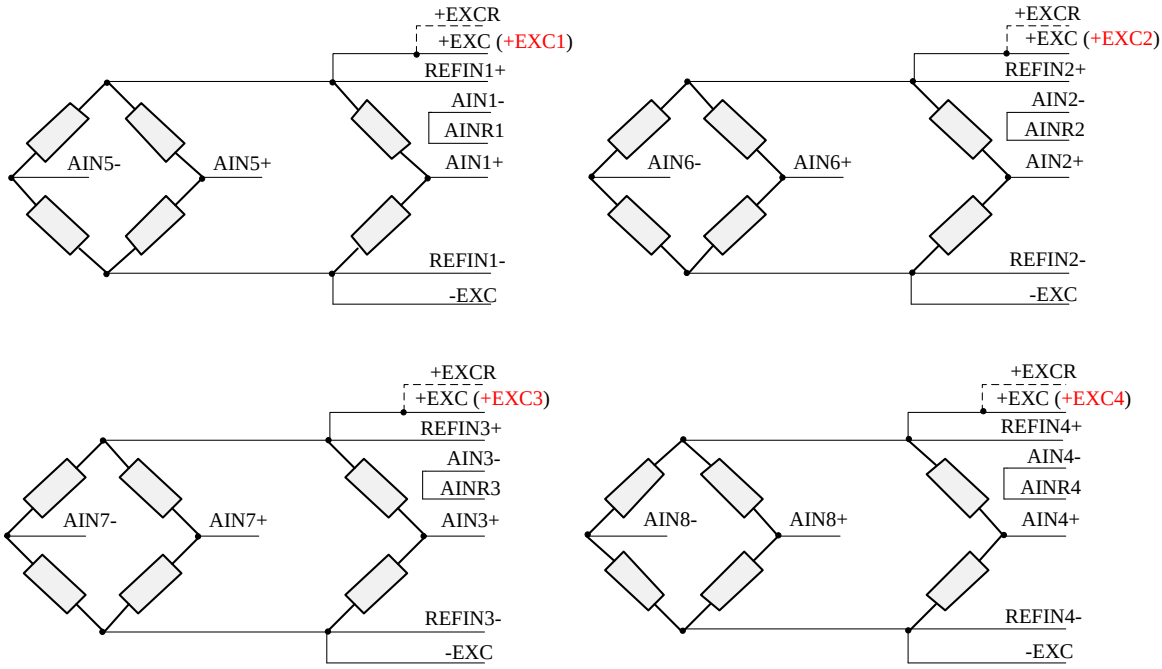


Fig. 6-10. LTR212(M). Half bridges and full bridges (8-channel mode)

In 8-channel mode, all modifications of LTR212 modules can work with the mixed connection diagram for up to 4 half bridges and up to 4 full bridges, as shown in fig. 6-10.

If LTR212M-1 module is used, the signals + EXC1, + EXC2, + EXC3, + EXC4, which are used only in this module modification (marked in red), can be used. However, if you use a ready cable made for the old module modification, where all or some of + EXC, + EXC1, + EXC2, + EXC3, + EXC4 signals are closed between each other on the cable part of the connector, there is *no need to re-make the cable*, as these connections will not affect the correct operation of the module.

It is most preferable to use such bridge connection that + EXC, + REFIN, and also -EXC, -REFIN circuits be connected to the bridge by separate wires. In this case, the maximum

independence of the result of measuring the bridge unbalance from the length of the cable and the temperature dependence of the resistance of the cable wires is achieved.

However, in case of connection with a relatively short cable, a diagram with the less number of wires can be used, in which the corresponding + EXC, + REFIN circuits are combined on the cable part of the connector, and the corresponding -EXC, -REFIN circuits are also combined there.

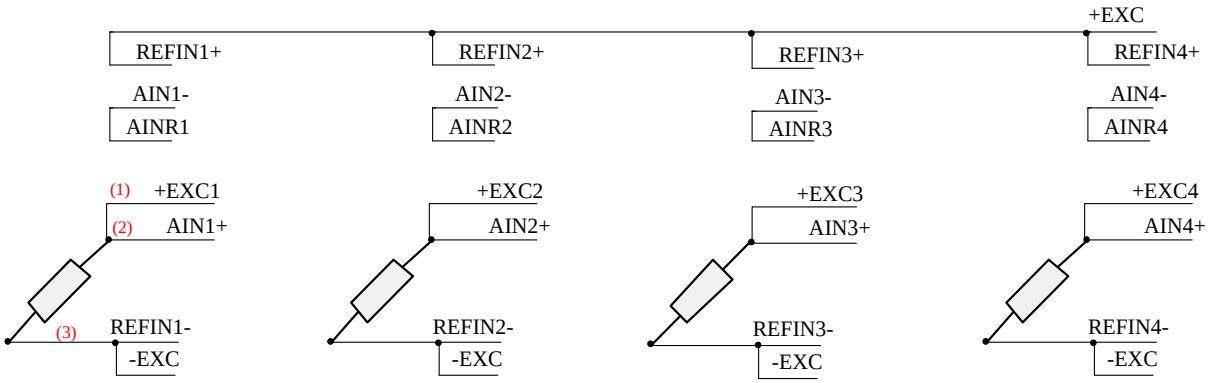


Fig. 6-11. LTR212M-1. Quarter bridges (4-channel mode)

In 4-channel mode, LTR212M-1 module can work with 3-wire connection diagram for up to 4 quarter bridges, as shown in fig. 6-11. For example, three cable wires going to one of the bridges are marked (1), (2), (3). All other circuits connecting each channel must be realized by short jumpers on the cable part of LTR212M-1 connector.

In this 3-wire circuit, temperature compensation is largely achieved in case where wires (1) and (3) (by the example of the 1st channel) have the same temperature coefficient (when they are of the same type) when they are of the same length and when they are in the same temperature conditions. This must be taken into account when making the cable.

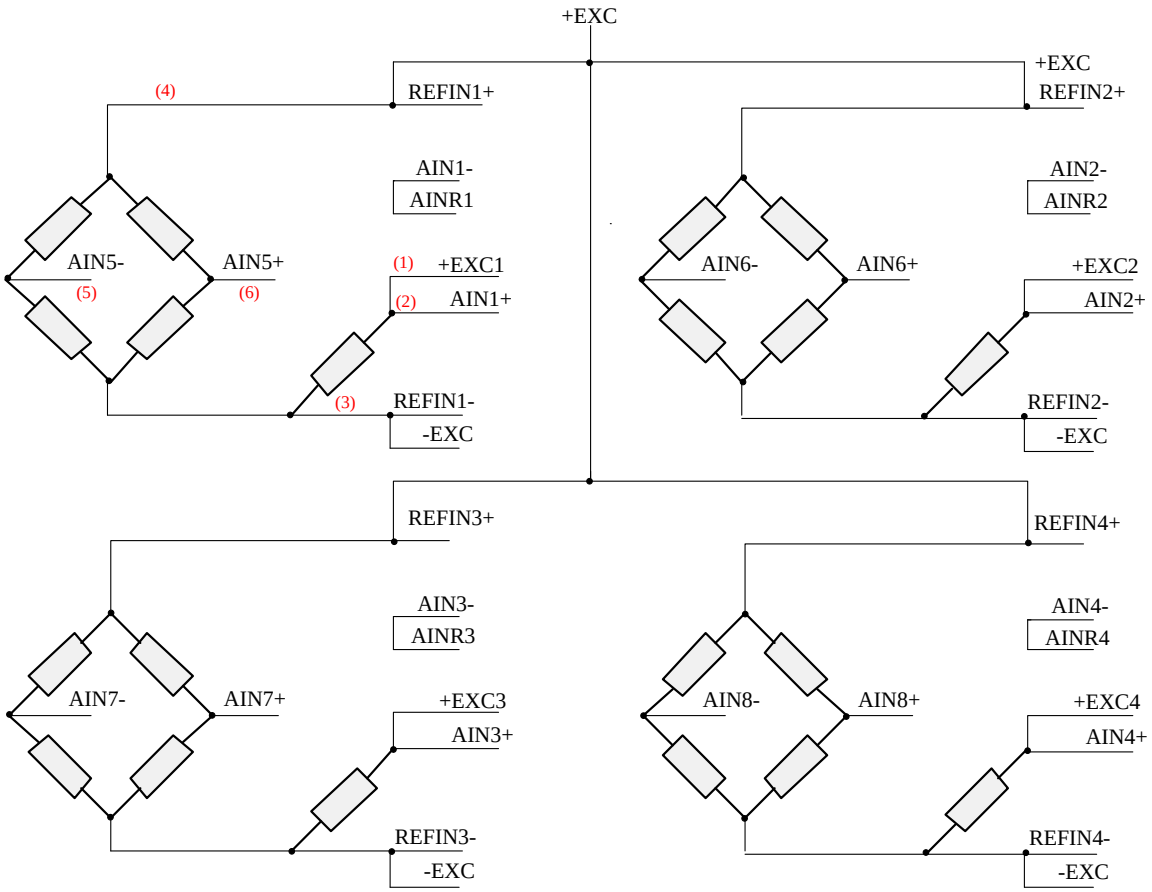


Fig. 6-12. LTR212M-1. Quarter bridges and full bridges (8-channel mode)

In 8-channel mode, LTR212M-1 module can work with the mixed connection diagram for up to 4 half bridges and up to 4 full bridges, as shown in fig. 6-12. For example, 6 cable wires going to one of the bridges (channels 1 and 5) are designated (1), (2), (3), (4), (5), (6). All other circuits connecting each channel must be realized by short jumpers on the cable part of LTR212M-1 connector.

Attention! The connection diagram fig. 6-12 provides for no compensation for the effect of wire length on measurement results. Therefore, this diagram is practically suiTable for very short cables only.

In addition, the installation can be complicated to some extent by a large number of + EXC circuit branches at the single contact on LTR212M-1 connector.

6.4.4.1 Screen connection.

In principle, there can be no screen. Nevertheless, it is recommended to use a screen for ensuring maximum measurement accuracy. The screen must be soldered to the metal housing of the mating part of the user connector. This circuit is connected to the LTR crate frame, so the screen will be the continuation of the system casing. Do not connect the screen on the bridge side.

6.5 Mezzanine card LTR212H for LTR212M-1.

The mezzanine board is provided to the user for mounting quarter-bridge balanced resistors. The rating and accuracy of these resistors must be selected based on the requirements to the initial bridge unbalance (paragraph 6.3.1). The recommended range is from 180 to 1000 Ohm.

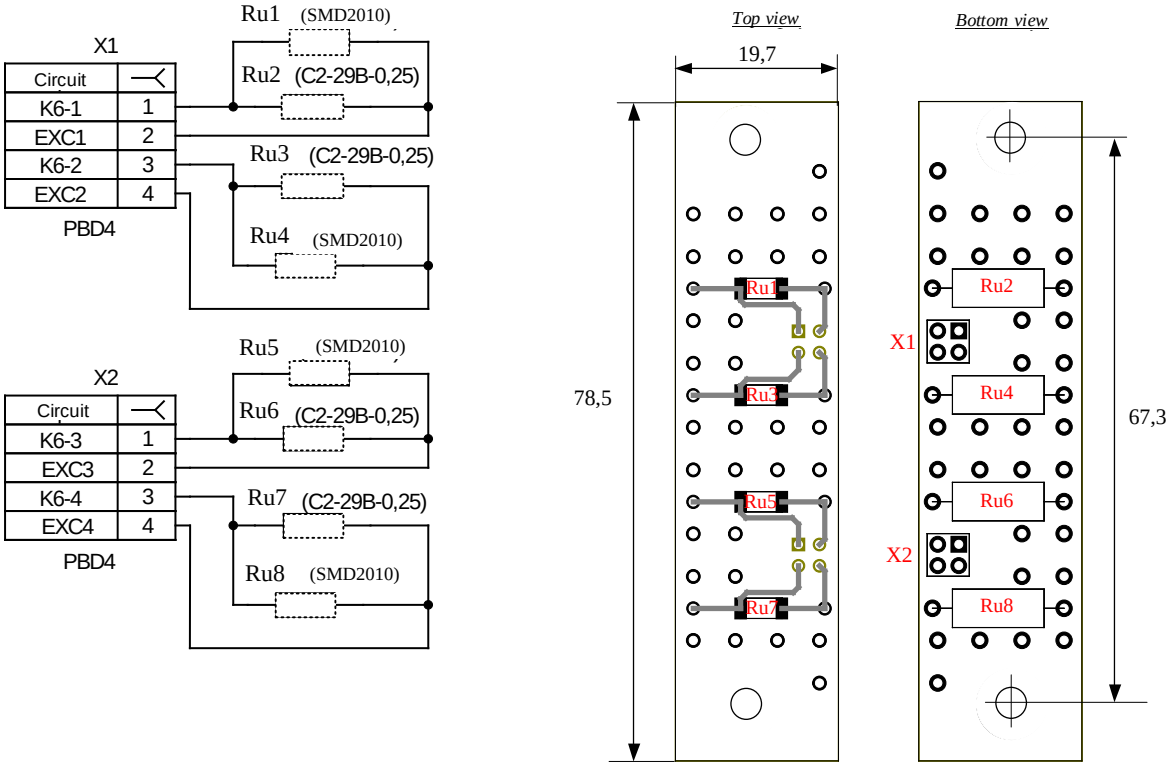


Fig. 6-13. The electrical diagram, top and bottom views of LTR212H.

Resistors Ru1-Ru8 shown in the figure are not physically soldered at the factory, because these are user resistors ("USER")[1]. On the 2-sided printed circuit board LTR212H, for flexibility, there are slots of SMD2010 standard size (surface-mounted 4.9 x 2.4 mm resistor) and C2-29B-0.25 standard size (output resistor with housing length of 11 mm, housing diameter of 4.5 mm, output diameter of 0.8 mm, distance between the openings for outputs of 16 mm, diameter of an opening for output of 1 mm).

LTR212H is installed according to fig. 6-14. When physically mounting elements on the LTR212H, the maximum height is 8 mm from the top and 9 mm from the bottom of the board. In fact, the height of 5 mm from the top and 7 mm from the bottom of the board must not be exceeded.

LTR212H board also has a large number of unconnected metallized openings with a diameter of 1 mm located over the entire free space of the board. These openings are intended for user installation in case of using resistors of a different design.

[1] In principle, L-Card can supply LTR212H with the required resistors, install and test the LTR212M-1 product in conjunction with LTR212H under an individual order.

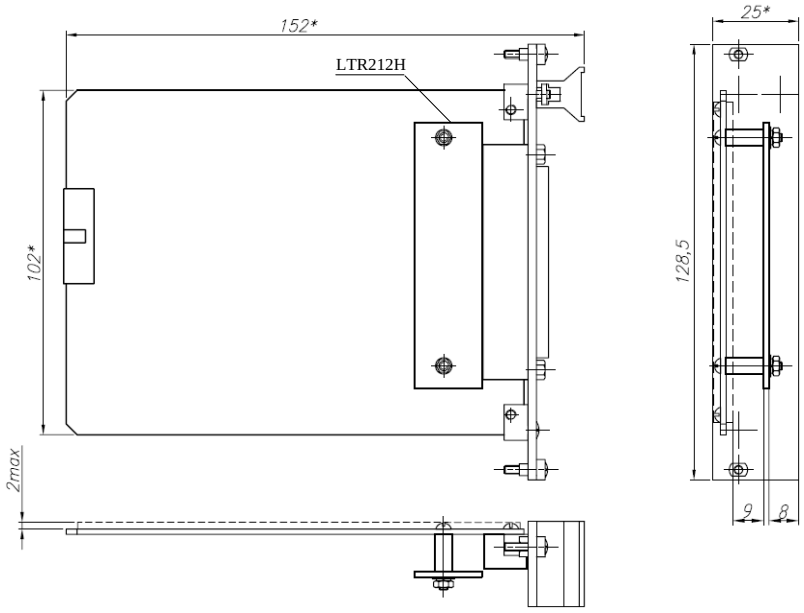


Fig. 6-14. LTR212M-1 with LTR212H mezzanine (design).

Restrictions for use of LTR212H mezzanine card:

The manufacturer's warranty is not provided for LTR212H.

LTR212H is delivered to the user "as is" subject to conducting qualified electrical installation operations by the user.

During the verification of LTR212M-1, the mezzanine board must be physically disconnected. When delivering LTR212M-1 to L-Card for re-verification, the mezzanine board must be removed and left by the user at his premises (do not deliver it to L-Card).

Under a separate order, LTR212M-1 can be equipped with more than one LTR212H mezzanine card, if the user needs replacement configurations for 4-bridge sensors other than 200 and 350 Ohms.

6.6 LTR212(M) module control

Here, the basic LTR -interface commands of LTR212(M) module implemented by hardware are described. Protocol of LTR- modules is described in p. 4.6.3,page 83. Hardware-dependent part of this protocol in the context of LTR212(M) is detailed herein. The complete description of LTR212(M) commands is given in the document *"LTR Crate System. Programmer's Manual"*[1] .

The STOP, RESET and PROGR commands are used in LTR212(M) for initialization of the module and ADSP loading. Then, by using the PROGR commands, the operating cycle of the module control is maintained. Unlike modules with AVR, restart of LTR212(M) (with ADSP reset) is only possible only through the procedure of ADSP reloading initiated by the STOP command.

Unlike modules with AVR, in LTR212(M), the PROGR command is used for loading (each time when the module is initialized), with no response from the DSP during the loading process. The correctness of DSP loading is confirmed by software after the loading is complete.

PROGR command (no response words).			
1	**01xx xxxx**	**pppp pppp**	**pppp pppp**
<24>	<23..16>	<15..8>	<7..0>

x – the bit values are not used;

p – is the loading information of BDMA ADSP loading protocol. Byte <15..8> is loaded first and byte <7..0> is loaded second.

The data packets received from LTR212(M) have the following format:

DATA packet.			
0	**NNNN hCCC**	**dddd dddd**	**dddd dddd**
<24>	<23..16>	<15..8>	<7..0>

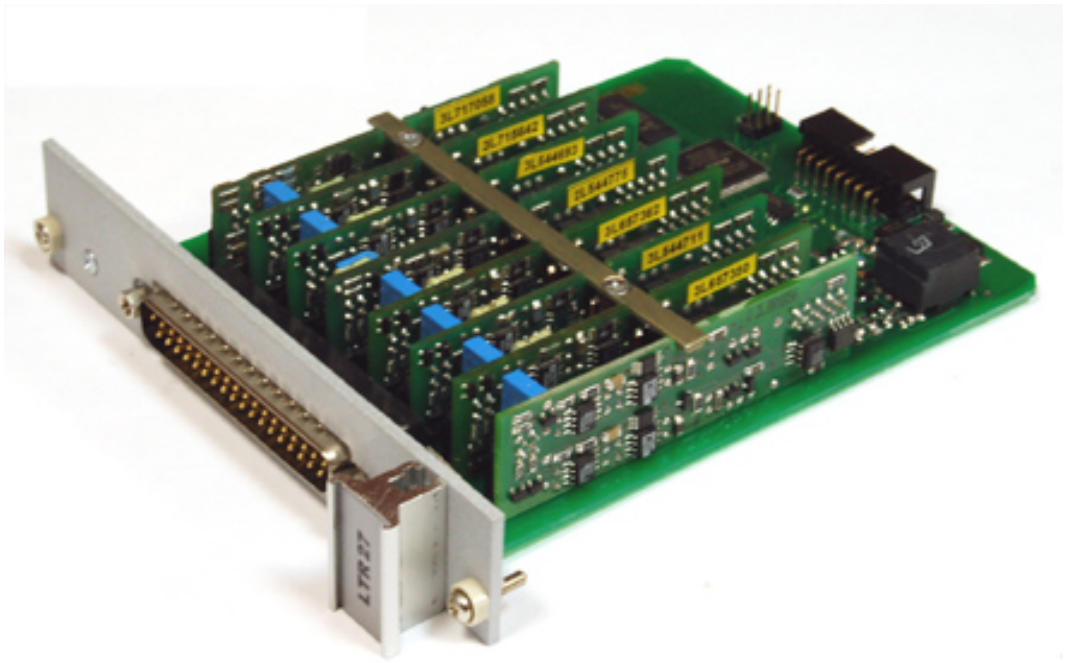
d *are* data bits; **C** *are* bits defining the physical channel number[1];

h *is* the bit defining the data format: if **0,** *than* this is the 16-bit format, if **1,** *then this is* the 24-bit format-.

! It is essential that **CCC** determines the physical channel number to which the data field **dd** ... **d** of this packet corresponds. The physical numbers of channels at the module connector are described in Table 6-3

[1] agreement about numbering of physical channels, see paragraph 3.1.2 on page 12

Chapter 7. LTR27 measuring module



7.1 General description of LTR27

Fig. 7-1. LTR27 view with H-27x sub-modules

7.1.1 Device assignment

LTR27 module carries measuring sub-modules H-27x, which are designed to measure slowly varying values of voltage, current and resistance.

7.1.2 General information about LTR27

- The configurable[1] architecture of LTR27 carrier module allows for the installation of 1 to 8 H-27x submodules (1- or 2-channel submodule depending on its type). The composition of submodules in the carrier module can be determined by the user.
- The installed configuration of submodules is software-accessible.
- Individual galvanic isolation - *The inputs of each channel are galvanically isolated* from the ground (frame) of the LTR crate and from other channels and LTR modules.
- The data acquisition frequency is from 5 Hz to 100 Hz.

Below are short characteristics of H-27x submodules.

[1] in accordance with the order

Table . 7-1
H-27x. H-27x sub-module types and measuring ranges

Submodule	Number of channels	Task	Range
H-27I5	2	Current meter	0…5 mA
H-27I10	2	Current meter	-10…10 mA
H-27I20	2	Current meter	0…+20 mA
H-27T	2	Thermocouple voltage meter	-25…+75 mV
H-27R100	1	Resistance meter	0…100 Ohm
H-27R250	1	Resistance meter	0…250 Ohm
H-27U01	2	Voltage meter	-1…+1 V
H-27U10	2	Voltage meter	-10…+10 V
H-27U20	2	Voltage meter	0…+20 V

All performance parameters of LTR27 module are summarized in Appendix 0, page 331 and A.4, page 332.

7.1.3 LTR27 module configuration

The basic LTR27 configuration is described in paragraph 2.4, page 29.

7.2 Installation and set-up

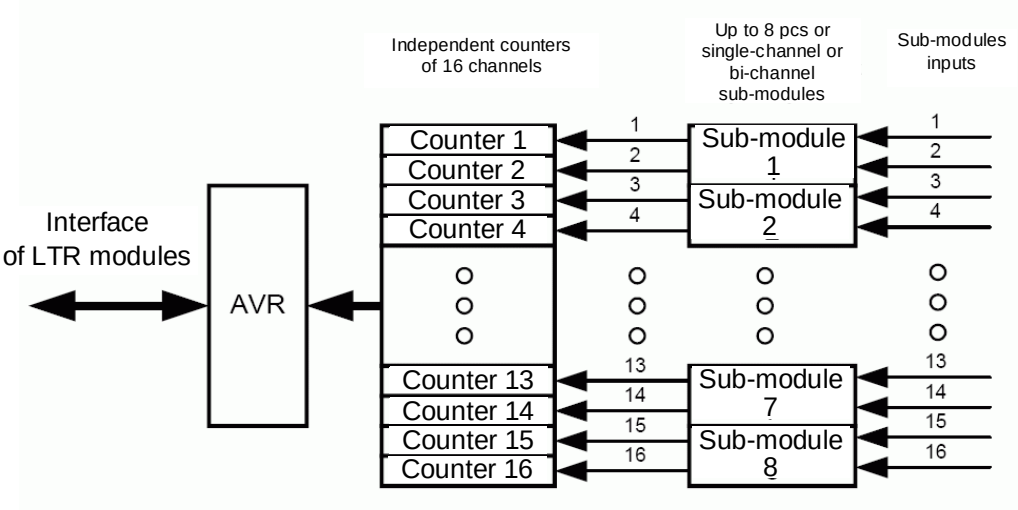
During LTR27 installation in crate, observe the module installation rules common for LTR system, see paragraph 3.6.2, page 51.

7.3 Overview of LTR27 hardware components and operation principles

7.3.1 Block diagram

The block diagram of LTR27 module is shown in Fig. Fig. 7-2.

Fig. 7-2. LTR27 module block diagram



On the block diagram, *pulse counters* count the number of pulses arriving for 1 ms. Pulses come from voltage-to-frequency converters (VFC) of H-27x submodules. The counters polls the AVR, counting the number of pulses for specified time periods (possibly more than 1 ms), and sends to the interface the calculated measurement sample codes. Therefore, the maximum sampling frequency for measurements of each channel (at the worst measurement accuracy) is 1 kHz. To

obtain better measurement accuracy, lower data acquisition frequencies are used; in this case, the AVR performs additional data averaging.

Let us consider the functional arrangement of H-27x submodules. The block diagram of one channel of H-27U, H-27T or H-27I submodule is presented in Fig. Fig. 7-3

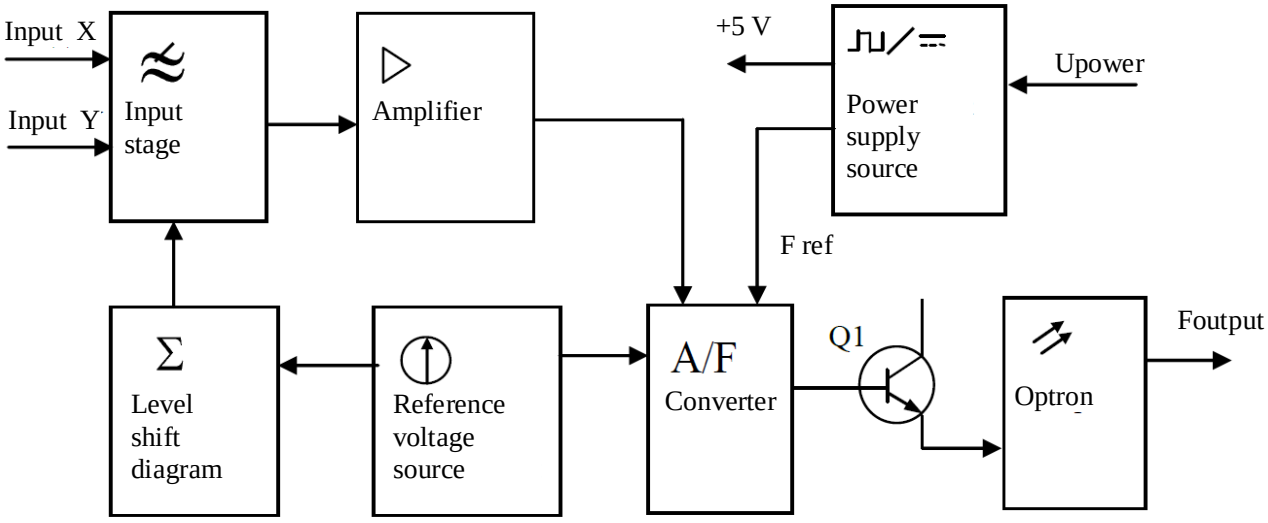


Fig. 7-3. Block diagram of the channel of H-27 submodules, type U, I and T

Two-channel submodules of all modifications have two identical measuring channels. The input stage of the submodule performs the filtering and brings the value of the input signal to a specified level, and also limits it to a safe value for subsequent stages in case of an input overload. The input stage circuit defines the type of the submodule, its dynamic range and the input resistance.

Relatively to a galvanically isolated channel of the submodule, the input of the submodule is - single-phased, since the Y input is connected to a level shift circuit. However, with respect to external signals, both inputs are symmetrical, which is ensured by galvanic isolation of the measuring path of the converter. The signal level offset is set in such a way as to provide the necessary position of the zero point during the subsequent voltage-to-frequency conversion. The voltage generated at the input stage is applied to an amplifier with the gain depending on the - submodule type. The amplifier and the level offset circuit are implemented on the basis of a precision two-channel operational amplifier, which provides high stability of converter characteristics over time and at a temperature change. From the amplifier output, the signal goes to the input of the integrated voltage-to-frequency converter of AD7740 type, with the ratio of the output frequency to the reference frequency varying proportionally to the change in the input signal value. The non-linearity of this converter does not exceed 0.012%, and the effective bit depth is determined by the measurement period. For example, the time required for obtaining a 15-bit code is 160 ms. The reference frequency for synchronizing the voltage-to-frequency converter is formed in the power supply circuit from AC voltage U_{sup} at a frequency of 250 kHz. Such a solution allows ensuring transformer galvanic isolation and reducing the influence of pulse noise on the power supply side due to its synchronization with the conversion frequency. Power is supplied to all converter unit from one voltage rating <+5 V> generated by the power supply. The reference voltage required for operation of AD7740 converter and the signal level offset are formed by the - integral reference voltage source REF192. The output signal of AD7740 converter passes through the buffer stage on transistor Q1 to the optocoupler, which provides galvanic isolation of the converter from the external circuit via the signal circuits.

All H-27x submodules have a PROM of AT93C46 type (not shown in the block diagram). Its electrical circuits are not connected directly to the measuring circuit and it is used to store the calibration coefficients of the converter, the serial number and the type designation of the submodule.

The block diagram of one-channel H-27R submodule is shown in Fig. Fig. 7-4.

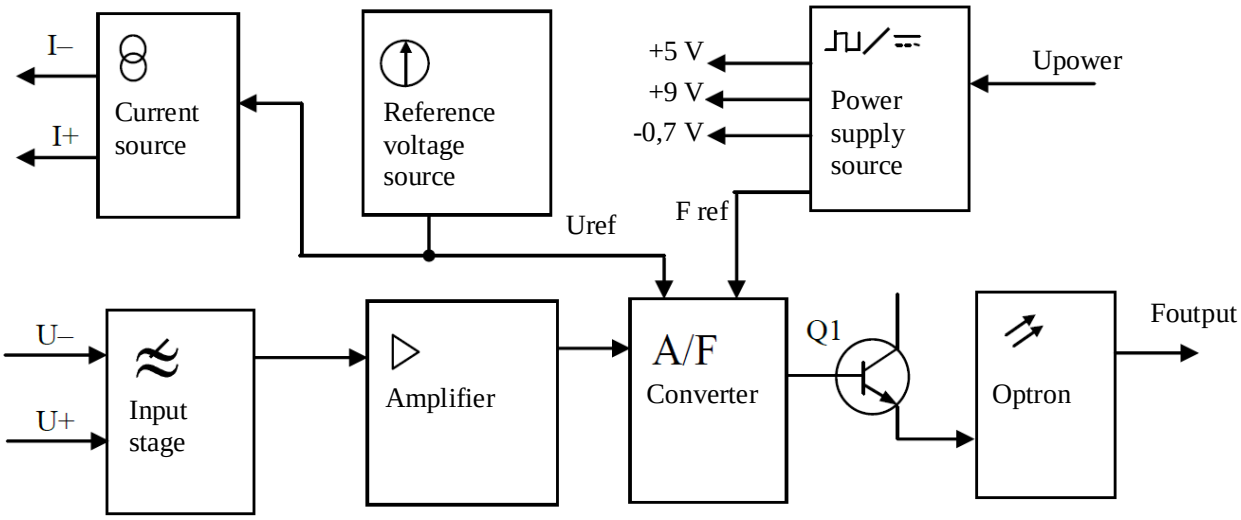


Fig. 7-4. Block diagram of H-27R submodule

Submodule H-27R differs from the above types with its input stage which is differential relatively to the converter circuit and with its current source and additional ratings of the power supply voltage (+ 9V and -0.7V) necessary for its operation. The current source generates sample current, the voltage drop from which on the measured resistor goes to the input stage with a diode voltage limiter and RC- low-frequency filter. Then the signal is amplified by a differential stage in the instrument amplifier. Then the scaled signal comes to the voltage-to-frequency converter AD7740, similarly to the converters described above.

The rated current of the precision current source is 1.6 mA, which corresponds to the voltage drop at the measured resistors to 0.4 V at a resistance of up to 250 Ohms.

Galvanic isolation of the converter channels simplifies for the system user the solution of problems related to the mutual influence of sensors circuits such as measuring signals from sensors having different housing potentials or selecting the optimal grounding scheme in the conditions of strong noise. In abnormal situations such as breaks, short circuits, penetration of impulse noise into circuits of sensors connected to one channel, parasitic effect on the circuits of the remaining channels will be minimal.

The use of the alternating current voltage to supply the converter provides galvanic isolation along the power circuit due to the use of a separating transformer, and galvanic isolation in signal circuits is provided by an optocoupler at the output of each channel.

7.3.2 LTR27 module control

7.3.2.1 Basic commands of LTR- interface in application to LTR27 module

Protocol of LTR modules is described in-p.4.6.3 , page83 . Hardware-dependent part of this protocol in the context of LTR27 is detailed herein. The complete description of LTR27 commands is given in the document "LTR Crate System. Programmer's Manual"[1].

7.4 Connection of signals

Read the general rules for signal connection, paragraph 3.6.6, page 58.

LTR27 module has panel-mount connector DRB-37M for connection of input signals. External connections to LTR27 must be implemented by connecting signal circuits to the cable part of the connector (DB-37F type).

The assignment of signals depends on the type of submodules H-27x installed in a certain LTR27 slot . The general view of the user connector of LTR27 is presented in Fig. Fig. 7-5.

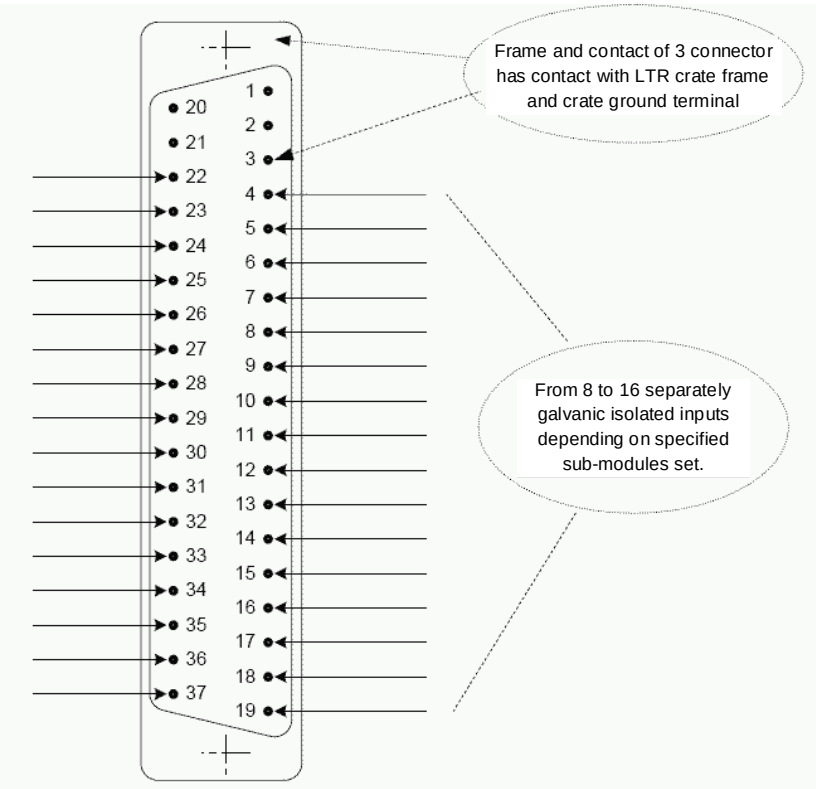


Fig. 7-5. LTR27 module connector (general view)

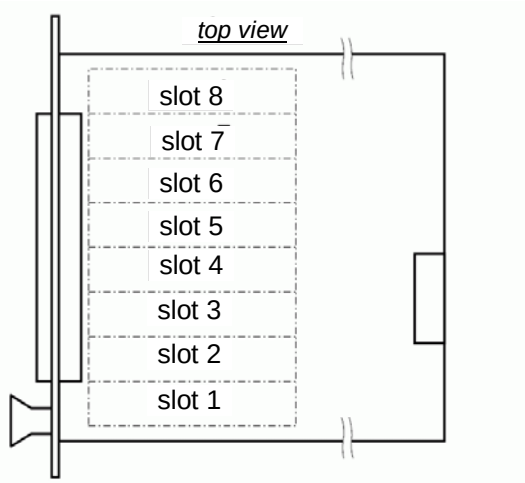
The slot layout is shown in Fig. Fig. 7-6.

The correspondence of the contact groups and slot numbers of the submodules is shown in Fig. Fig. 7-7 on the left. Any combination of types up to 8 installed submodules is possible in principle, therefore, the assignment of signals in a group depends on the type of submodule in the corresponding slot.

Let us consider a special case of LTR27 supplied with eight two-channel submodules H-27x (except for H-27R) and 16 individually galvanically isolated inputs ± CH1, ..., ± CH16 for measurements of a physical value (see Fig. Fig. 7-7in the center). For example, if eight H-27I submodules are used, we will get 16 independent current measurement inputs.

In the case of eight single-channel H-27R submodules (see Fig. Fig. 7-7 on the right), channel numbers with even numbers will not be used, and we will get 8 individual galvanically isolated channels ± U1 ± I1, ± U3 ± I3, ..., ± U15 ± I15 for resistance measurement in a 4-wire circuit (see Fig. 7-8).

Fig. 7-6. Layout of submodules slots in LTR27.



Naturally, a mixed installation of H-27x submodules of different types in LTR27 is possible.

In the case of using 2-channel submodules for current measurement H-27I, the + CH inputs of the corresponding channel will be the inputs of the *inflowing current*, and the -CH *inputs will be the inputs of the outflowing current*.

In all figures showing the connectors, the arrow pointing to the connector conventionally indicates the input, and the arrow pointing from the connector indicates the output.

If you use screened connection of the input signals, it is recommended to connect the cable screen to the metal casing of the DB-37F cable connector, or to pin 3 of this connector.

When using long cables, it is recommended that the multi-pole pairs of input signals (-CH + CH, -U + U, -I + I) be laid either as twisted pairs or as screened pairs of wires.

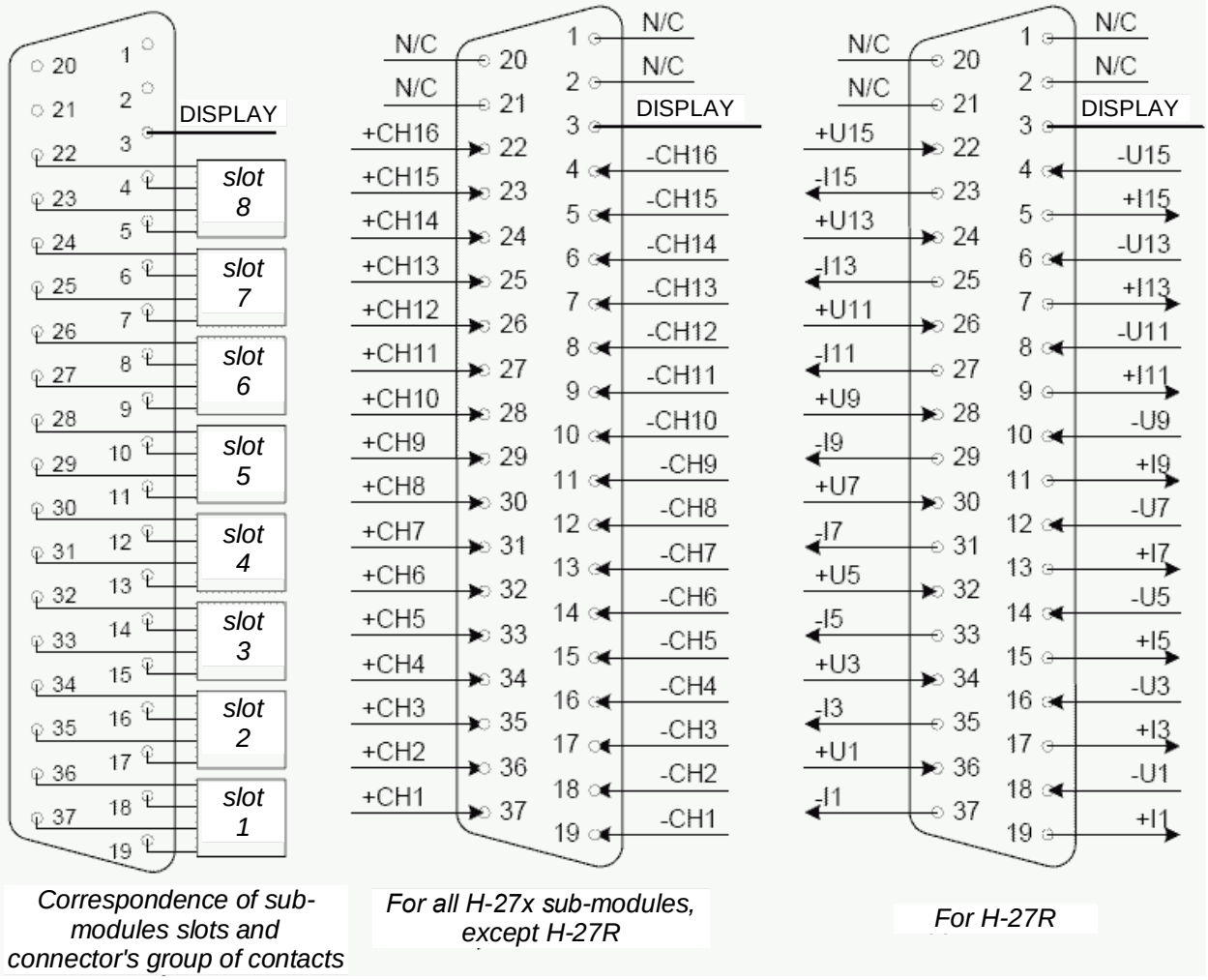


Fig. 7-7. Input signals at LTR27 module connector

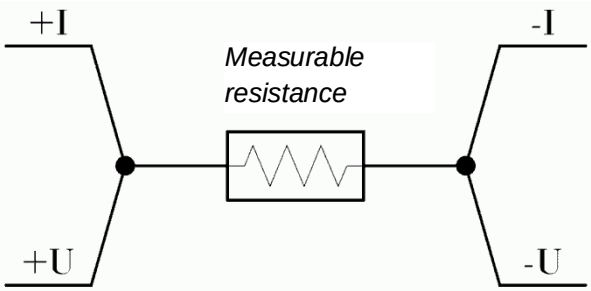


Fig. 7-8. 4-Wire connection for the case with H-27R

7.4.1 Cold junction compensation

OP-27TR cold junction compensator is used to *measure the cold junction temperature* when performing temperature measurements[1].

OP-27TR is a copper resistive temperature converter. Its characteristics are specified in the certificate supplied with it and conform to GOST 6651[16]. OP-27TR resistive temperature converter is designed to work in conjunction with *H-27R100*[2] *submodule* and is connected to its input as an external resistor.

7.4.2 Characteristics of signal line inputs and outputs

! When connecting LTR27 module to your system, strictly observe the parameters specified in Table s of this section.

The manufacturer shall not be warranty liable for LTR27 failure caused by violation of maximum permissible operation conditions . The characteristics of galvanic isolation in LTR are given in appendixA.18, page 362.

7.4.3 LTR27 operating mode

LTR27 module installed in a LTR crate has the following characteristics of input and output signal lines after the LTR crate is powered on:

Table 7-2. Characteristics of signal lines inputs, operating mode

Signal	Input impedance	Maximum permissible - conditions
Inputs +I, -I of sub-module H-27I5	392±4 Ohm	±7.5 mA
Inputs +I, -I of sub-module H-27I10	100±1 Ohm	±15 mA
Inputs +I, -I of sub-module H-27I20	100±1 Ohm	±30 mA
Inputs +U, -U of sub-module H-27T	more than 10 MOhm	±2 V
Inputs +U, -U of sub-module H-27U01	more than 10 MOhm	±15 V
Inputs +U, -U of sub-module H-27U10	1.02±0.02 MOhm	±15 V
Inputs +U, -U of sub-module H-27U20	1.02±0.02 MOhm	±35 V
Circuits +I, -I and +U, -U of sub-module H-27R100 or H-27R250, connected according to the diagram shown in Fig. 7-8	–	Measured resistance 0…∞ circuit

[1] for example, when measuring the signal from thermocouples with the use of H-27T submodule

[2] in this case, a single measuring channel of the submodule is used.

! The + I, -I and + U, -U circuits of H-27R submodule can only be connected in a circuit with a passive measuring resistor, as shown in Fig. 7-8. It is forbidden to include any external sources of current or voltage in the measuring circuit.

7.4.4 LTR27 in switched-off state

In switched-off state, LTR27 module has the following characteristics of the signal lines:

Table 7-3. Characteristics of signal lines inputs for LTR switched-off.

Signal	Input impedance	Maximum permissible - conditions
Inputs +I, -I of sub-module H-27I5	392±4 Ohm	±7.5 mA
Inputs +I,- I of sub-modules H-27I10	100±1 Ohm	±15 mA
Inputs +I, -I of sub-modules H-27I20	100±1 Ohm	±30 mA
Inputs +U, -U of sub-module H-27T	Not less than 100 kOhm in the operational range of 25…+75 V; not less than 2 kOhm in the range of ±2 V	±2 V
Inputs +U, -U of sub-module H-27U01	Not less than 12 kOhm	±15 V
Inputs +U, -U of sub-module H-27U10	Not less than 900 kOhm	±15 V
Inputs +U, -U of sub-module H-27U20	Not less than 900 kOhm	±35 V
Circuits +I, -I and +U, -U of sub-module- H27R100 or -H27R250, connected according to the diagram shown in Fig. 7-8	–	Measured resistance 0…∞ circuit

Chapter 8. LTR43 digital input/output and synchronization module

8.1 General description of LTR43

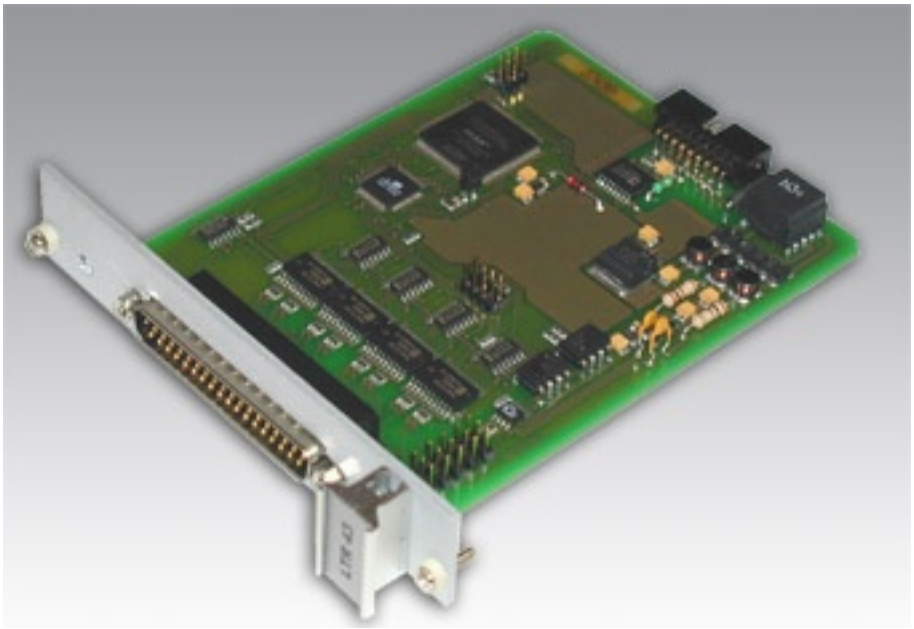


Fig. 8-1. LTR43 view

8.1.1 Device assignment

- Digital input/output of TTL-signals (5 B-logic) in asynchronous[1] mode.
- Digital stream input with an average input period from 10 ms to 10 μs (possible input irregularity is about 1 μs).
- Control of TTL-compatible external low-current (up to 10 mA) devices.
- Internal or external synchrosignals (synchroevents) synchronization of data collection in one crate or in multi-crate*system*.
- RS-485 interface for external user functions (in particular, for controlling multiple LE-41 charge amplifiers).

[1] asynchronous *that* means that strictly periodical data input-output is not supported.

8.1.2 General information about LTR43

- LTR43 has four 8-bit ports (32 lines in total) of asynchronous input/output of TTL signals on the user connector. Each of the four ports can be software-configured for both input and output. In addition, there is a possibility for forced *active zero to output state setting at powering-on* for each of the -4 ports by installing the appropriate jumper. In the latter case the proper port may be used for output only. *All 32 lines have pull-up resistors connected to high logic level (in LTR43), or to low logic level (in LTR43-0). This is the only functional difference of special LTR43-0 modification from LTR43 basic modification.* LTR43 module modifications have the similar software as LTR43-0[1], they are distinguished only in appearance by label on the module handle.
- 5 of 32-input-output lines may be configured with jumpers for an *individual galvanically isolated section* including external analog power supply and control lines. Among them are: two control interface data lines for RS-485, two external device power lines with a voltage of ±12 V (up to 120 mA at a total load power not exceeding 2.8 W) and one common power and interface RS-485 wire.
- LTR43 has 2 bi-directional TTL- synchronization lines: "START TAG" and "SECOND TAG".
- If the crate has one LTR43 module it may be used as a source of special format commands sent to the host-computer when an external or internal synchronization *event* occurs. Based on the procedure for data packets receiving from all LTR modules relative to packages of synchronization commands from LTR43, the host computer is able to reference the data sample input time in the certain LTR module to the synchronization *event*. *The method of synchronization implemented in LTR* is described in paragraph 4.7, page 91.
- Two types of synchronization events are *supported independently*: arrival of a *start tag* and arrival of a *second tag*. The *start tag may* be either external (TTL-signal "START TAG") or internal when it is generated by software. In the latter case it is also possible to translate the *start tag* out via the "START TAG" TTL- line of the connector, which allows for sending this signal to external devices including other LTR crates. The *second tag* may be used independently of the *start tag* and can be configured as an external tag("SECOND TAG" from connector), an internal tag (hardware-generated in LTR43 at 1 sec intervals), or as an internal tag with translation to output ("SECOND TAG" of the connector).
- Like the rest of LTR modules, all *inputs-outputs* at the user connector *are galvanically isolated* from LTR crate ground and from other modules but the inputs-outputs are connected to one another galvanically as they have the common line of digital ground GND. As was mentioned above,5 of 32-input-output lines may be configured with jumpers as an *individual galvanically isolated section* ; in this case, LTR43 will have two galvanically isolated signal sections.

8.1.3 LTR43 module configuration

The basic configuration of LTR43 is described in paragraph 2.4, page 29.

8.2 Installation and set-up

During LTR43 installation in crate, observe the module installation rules common for LTR system, see paragraph3.6.2, page 51.

Prior to the installation of LTR43, the jumpers should be located in the positions suitable for yourtask (Table 8-1, page 149, 8-2, page 150). Connectors location for configuration is shown on a

[1] Any LTR module has a unique serial number which is software-readable.

board section, Fig 8-2. The configuration shown in the figure is corresponding the following case: all 32 input-output lines are used, input-output lines are configured for input when LTR43 is powered on, the direction is set for each port by software.

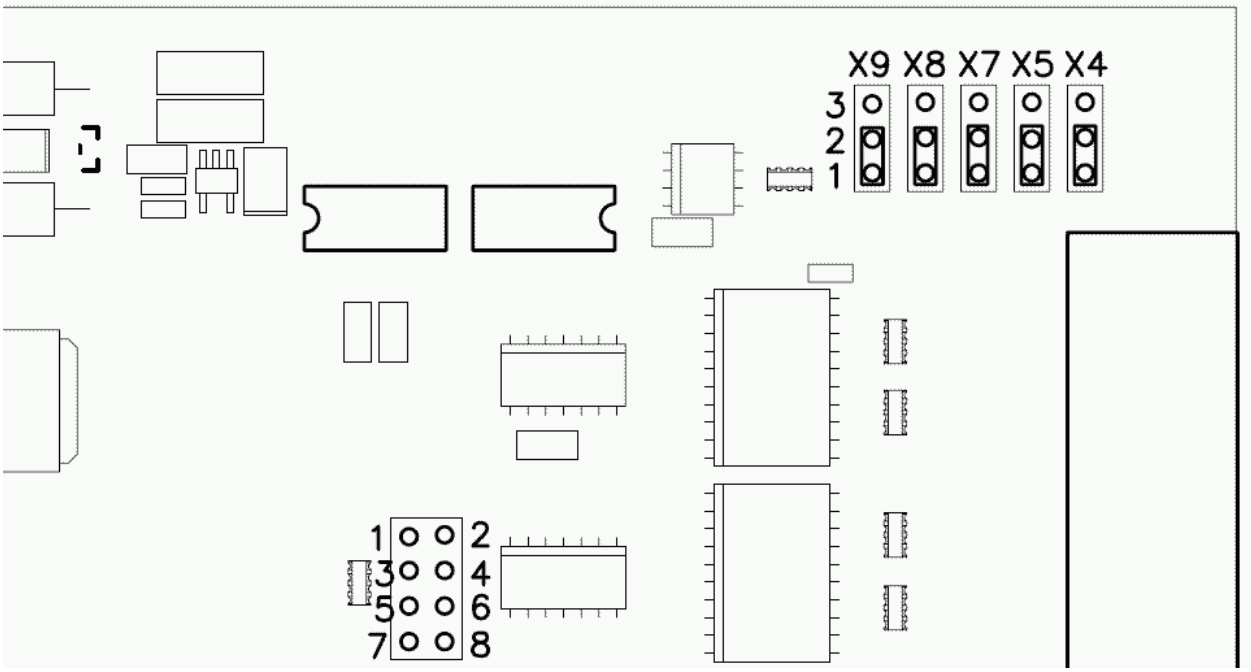


Fig.8-2. Configuration connectors layout

8.3 Overview of LTR43 hardware components and operation principles

8.3.1 Block diagram

The block diagram for LTR43 hardware engaged in data collection is shown in Fig.8-3.

Internal control in LTR43 is implemented with AVR ATmega8515 micro controller, which performs the following functions: receiving commands from the LTR interface, transmitting response command, program access to port registers.

It is noteworthy that despite of the possibility to set the 4 ports for different directions (input or output), *the input-output of all 32 bits data is always performed in parallel*: all ports configured to output update output logic levels simultaneously (with an accuracy of several nanoseconds), and all ports configured for input trip signal input levels simultaneously as well.

Alternative functions of IO1…IO5 lines are defined by jumper locations on connectors X4, X5, X7, X8, X9 (see Table 8-1, page 149).

The function of ports forcing for output with zero output logic level at LTR43 powering on is defined by setting four -jumpers for connection X6 (see Table 8-2, page 150).

All operating data on LTR43 module application are summarized in specification A.5 on page 156.

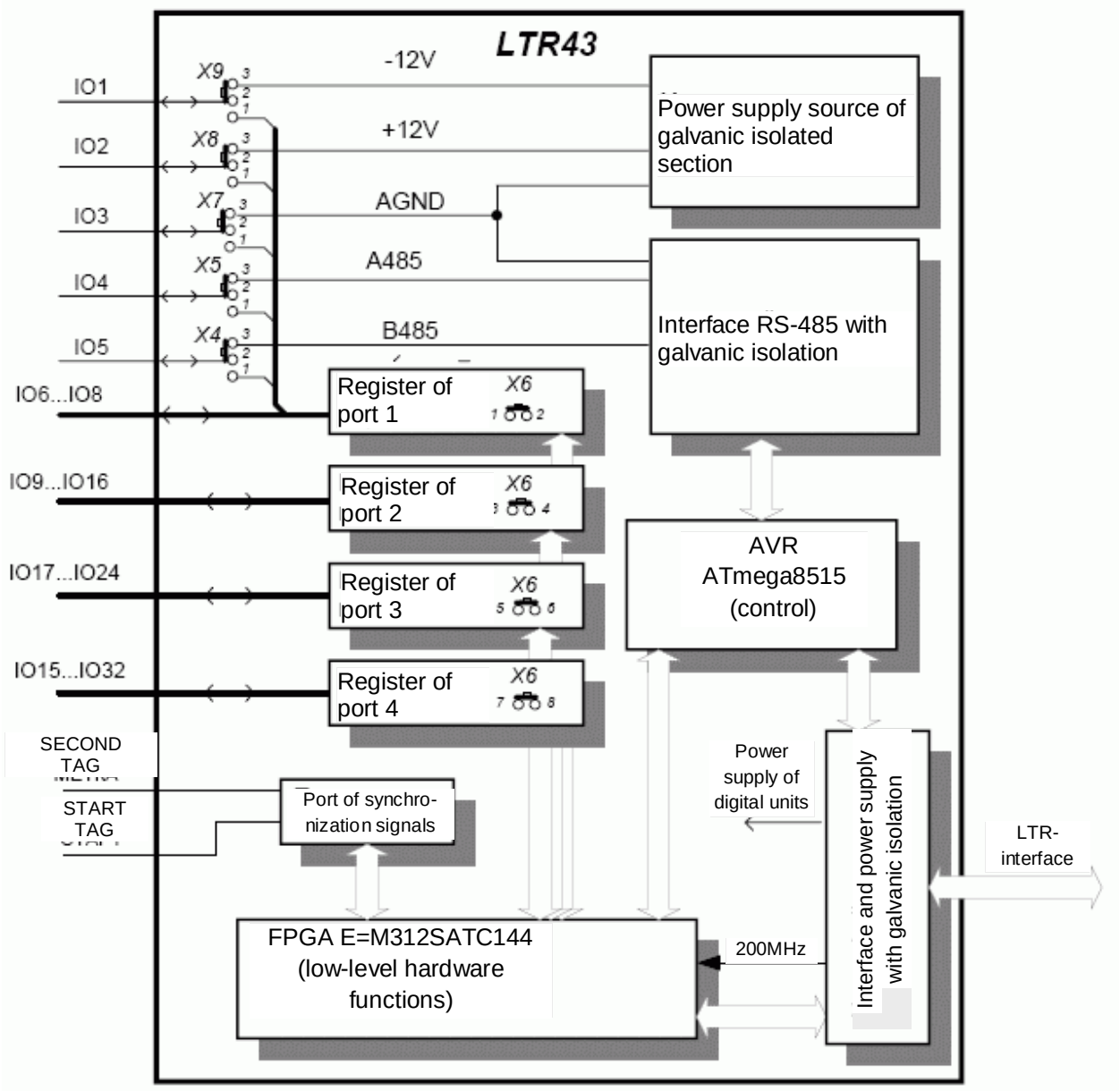


Fig.8-3. LTR43 module block diagram

8.3.2 LTR43 module control

8.3.2.1 Basic LTR- interface commands in application to LTR43 module

The common protocol of LTR- modules is described in paragraph 4.6.3, page 83. Formats of commands and data for LTR43 pre-determined at the hardware level are given below.

Command to LTR43			
1	**11uu uuuu**	**uuuu uuuu**	**uuuu uuuu**
<24>	<23..16>	<15..8>	<7..0>

Data <16..0> to LTR43			
0	**uuuu uuu0**	**dddd dddd**	**dddd dddd**
<24>	<23..16>	<15..8>	<7..0>

Data <31..17> to LTR43			
0	**uuuu uuu1**	**dddd dddd**	**dddd dddd**
<24>	<23..16>	<15..8>	<7..0>

Command from LTR43			
1	**uuuu uuuu**	**0000 0000**	**uuuu uuuu**
<24>	<23..16>	<15..8>	<7..0>

Data <16..0> from LTR43			
0	**uuuu uuu0**	**dddd dddd**	**dddd dddd**
<24>	<23..16>	<15..8>	<7..0>

Data <31..17> from LTR43			
0	**uuuu uuu1**	**dddd dddd**	**dddd dddd**
<24>	<23..16>	<15..8>	<7..0>

Time tags from LTR43			
1	**0000 0000**	**00ts 0000**	**0000 0000**
<24>	<23..16>	<15..8>	<7..0>

u *are* control bits available for AVR micro controller inside LTR43

d *are* data bits

1, 0 *are* pre-determined bit values

t *is* second tag

s *is* start tag.

The complete description of LTR43 commands is given in the document *"LTR Crate System. Programmer's Manual"*[1].

LTR43 control has the following features:

- If LTR43 is used as a synchronizing crate module, then to obtain the minimum range of delay time variations from the moment of external or internal synchronization signaling until the end of the synchronization packet output to the interface the data input operation should not be implemented because a situation is possible in which during the data packet input a synchronization event will occur and LTR43 hardware, naturally, will have to wait for the completion of the data packet output to transfer a special synchronization packet. However, if the required synchronization accuracy in the system *is* max. 10 μs, the data input may be performed at any moment of time.
- If the crate has several LTR43 modules, then it is recommended to use only one of them for synchronization in the crate.

8.3.3 Detailed description of synchronization signals

LTR43 supports *independently two types of synchronization events*: arrival of a *start tag* and arrival of a *second tag*. In any case, LTR43 sends time a tag packet to the interface in relation to these *events* (paragraph 8.3.2.1, page 146). Regardless of this, either of the two tags can be configured for different modes.

The *Start tag* can be configured by software to the following modes:

- **External**: in this case, the event occurs when the external device generates low to high level transition of TTL-"START TAG" signal (on the module connector)
- **Internal**: the event is triggered by according to a command to LTR43 module. In this mode, the TTL-line "START TAG" is configured for input and has no effect on LTR43.
- **Internal with translation to output**: the event is triggered by software according to a command to LTR43 module. In this mode, the start signal (a pulse generated by AVR) is translated via the TTL-line "START TAG" which is configured to output. The pulse duration (high level residence time) is about 500 ns, the initial level is low. This allows for sending a start signal to an external device or to other LTR modules (including other LTR crates).

The *Second tag* can be configured by software for the following modes:

- **External**: in this case, the event occurs when the external device generates low to high level transition of TTL-signal -"START TAG" *(on the module connector)*
- **Internal**: the event is triggered by hardware with a frequency of 1.0000 Hz (with the LTR crate single generator frequency accuracy, see Appendix A.16, page 359). In this mode, the TTL-line "SECOND TAG" is configured for input and has no effect on LTR43.
- **Internal with translation to output**: the event is triggered by hardware with a frequency of 1.0000 Hz. In this mode, the second synchronization signal (a pulse generated by hardware) is translated via the TTL-line "SECOND TAG" which is configured for output. The pulse duration (high level residence time) is about 470 ms, the initial level is low, the positive edge (that is used to send a synchronization packet to the interface) is from low to high level.

The issues of synchronization line electrical connections are considered in paragraph 8.4.5, page 148**.**

8.4 Connection of signals

Read the general rules for signal connection, paragraph 3.6.6, page 58.

LTR43 module has DRB-37M panel-mount connector for connection of input signals. External connections to LTR43 must be implemented by connecting signal circuits to the cable part of the connector (DB-37F type). Signal assignments are given in Table 8-1, page 149, and the view of the panel-mounted connector is presented in Fig. **Ошибка! Источник ссылки не найден.**. On the view: N/C line is a connector pin which is not connected inside LTR43. It is not recommended to connect it to any circuit.

LTR43 is compatible with external signals of TTL-levels. The question, certainly, is not about the logical elements according to the last century TTL technology as such but about the TTL logic levels standard with which modern logical elements are still compatible and which electronics manufacturers still refer to:
- “logic-0” level, max. +0.8 V;
- “logic-1” level, min.+2.4 V;
- Peak voltage -0.3...+5.3 V.

Isolated "dry contacts" (switching elements equivalent to isolated mechanical contacts) can be connected to LTR43 ports configured for input. A contact is connected relative to the GND circuit of LTR43 module. Closed state of the contact will correspond to "logic 0", opened state to "logic 1".

Not connected signals of LTR43 ports configured for input are in the "logic 1" state due to internal "pull-up resistors".

Table 8-1. Application of LTR43 user connector signals

Signal	Common point	Direction	State after connection	Description
IO1/-12 V 1) jumper X9 in position-1-2: IO1 2) jumper X9 in position-2-3: -12 V	1)GND 2)AGND	1) bi-directional 2) output	1) input and logic 0[1] 2) output	1) Signal IO1 of port 1 2) Power supply to external device
IO2/+12V 1) jumper X8 in position-1-2: IO2 2) jumper X8 in position-2-3: -12 V	1)GND 2)AGND	1) bi-directional 2) output	1) input and logic 01 2) output	1) Signal IO2 of port 1 2) Power supply to external device
IO3/AGND 1) jumper X7 in -position1-2: IO3 2) jumper X7 in position-2-3: AGND	1)GND 2)AGND	1) bi-directional 2) –	1) input and logic 01 2) –	1) Signal IO3 of port 1 2) Common wire of the galvanically isolated section of signals: -12 V, +12 V, A485, B485
IO4/A485 1) jumper X5 in position-1-2: IO4 2) jumper X5 in -position2-3: A485	1)GND 2)AGND	1) bi-directional 2) bi-directional	1) input and logic 01 2) input	1) Signal IO4 of port 1 2) Data line A of RS-485 interface
IO5/B485 1) jumper X4 in position-1-2: IO5 2) jumper X4 in position-2-3: B485	1)GND 2)AGND	1) bi-directional 2) bi-directional	1) input and logic 01 2) input	1) Signal IO5 of port 1 2) Data line B of RS-485 interface
IO6…IO8	GND	bi-directional	input and logic 01	Port 1
IO9…IO16	GND	bi-directional	input and logic 01	Port 2
IO17…IO24	GND	bi-directional	input and logic 01	Port 3
IO25…IO32	GND	bi-directional	input and logic 01	Port 4

[1] independently configured by jumpers for each port, see Table 8.2; logic 1 level will be available on the unconnected digital line configured for input due to the availability of 4.7 kOhm internal pull-up resistor (to +5 V)

Signal	Common point	Direction	State after connection	Description
START TAG	GND	bi-directional	input	START TAG
SECOND TAG	GND	bi-directional	input	SECOND TAG
GND	–	–	–	Common wire of digital - TTL-lines IO1…IO32

By default, if only digital input-output lines are used in LTR43, jumpers X4, X5, X7, X8, X9 should be pre-set in position 1-2.

If RS-485 is used only, jumpers X4, X5, X7 should be set in position 2-3 while jumpers X8 and X9 should be left in position 1-2.

While connecting up to 4- charge amplifiers LE-41, powered from LTR43 module and using its RS-485 interface, jumpers X4, X5, X7, X8, X9 should be set in position 2-3.

Table 8-2. LTR43 ports configuration

X6 connector pins	Jumper	Port state when powered on	Operating port state
1-2	not installed	port 1 - input	software-specified direction
1-2	installed	port 1 – output in logic0 (paragraph 8.4.4, page 153)	in operation – always active output only
3-4	not installed	port 2 – input	software-specified direction
3-4	installed	port 2 – output to logic0 (paragraph 8.4.4, page 153)	in operation – always active output only
5-6	not installed	port 3 - input	software-specified direction
5-6	installed	port 3 – output to logic0 (paragraph 8.4.4, page 153)	in operation – always active output only
7-8	not installed	port 4 – input	software-specified direction
7-8	installed	port 4 – output to logic0 (paragraph 8.4.4, page 153)	in operation – always active output only

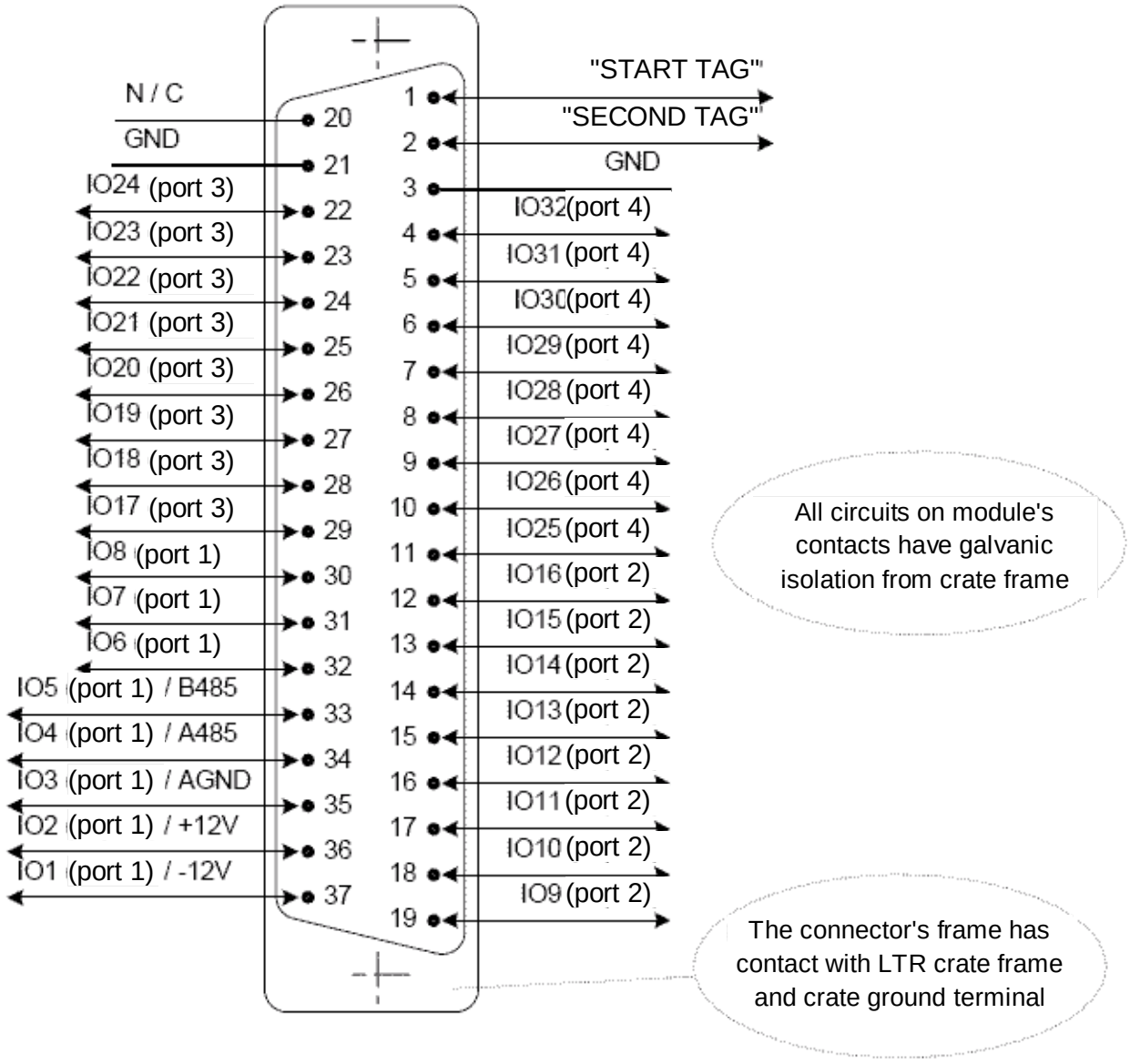


Fig.8-4. LTR43 module connector signals

8.4.1 Characteristics of signal line inputs and outputs

! When connecting LTR43 module to your system, strictly observe the parameters specified in tables of this section.

The manufacturer shall not be warranty liable for LTR43 failure caused by violation of maximum permissible operation conditions .

The characteristics of galvanic isolation in LTR are given in Appendix A.18, page 362.

The following symbols are given in tables of this section:

- **DIO** – digital bi-directional TTL-line;
- **RS-485** – digital bi-directional line of RS-485 interface;
- **P** – external device power output.

8.4.2 LTR43 operating mode

LTR43 module installed in LTR crate has the following characteristics of input and output signal lines after LTR crate is powered on:

Table8-3. LTR43. Line characteristics, operating mode

Signal	Type	Input impedance	Maximum permissible conditions at input	Maximum permissible conditions at output	Pull-up resistor
IO1…IO32	DIO	4.7 kOhm (LTR43) 2.2 kOhm (LTR43-0)	-0.3…+5.5 V relative to GND	±30 mA at –0.3…+5.5 V relative to GND	4.7 kOhm relative to +5 V[1] (LTR43) 2.2 kOhm relative to GND (LTR43-0)
A485, B485	RS-485	12 kOhm	±12 V relative to AGND[2]	±12 V relative to - AGND2	–
-12 V, +12 V	P	–	–	±120 mA relative to AGND at total power delivered as a load not exceeding 2.8 W	–
START TAG, SECOND TAG	DIO	min. 1 MOhm when switched on to input	-0.3…+5.5 V relative to GND	±20 mA at –0.3…+5.5 V relative to GND	–

8.4.3 LTR switched-off state

Module switched-off state is described in paragraph 4.8, page 93.

[1] internal power voltage +5V of LTR43 module.

[2] the specifications of RS-485 ADM483EAR interface transceiver used in LTR43 can be found on manufacturer's site www.analog.com

Table8-4. Characteristics of the lines, module is switched off

Signal	Type	Input impedance	Maximum permissible conditions at input	Maximum permissible conditions at output	Pull-up resistor
IO1…IO32	DIO	Hundreds Ohm[1]	-0.3…+5.5 V at current to ±30 mA - relative to GND	±30 mA at –0.3…+5.5 V relative to GND	–
A485, B485	RS-485	Hundreds Ohm	±12 V relative to AGND	±12 V relative to AGND	–
-12 V	P	–	–	0…-15 V relative to AGND	–
+12 V	P	–	–	0…+15 V relative to AGND	–
START TAG, SECOND TAG	DIO	Hundreds Ohm	-0.3…+5.5 V at current to ±40 mA - relative to GND	±20 mA at –0.3…+5.5 V relative to GND	–

8.4.4 LTR43 outputs behavior at powering on-off in the pre-set initial state *"positive zero to output"*

There are tasks when it is important that pure logic-0 level be at the module inputs when powered on-off without any transition processes. Let us consider how to achieve that for LTR43.

After LTR crate switching on-off, the power voltage in LTR43 increases/drops with a non-infinite rate. Hence, output buffers when being forced *to positive 0* at output for a short-time (for tens of milliseconds) pass a stage when their power voltage is between zero and normal value. In this short-time state, the buffers can not produce normal logic-0 output current and, since in the basic delivery option of LTR43 each digital input-output line has an internal pull-up resistor to +5 V power circuit, this leads to the effect of *logic-0 level short-time raising up to* 0.8 V[2] once after LTR crate powering on/off. If it is crucially for your application software, this problem can be solved in two ways:

- Use an external pull-up resistor to zero (a 1…1.5 kOhm resistor connected between the output and GND circuit.
- Order in L-CARD a modification of LTR43-0- with internal pull-up resistors to zero.

8.4.5 Principles of synchronization lines connection in LTR41, LTR42, LTR43

Electric bi-directional TTL synchronization lines "START TAG" and "SECOND TAG" are implemented identically in LTR41, LTR42, LTR43 -modules. These lines are set for input when powered on by default. The internal circuitry of synchronization lines is shown in Fig. 8-5. A *Z-state* output is implemented with the use of 74ACT125 transmitter, and an input with the use of 74HCT14 receiver.

[1] positive potential at input

[2] the typical peak pulse value relative to GND is specified, the maximum possible value is not guaranteed

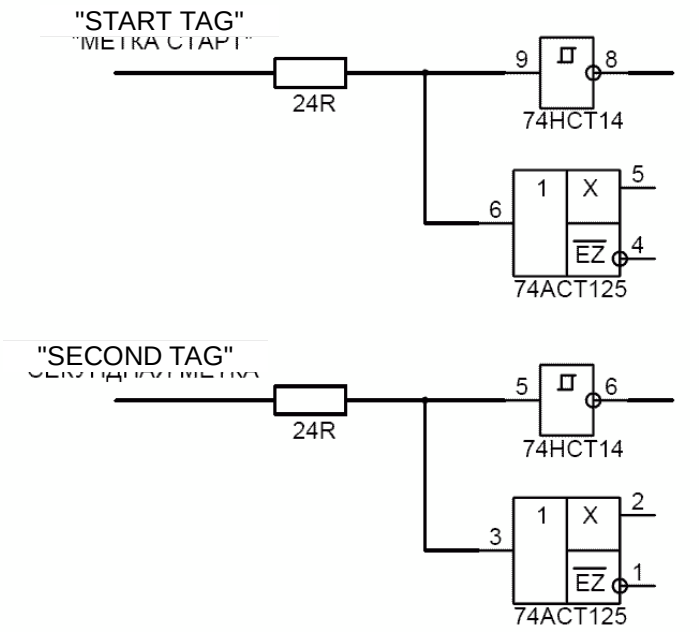


Fig.8-5. LTR41-LTR43. Diagram of synchronization line transmitter/receiver unit

It is assumed that the initial state of the synchronization lines is low logic level, and in case when all devices connected to a synchronization line are configured for input (for example, at the moment of powering-on), the logic 0 state can only be ensured by using a pull-up resistor to zero (to GND circuit) if such resistor is no more available in connected equipment.

The total resistance of synchronization line pull-up resistor to GND should not be less than 75 Ohm including all resistors connected to the synchronization line relative to GND.

When connecting LTR43 synchronization lines to an external device having a synchronization input with pull-up resistor to 1, it should be taken into account that the external device can recognize the LTR43 transition from the initial state (or switched-off - state) in state of lines …*with translation to output* as a false synchronization pulse.

8.4.6 Internal arrangement of LTR43 inputs-outputs

LTR43 input-output lines are bi-directional, see fig.8-6. When the line is configured for output, 74HCT573 register output is in active state while in case of line configured for input this output is in Z-state.

Both input and output signals IO1…IO32 are gated synchronously to each other. Previous (i-1) state at the input register is not changed when i-state of the output register is delivered to the output.

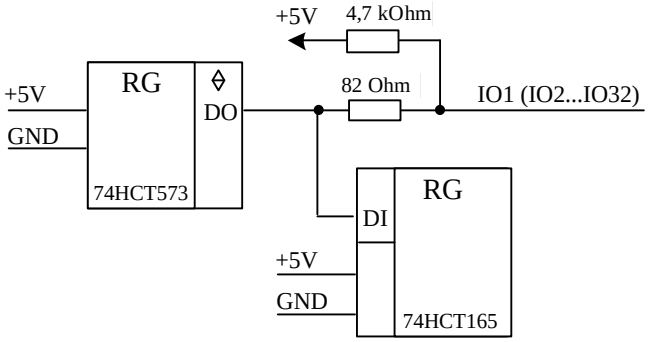


Fig.8-6. LTR43. Interior arrangement of circuits IO1…IO32

LTR43-0 has a modification with 2.2 kOhm pull-up resistors connected relative to GND which can be ordered, see fig.8-7.

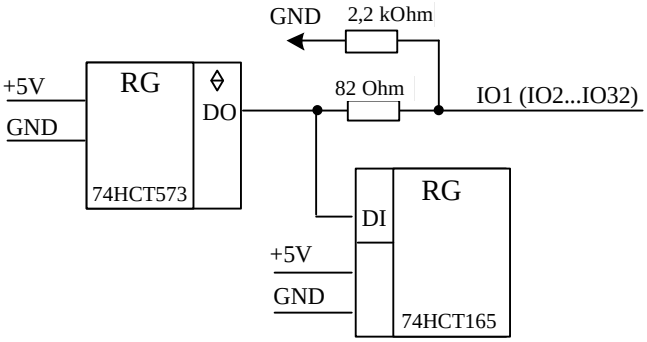


Fig.8-7. LTR43-0. Interior arrangement of circuits IO1…IO32

LTR43-0 has an identification label "LTR43-0" on the handle of the module front panel. LTR43 and LTR34-0 modules are equivalent in terms of software.

Chapter 9. LTR41 и LTR42 modules of digital input, output and synchronization have channel-by-channel galvanic isolation

9.1 General description of LTR41 and LTR42

This document contains preliminary data about LTR41 and LTR42. The complete data will be presented in the next revisions of this document.

9.1.1 Devices application

- LTR41: Digital input of 16- TTL/CMOS- signals (5 V- logic) as well as current logic signals (to 25 mA) with channel-by-channel optical isolation.
- LTR42: Output of 16- control signals by external actuators via optorelay outputs with channel-by-channel galvanic isolation. **Opto-relay actuating circuit may be connected into DC or AC circuits**.
- LTR41 and LTR42 operate in the asynchronous input-output mode (accordingly). This means that strictly periodical data input-output is not supported.
- Internal or external synchrosignals (synchroevents) synchronization of data collection in one crate or in multi-crate *system*. In LTR-crate, at least one LTR41, LTR42, or LTR43 module is sufficient to support data collection synchronization functions.

9.1.2 General information about LTR41, LTR42

- LTR41 has one 16-bit port for asynchronous input of signals with channel-by-channel optical isolation at the user connector.
- LTR42 has one 16-bit port for asynchronous output of signals of external actuators control by opto-relay at the user connector.
- LTR41 and LTR42 have an individual galvanically isolated group of signals comprising:
  - two bi-directional TTL-lines of synchronization: "START TAG" and "SECOND TAG" (similar to LTR43);
  - external device stabilized power supply output +5 V 0.5 A.
- If the crate has at least one LTR41, LTR42 or LTR43 module it may serve as a source of special format commands sent to the host computer when *an external or internal synchronization event occurs*. Based on the procedure for data packets receiving from all LTR modules relative to packages of synchronization commands from LTR41 (LTR42, LTR43), reference the data sample input time in the certain LTR module to the *synchronization event*. *The method of synchronization implemented in LTR* is described in paragraph 4.7, page 91.

- Two types of synchronization events are *supported independently*: arrival of a *start tag* and arrival of a *second tag*. The *start tag may* be either external (TTL-signal "START TAG") or internal when it is generated by software. In the latter case it is also possible to translate the *start tag* out via the "START TAG" TTL- line of the connector, which allows for sending this signal to external devices including other LTR crates. The *second tag* may be used independently of the *start tag* and can be configured as an external tag("SECOND TAG" from connector), an internal tag (hardware-generated in LTR41 (LTR42, LTR43) at 1 sec intervals), or as an internal tag with translation to output ("SECOND TAG" of the connector).

9.1.3 Configuration of LTR41, LTR42 modules

The basic configuration of LTR41, LTR42 is described in paragraph 2.4, page 29.

9.2 Installation and set-up

During LTR41, LTR42 installation in crate, observe the module installation rules common for LTR system, see paragraph 3.6.2, page 51.

9.3 Overview of LTR41 and LTR42 hardware components and operation principles

9.3.1 Block diagram

Block diagrams of LTR41, LTR42 modules are given in Fig. 9-1.

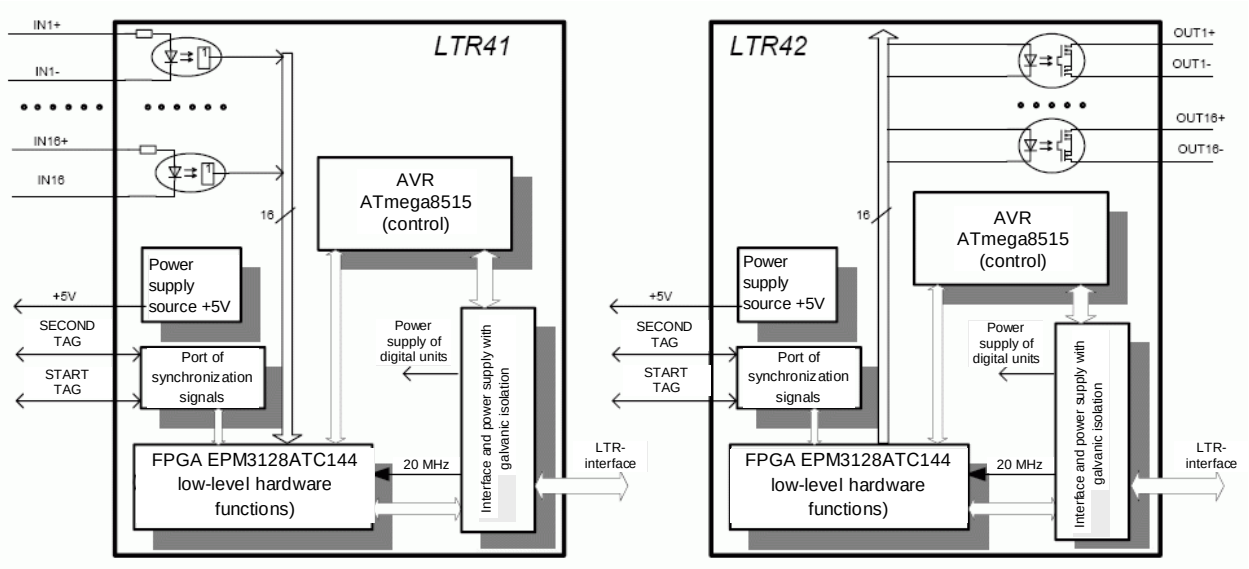


Fig.9-1. Block diagrams of LTR41, LTR42 modules

The only difference between LTR41 and LTR42 modules in terms of architecture is that the first one is configured for parallel input of 16- data bits and the second one for parallel output of 16- data bits. In all other respects these modules are identical.

Similarly to LTR43, internal control in LTR41, LTR42 is implemented with AVR ATmega8515 micro controller:

The **input circuit in LTR41** is made based on optron *HCPL-2630*[1] with diode protection, fig.9-2.

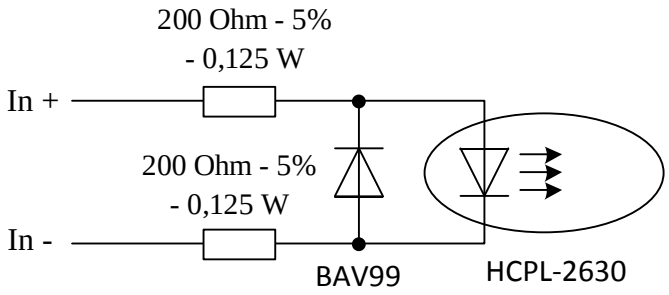


Fig.9-2. LTR41 input circuit electric diagram.

All operating data for LTR41 module application are given in Appendix A.6, page 335. Estimated current-voltage characteristic of the input circuit of one channel of LTR41 is given in Fig.9-3.

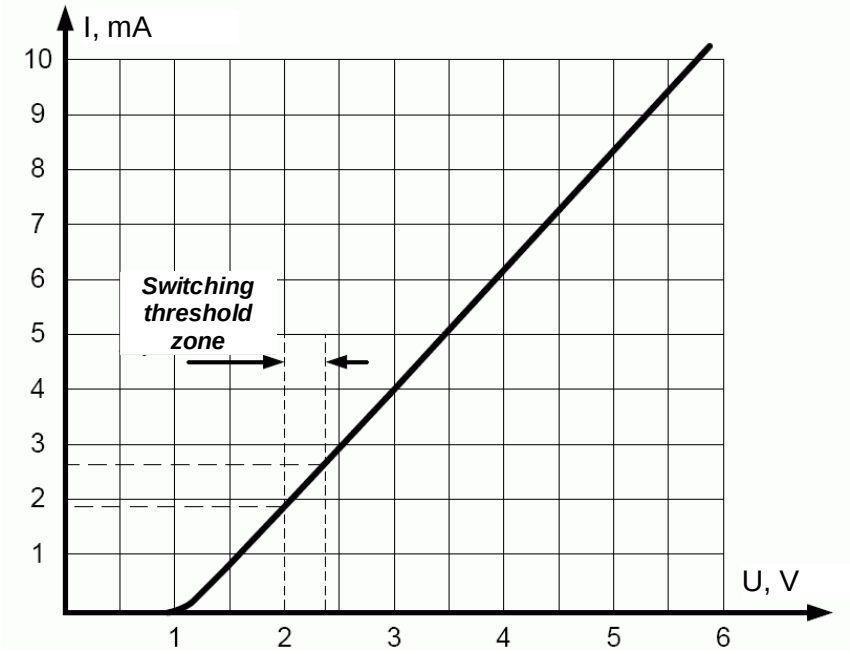


Fig.9-3. LTR41 input circuit current-voltage characteristic

It also should be noted that in principle it is allowed to supply a slowly varying signal to LTR41 input because there is a hysteresis effect (about 0.1 V in voltage) in the switching threshold zone and logically indeterminate state is excluded. The given current-voltage characteristic shows that ***LTR41 can be also used to receipt current signals with switching threshold of about 2 mA.***

CPC1035N optorelays serve as an optorelay *output* in LTR42.[1] LTR42 specifications are given in Appendix A.7, page 336.

[1] the manufacturer is Clare, Inc. www.clare.com

9.3.2 Control of LTR41 and LTR42 modules

9.3.2.1 Basic LTR-interface commands are presented in Appendix to LTR41 and LTR42 modules

The common protocol of LTR- modules is described in paragraph 4.6.3, page 83. Formats of command and data for LTR41 and LTR42 are similar to LTR43 formats, paragraph 8.3.2.1, page 146 (except for that in LTR41, LTR42 low 16 data bits of LTR43 32-bit format are used as 16-data bits-), so they are not considered here.

The full description of LTR41, LTR42 commands system is given in the document "LTR Crate System. Programmer's Manual"[1].

LTR41 and LTR42 have the following features:

- **LTR41 does not perform input signal levels inversion**, in other words, high level of input signals (high level in terms of current and voltage) is coded as logical one and low level as logical zero.
- When using LTR42 it should be taken into account that **the open state of current executive circuit of optorelay (minimum current) is coded as logical zero, and closed state of executive circuit (maximum current) is coded as logical one.**
- If LTR41 is used as a synchronizing crate module, then to *obtain the minimum range of delay time variations from the moment of external or internal synchronization signaling until the end of the synchronization packet output to the interface the* data input operation should not be implemented because a situation is possible in which during the data packet input a synchronization event will occur and LTR41 hardware, naturally, will have to wait for the - completion of the data packet output to transfer a special synchronization packet. However, if the required synchronization accuracy in the system is max. 10 μs, the data input may be performed at any moment of time.

9.3.3 Detailed description of synchronization signals

The synchronization signals are similar to those described in paragraph 8.3.3, page 147

9.4 Connection of signals

! Read the general rules for signal connection, paragraph 3.6.6, page 58.

LTR41 and LTR42 modules have panel-mount connector DRB-37M to connect signals. External connections to LTR41 and LTR42 should be implemented by connecting signal circuits to the cable part of the connector (DB-37F type). Signal assignments are given in Table 9-1, and the view of the panel-mounted connector is presented in Fig.9-4.

! When connecting signals to LTR41, LTR42 it should be noted that the modules have 17 galvanically isolated signal sections each: 16 inputs (outputs) plus one section for synchronization and power supply to an external device. It should be noted that circuits of common wires GND and GNDP are connected at one point inside LTR41 (LTR42). Synchronization signals should be sent (cleared) relative to GND connector pin and external device power current from circuit of +5 V should be cleared relative to GNDP pin. This method allows for separating external device power supply current flow circuit from the common wire of the synchronization line to ensure proper (failure-free) operating conditions for the module.

Principles of synchronization lines connection in LTR41, LTR42, LTR43 are set out in paragraph 8.4.5, page 159**.**

Table9-1. Assignment of user connector signals in LTR41, LTR42 modules

Signal	Common point	Direction	State after connection	Description
+5 V	GNDP			External device power output
IN1+ IN1- … IN16+ IN16-		input	input	Galvanically isolated inputs of channels from 1 to 16. In LTR41, 16 inputs have 2 lines "+" and 2 lines "-" for application of positive and negative potential of the signal source, respectively.
OUT1+ OUT1- … OUT16+ OUT16-		output	no current in executive circuits of optorelay[1]	Galvanically isolated outputs of channels from 1 to 16. In LTR42, 16 inputs have 2 lines "+" and 2 lines "-" for executive current of output optorelays of LTR42 module Symbols "+" and "-" are merely a convention because current passage direction in the executive circuit may vary.
START TAG	GND	bi--directional	input	START TAG
SECOND TAG	GND	bi--directional	input	SECOND TAG
GND				– Common wire circuit of signals START TAG and SECOND TAG
GNDP				– Common wire circuit of +5 V external device power source

9.4.1 Characteristics of signal line inputs and outputs

! When connecting LTR41 and LTR42 modules to your system, strictly observe the parameters specified in tables of this section.

The manufacturer shall not be warranty liable for LTR41 and LTR42 failure caused by violation of maximum permissible operation conditions.

The characteristics of galvanic isolation in LTR are given in Appendix A.18, page362 .

The following symbols are given in tables of this section:

- **DIO** is digital bi-directional TTL-line;
- **DI+ DI-** is galvanically isolated pair of digital input lines (LTR41);
- **DO+ DO-** is galvanically isolated pair of digital output lines (LTR42);
- **P** is external device power output.

9.4.2 LTR41, LTR42 operating mode

LTR41 (LTR42) modules installed in LTR crate has the following characteristics of input and output signal lines after LTR crate is powered on:

[1] equivalently to open relay contacts - this state is coded as logic 0 level

Table9-2. LTR41, LTR42: line characteristics, operating mode

Signal	Type	Input impedance	Maximum permissible conditions at input	Output impedance	Maximum permissible conditions at output	Pull-up resistor
IN1- IN1+ … IN16- IN16+	DI+ DI-	about 700 Ohm	±12 V between IN_i+ and IN_i- ±25 mA in the continuous operation mode	–	–	–
OUT1-OUT1+ … OUT16- OUT16+	DO+ DO-			30 Ohm and above 50 MOhm in the switched-on and switched-off states of optorelay	to ±70 mA in the switched-on state and ±250 V in the switched-off state of optorelay	–
+5 V	P	–	–	–	±300 mA relative to GNDP	–
START TAG, SECOND TAG	DIO	min. 1 MOhm if configured for input	-0.3…+5.5 V relative to GND	–	±40 mA at –0.3…+5.5 V relative to GND	–

9.4.3 LTR switched-off state

Module switched-off state is described in paragraph 4.8, page 93.

Table 9-3
LTR41, LTR42: line specifications, modules are off

Signal	Type	Input impedance	Maximum permissible conditions at input	Output impedance	Maximum permissible conditions at output	Pull-up resistor
IN1- IN1+ … IN16- IN16+	DI+ DI-	about 700 Ohm	±12 V between IN_i+ and IN_i-	–	–	–
OUT1- OUT1+ … OUT16- OUT16+	DO+ DO-			above 50 MOhm – corresponds to the switched-off state of optorelay	up to ±250 V	–
START TAG, SECOND TAG	DIO	Hundreds Ohm[1]	-0.3…+5.5 V at current up to ±40 mA relative to GND	–	±40 mA at –0.3…+5.5 V relative to GND	–

[1] positive potential at input

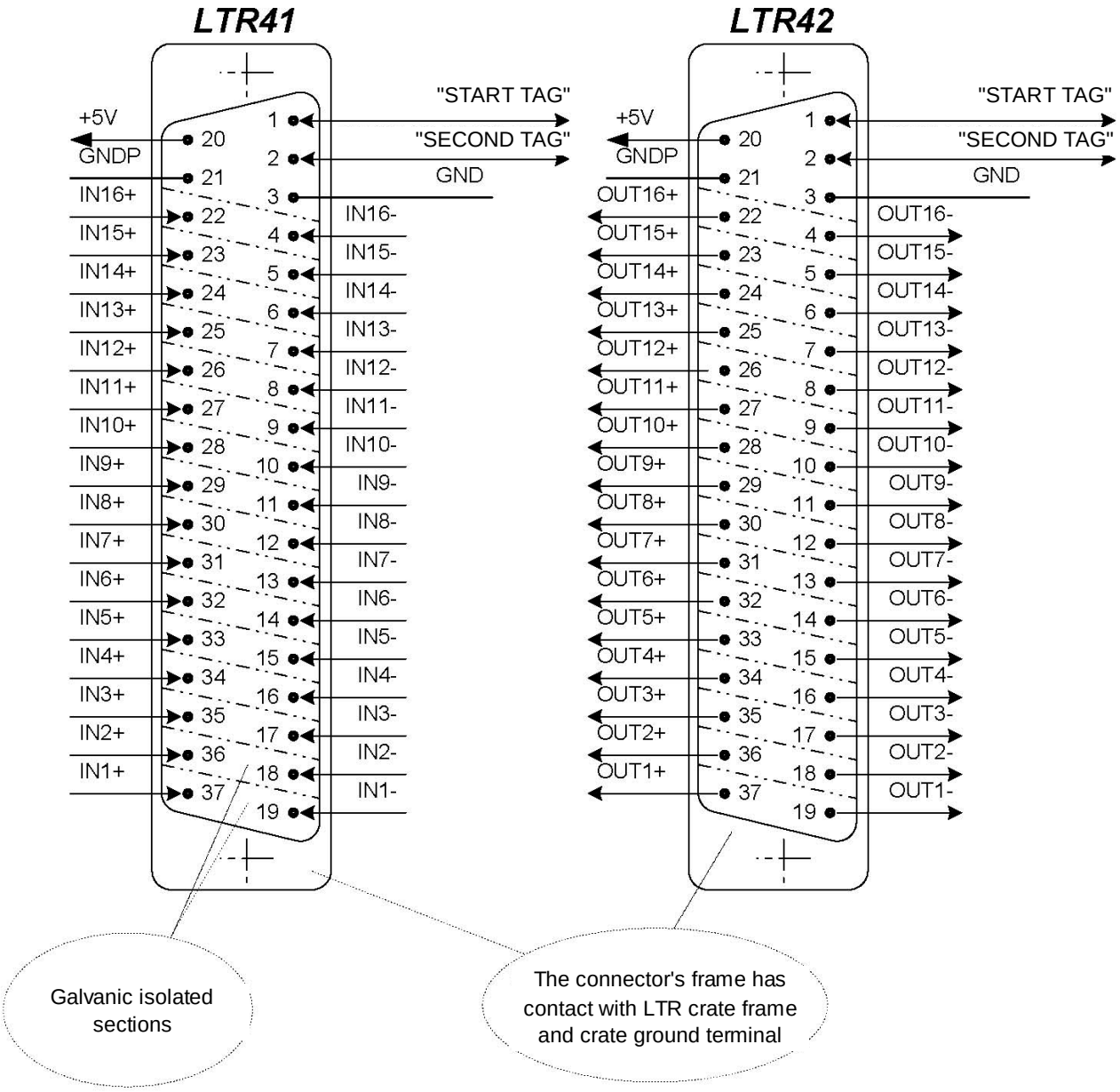


Fig.9-4. Signals at LTR41 and LTR42 module connectors

9.4.4 Special cases of connection

9.4.4.1 LTR41 input voltage range extension

LTR41 input voltage range is ±12 V. To extend this range, a multiplier resistor R1 can be connected sequentially into LTR41 input circuit,fig.9-5. R1 resistor rating should be selected based on the following rule:

- To obtain input range of LTR41 ±(12+U) V, where U>0, you need to select multiplier resistor resistance:
  R1 = 40.2*U and resistor capacity (W) min. $\mathbf{U^2/R}$
  (where units are U –Volt, R1 – Ohm).
- Multiplier resistor R1 shifts LTR41 typical voltage triggering threshold. Voltage triggering threshold U_t with the use of multiplier resistor R1: U_t = **R1*0.0021 + 2.2**
  (where units are R1 – Ohm, U_t – Volt);

- Multiplier resistor R1 does not **shift** LTR41 typical current triggering threshold equal to 2.1 mA.

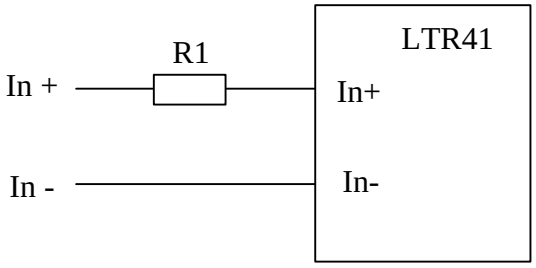


Fig.9-5. Pertains to LTR41 input range extension

It is recommended to define LTR41 input range with a margin of min. 20% to avoid continuous operation of internal and external resistors of LTR41 input circuit under maximum power dissipation.

When connecting LTR to any circuits, the ganvanic isolation characteristics should be taken into account, Appendix A.18, page 362

Chapter 10. LTR51 frequency metering module

10.1 General description

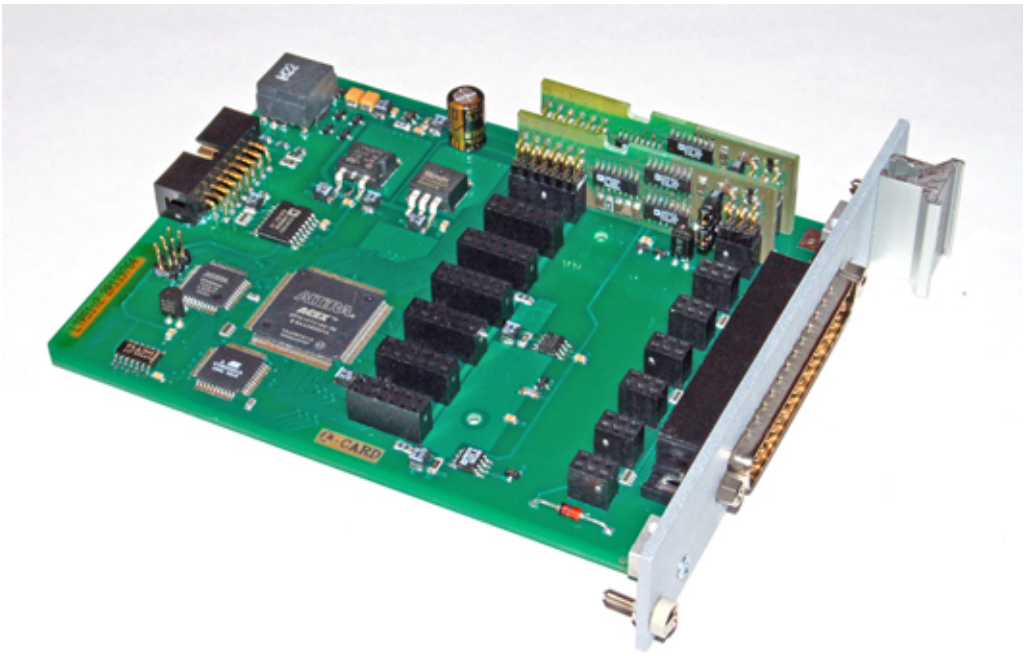


Fig.10-1. LTR51 view

10.1.1 Device application

LTR51 module is intended for multichannel measurement of frequencies and time intervals of complex signals and for multi-channel detection of signals by selecting at a programmable level.

10.1.2 Features

- Possible configuration with two types of submodules *(* **low-frequency**H-51FL and **high-frequency** H-51FH) differing with upper cutoff frequency of analog path allows to improve noise immunity of frequency measurement process for low-frequency applications (to 10-15 kHz) if low-frequency *module is* used.
- **Extended configuration** of LTR51 module allows to expand channels from 2 to 16 by installing -2-channel submodules H51Fx- on LTR51 carrier-board -.
- The frequency meter comprises a selection (calibration) **diagram for input signal selection by level with programmed upper and lower hysteresis thresholds** for measuring complex signals frequencies. Programmed hysteresis thresholds provide a debouncing effect for the input threshold device by their setting up *at desired levels and* thereby allow to avoid errors in measuring complex signals frequencies.

- **Two ranges of signal selection diagram thresholds with 256 levels per range**. The level of set threshold (in Volts) is determined by two factors:
  - set threshold range **defined by** jumpers on submodules H51Fx *independenty* for each of the channels
  - software-defined **threshold level** within the selected range; 256 levels of programmed thresholds are defined independently for each of channels

! LTR51 has input range of ±10 V for any defined range of thresholds.

- LTR51 is an analog of H-51 module. Parallel data acquisition from the channels and intermediary results issuing is *performed* by hardware by loaded FPGA EP1K10TC144[1] (in the analog module H-51 of H-2000 family the same functions were performed by signaling processor). **Calculation of signal frequency or period should be carried out by a top-level program based on intermediate data**
- Each of 16- channels of the frequency meter can be set independently for the mode of counting positive edges "on edge" or "on drop".
- Flexible downloaded architecture of LTR51 allows for assigning completely different functions to the same module hardware. For example, LTR51 can be transformed into a **logic analizer** by downloading another FPGA firmware without taking module out of the crate. L-Card is ready to consider the possibility of such implementations at your request.

! Do not confuse the concepts: **submodule input range** (Table 10-2, page 170) with **comparator hysteresis thresholds setting range** for this submodule channel (see Table 10-1, page 170 and Fig. 10-3, page 167).

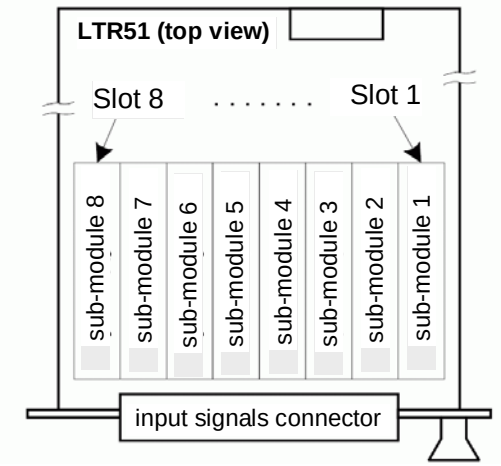


Fig.10-2. LTR51. H-51x submodules arrangement

10.2 Installation and set-up

LTR51 has 8 slots for installation of H-51FH or H-51Fx submodules.

[1] manufacturer: Altera Corporation

LTR51 can be supplied with submodules of both types in the quantity from 1 to 8 pcs., which can be installed in any slots in any order. As shown in Fig. 10-2, the slots in LTR51 are numbered from 1 to 8[1].

It is required to set the desired hysteresis threshold range for each module. The range is set for each channel using an individual jumper, and **jumpers state is program-invisible.**

X3 and X4 jumpers arrangement on H-51Fx module is shown in Fig. 10-3. Jumpers specify the input calibration threshold setting range in accordance with Table 10-1.

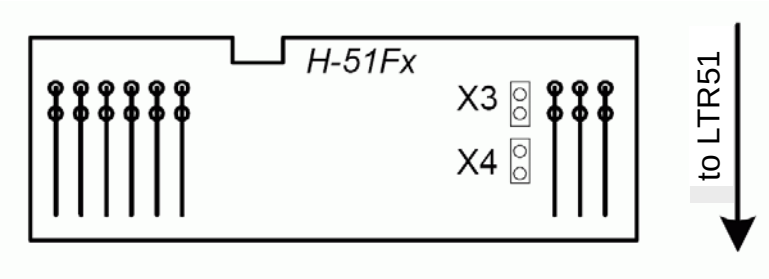


Fig.10-3. Jumpers arrangement for thresholds setting

X3 jumper corresponds to submodule channel 1, X4 jumper to submodule channel 2.

Table10-1. H-51Fx. Jumpers arrangement and corresponding parameters

Submodule channel	Jumper X3	Jumper X4	Threshold range, V	Threshold setting pitch, V
1	Installed	-	-1.2 V… +1.2 V	9.5 mV
	Not installed	-	-10 V… +10 V	79 mV
2	-	Installed	-1.2 V… +1.2 V	9.5 mV
	-	Not installed	-10 V… +10 V	79 mV

! A relative disadvantage of LTR51 module is the lack of a mechanism for reading the configuration of submodules and threshold ranges set by the user. To overcome this, the user can enter the configuration information into the free space of AVR micro controller flash memory by himself, see LTR Crate System. Programmer's Manual"[1]. In this case, if several LTR51modules are used, their configuration will be distinguished by software.

10.3 Overview of LTR51 hardware components and operation principles

LTR51 operation principle is based on calculation of number of pulses with unknown frequency at the measuring submodule output for a specific time range with simultaneous recording of the final pulse arrival time within this range. LTR51 i*mplements a* comprehensive method of measure frequency and period measurement. Measurements are carried out in such a way that time intervals form a continuous sequence.

10.3.1 Block diagram

LTR51 contains the following functional units (Fig. 10-4):

- Galvanically isolated LTR interface unit

[1] see the numbering agreement 3.1.2 on page 12

- AT8515 AVR micro controller which receives commands from the LTR interface, sends response commands, and performs the internal control of LTR51/LTR51Fx
- 8-slot system for installation of submodules H-51Fx
- ±2.048 V reference voltage source (RVS) used by submodules LTR51FX in a precision circuit for generating tripping thresholds during the selection of input voltage by level.
- Field-programmable circuit array FPGA EP1K10TC144 implementing digital counting units. FPGA configuration is loaded via the LTR interface every time when module is switched on.

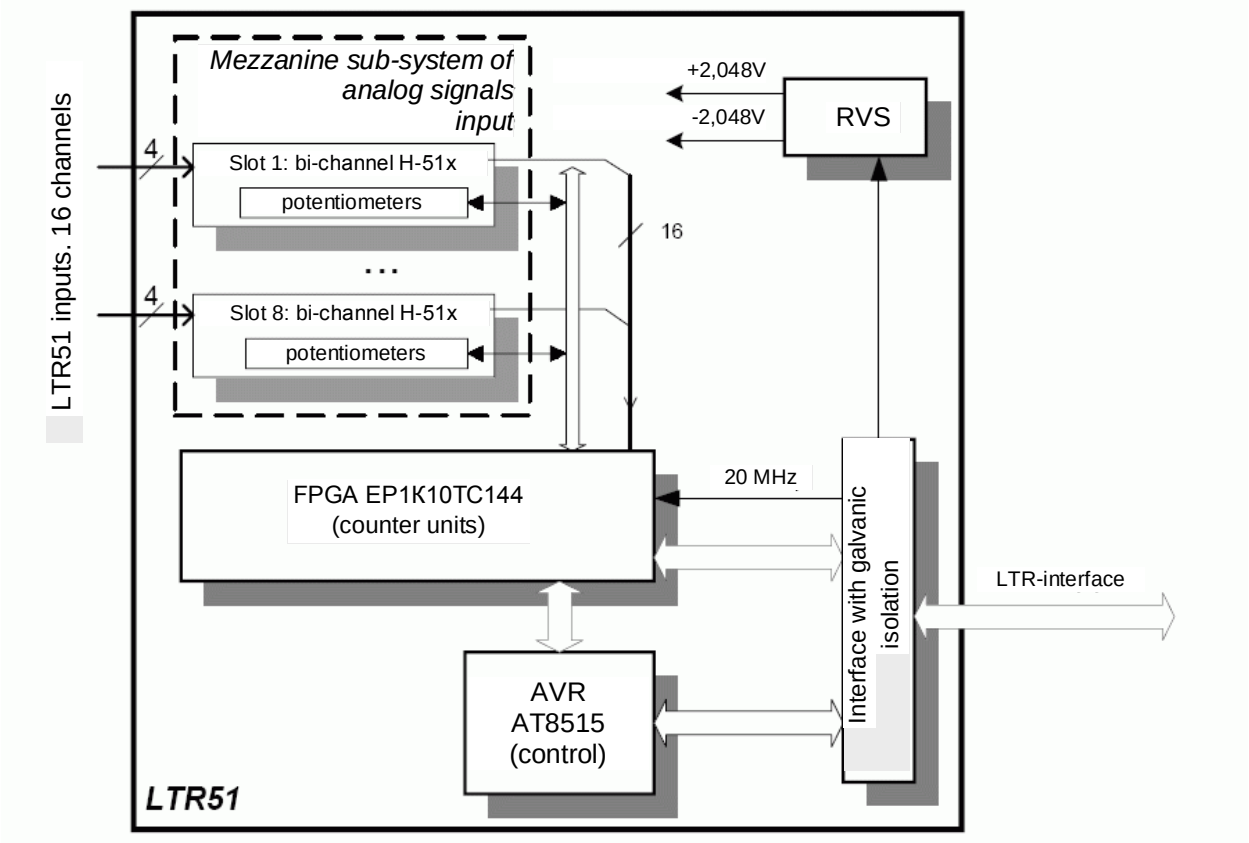


Fig.10-4. LTR51. LTR51 module block diagram

Input signals come to the corresponding input 1…16 of H-51 module and are translated to the corresponding inputs *+CH1…16* of bi-channel submodules H51Fx. Inputs 1…16, in terms of internal connections, are *single-phase voltage inputs with group galvanic isolation of* 16 inputs relative to external circuits. Circuit *AGND* is a common wire for connection of single-phase input signals.

LTR51Fx submodule block diagram (Fig.10-5) contains:

- *input signal scaling amplifier* with a possibility to set two values of each channel gain factors using jumpers *X3* or *X4*
- *bi-threshold diagram of input signal selection* by level, which, in turn, consists of:
  - two programmable *potentiometers* setting the voltage of the upper and the lower thresholds
  - two comparators: for the upper and the lower threshold, respectively
  - RS-trigger.

An input signal sent to the submodule input goes through the scaling amplifier which determines one of the two threshold ranges depending on the jumper settings and is sent to the *bi-*

threshold diagram of input signal selection by level consisting of the upper and the lower threshold potentiometers and the RS- trigger. The RS-trigger output is an output of LTR51 module through which a binary function being the result of input signal calibration is sent to FPGA for logic processing.

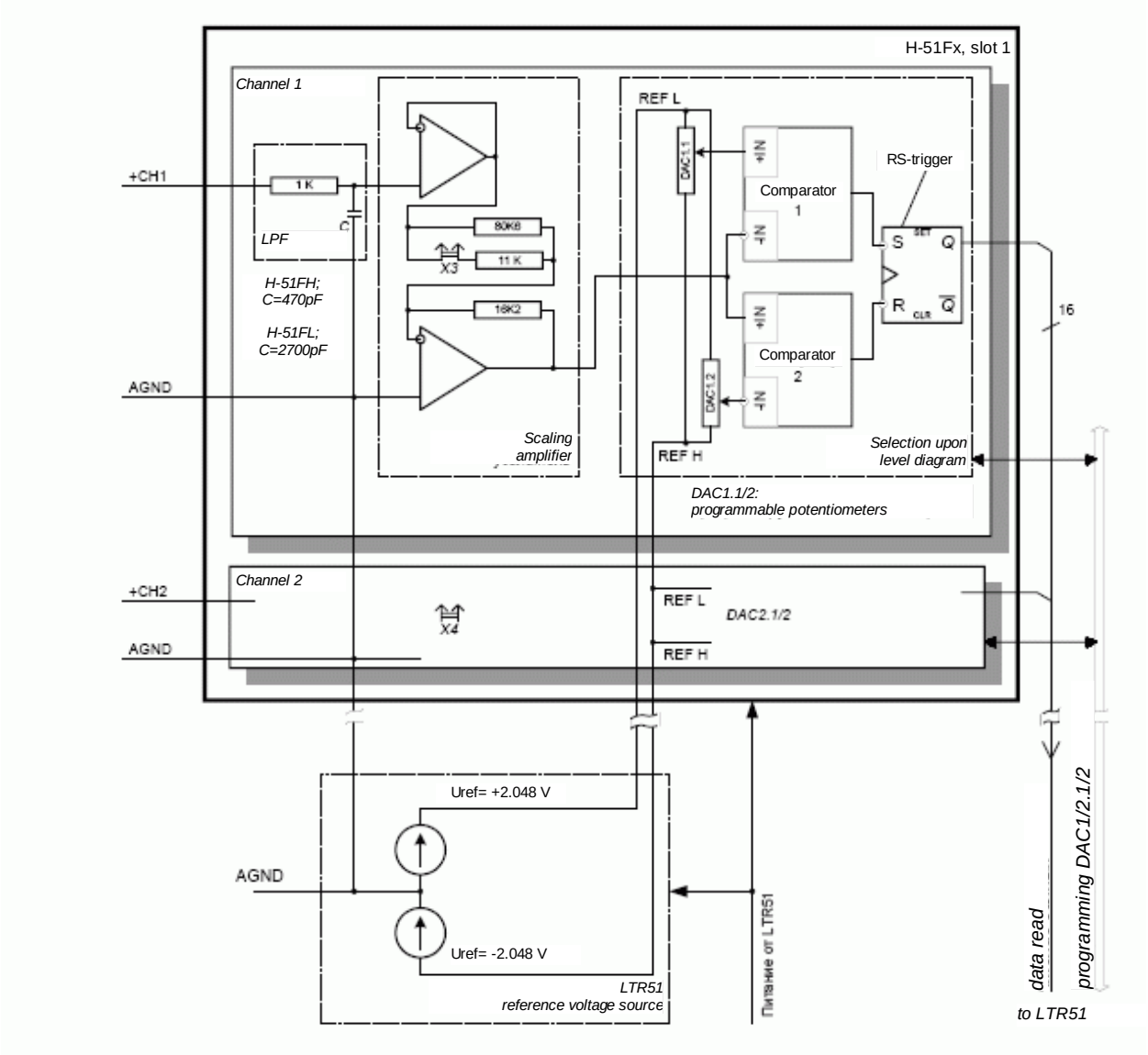


Fig.10-5. LTR51/LTR51x. LTR51x submodule block diagram

It should be considered that the estimated *threshold voltage level* is supplied to LTR51 input.

The upper frequency passband of the scaling amplifier depends on the type of submodule- H-51FH or H-51FL (paragraph 10.3.2, page 169) as well as on signal source resistance in case if it exceeds a few hundreds Ohm because in the input RC- filter (Fig. 10-5) a 1 kOhm resistance link is used, and the internal resistance of the signal source will be directly summed up with it and will shift the upper limit of frequency passband to the low-frequency area.

10.3.2 H-51Fx submodules specifications

Table10-2. H-51Fx submodule types and measuring ranges

Submodule	Number of channels	Application	Signal frequency range	Signal input voltage range
H-51FL	2	Low frequency meter	0…30 kHz	±10 V
H-51FH	2	Medium-high frequency meter	0…150 kHz	±10 V

Table10-3. Amplitude-frequency characteristic (AFC) reference points of H-51Fx submodules analog path

Submodule	F1, kHz	F2, kHz	F3, kHz
H-51FL	5.9	36.0	137.0
H-51FH	29.0	178.0	675.0

Amplitude-frequency characteristic (AFC) reference points of H51Fx submodules analog path are given in Table 10-3:

- F_1 is the cutoff frequency on level –0.09 dB (fall-off 1%)
- F_2 is the cutoff frequency on level –3.0 dB (fall-off 30%)
- F_3 is the cutoff frequency on level –20.0 dB (fall-off 90%)

10.3.3 LTR51 module control

10.3.3.1 Basic commands of LTR -interface in application to LTR51 module

The protocol of LTR modules is described in-paragraph 4.6.3, page 83 . Hardware-dependent part of this protocol in the context of LTR51 is detailed herein. The complete description of LTR51 commands is given in the document "LTR Crate System. Programmer's Manual"[1].

As well as for the rest modules, STOP, RESET, PROGR commands are purely hardware commands at which the micro controller in LTR51 module is passive. When the host computer sends the very first INSTR command, LTR51 switches-over to the *operating cycle* in which the micro controller is activated and implements all data collection and management processes in LTR51.

Then, by using the INSTR commands, the host computer loads the firmware to FPGA and records the desired settings into LTR51. All these functions are implemented via AVR of LTR51 module. The formats of corresponding commands are described in the *Programmer's Manual* [1] . To begin the data collecting, the host computer sends the corresponding command after the receipt of which the module AVR sends the start signal to FPGA. Then FPGA without any participation of AVR periodically sends measurement results in the form of **K** and **M** factors (their meaning is described in paragraph 10.3.4, page 170) sequentially for each channel.

It is significant that FPGA computes **K** and **M** in parallel and independently per channel and only measurement results are sequentially sent to the LTR interface.

K and M data packet formats are as follows:

M factor transmission data packet			
0	nnn0 CCCC	dddd dddd	dddd dddd
<24>	<23..16>	<15..8>	<7..0>

N factor transmission data packet			
0	nnn1 CCCC	dddd dddd	dddd dddd
<24>	<23..16>	<15..8>	<7..0>

Here, **nnn0CCCC**, **nnn1CCCC** *is* the control byte and **dddddddddddddddd** *is* 16-bit value of factor **M** or **N**, **nnn** *is* the value of sequence rolling counter incremented after transmitting every next data packet and cleared to zero after receipt of the RESET command.

To stop data collecting, the host computer issues the corresponding command after which the module AVR sends the stop signal to FPGA. Then FPGA firstly terminates the current cycle of data transmission from 16- channels and then stops data collecting.

! All settings in LTR51 module must be made when data collection is stopped.

10.3.4 Module operating principles

Input signals of each LTR51 channel come to inputs of corresponding LTR51Fx submodules. Having passed the passive RC- filters, the signals are routed to scaling amplifiers. Then the scaled analog signal is selected by level and converted into a digital (binary) signal which is an output signal for LTR51Fx submodule.

Bi-threshold diagrams for signal selection by H-51Fx submodule level have the upper and the lower reference voltage values U_{REFL} and U_{REFH} *WHICH ARE COMMON FOR BOTH CHANNELS AND* are supplied from LTR51. Programmable potentiometers *DAC1/2.1/2* of the level selection diagram can divide the range of voltages U_{REFL}…U_{REFH} into 256 programmable levels and generate upper and lower threshold voltages supplied to comparators.

In Fig. 10-6, the **hysteresis principle** is described in detail as the basis of operation of the diagram for frequency meter input signal selection by level: any input signal changes occurring between the *set threshold levels* without reaching them do not change the RS- trigger state; any (even short-time) input signal duration over-ranging causes stable shift of the RS -trigger state - which continues until the input signal *goes beyond the opposite* limit.

Digital signals dedicated at submodule outputs (in parallel from 16-channels) containing frequency information are entered to LTR51 FPGA with *sampling frequency*F_s. FPGA detects changes in the RS-trigger state in each channel. Sampling period *value* $\tau = 1/F_S$ determines *the time resolution* (sample unit) of LTR51 module and, respectively, its measurement limit and accuracy. F_S is- programmable frequency, the value of which is detemined according to the formula

$$F_s = \frac{2*10^7}{Ks} \qquad (10\text{-}1)$$

where, K_S *is* programmable dividing coefficient K_S = 40, 41, …, 65536.

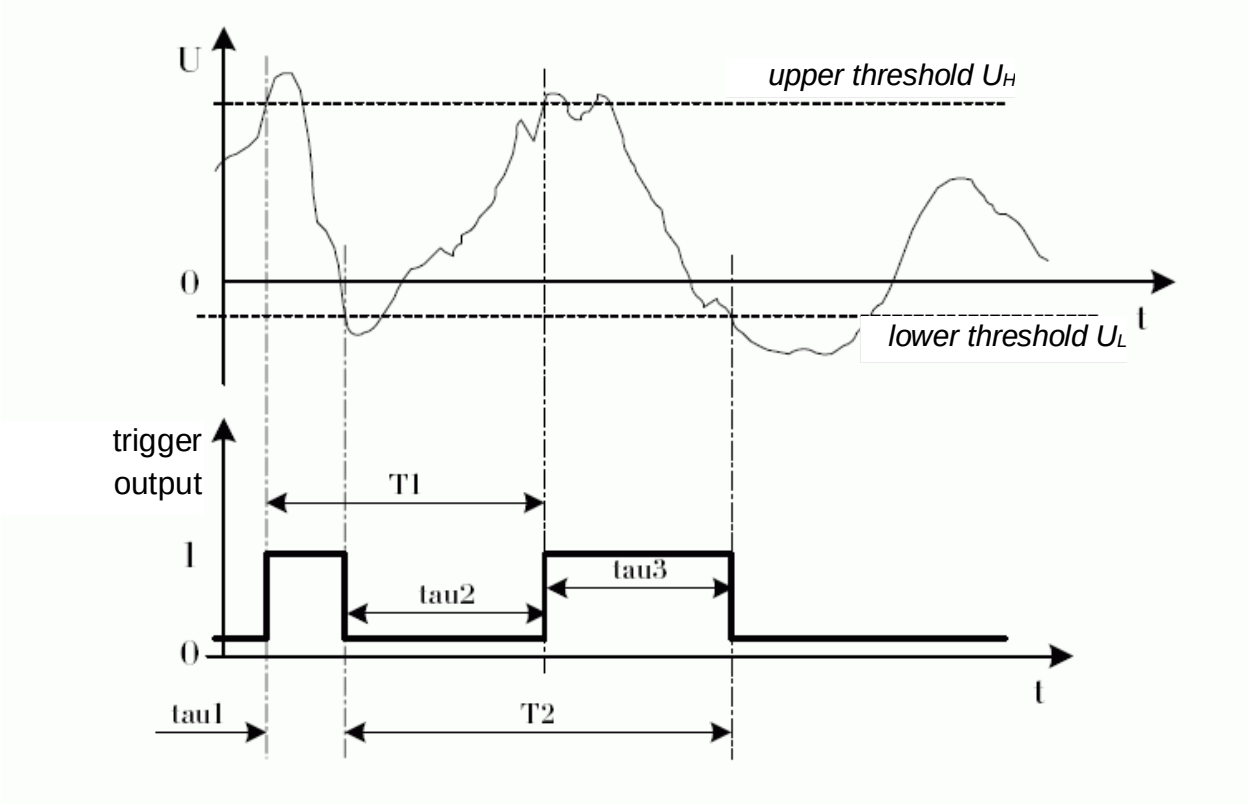


Fig.10-6. LTR-51/H-51x. The principle of selection by input signal level.

FPGA collects information about the signal in a fixed-duration time interval named *measurement period* T_{BASE} (see the note about the *measurement period).* Value T_{BASE} is user-programmable in units τ. Measuring frequency $F_{BASE} = 1/T_{BASE}$ is determined according to the formula

$$F_{BASE} = \frac{F_S}{BASE} \qquad (10\text{-}2)$$

where BASE = 70, 71, …, 65535.

In Fig. 10-7, a time diagram is shown where the principle of receiving intermediate data (flow of factors **M** and **N**) is explained. Pair of factors **M** and **N** are calculated by hardware in LTR51 for each *measuring period* T_{BASE} and are transmitted via the LTR interface to an upper-level program.

N is the number of *positive transitions* detected for a *measurement period*, **N** = 0, 1, 2, …, BASE

M is the period from the latest positive transition to the end of *the measurement period* expressed as the number of *sampling periods*, **M** = 1, 2, …, BASE.

A positive transition of input signal may have the form of *edge* or *fall* depending on the individual settings of the selected channel.

Special cases:

If there was no positive transition in the current measurement period (**N** = 0), LTR51 issues **M** = BASE.

M = BASE, **N** = 1 corresponds to a positive transition arrival in the last cycle of the previous measurement period with no positive transition in the current cycle.

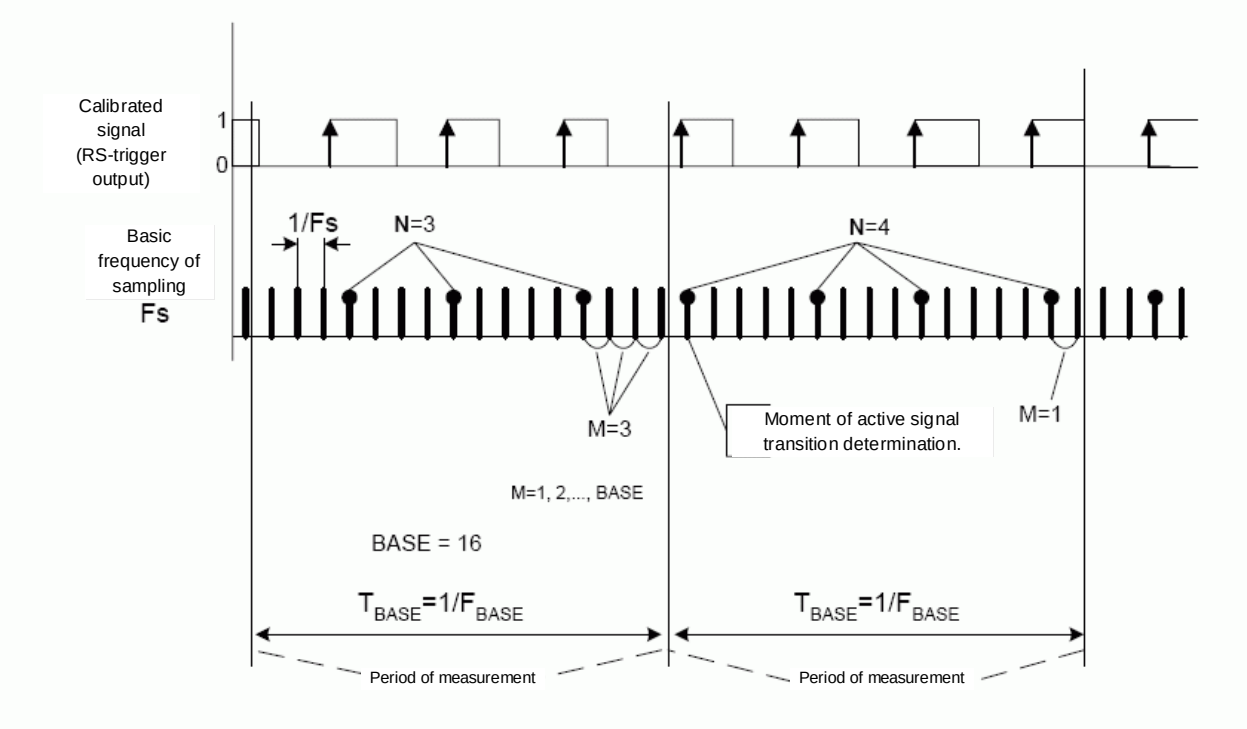


Fig.10-7. LTR51. Data acquisition process.

LTR51 generating the flow of pairs of factors **M** and **N** for each *measurement period together with* the upper-level program implement **continuous measuring mode** under which adjacent measurement periods are interfaced at the top level in time without breaks, and loss[1] of information on signal positive transitions is *prevented*.

Note on the term *"measurement period"*

! The concept of *measurement period* equal to the BASE sample introduced in this document means the period of determination of pairs of factors **M** and **N**. However, at the upper (user) level, *measurement period* can mean, for example, a frequency measurement period which can include more than one period with equal to the BASE sample.

Since LTR51module is a device similar in operation to H-51 module, you can refer to the theoretical description of the upper-level algorithms for counting frequencies in tthe H-51 section in the document "HB-16 Target Measuring Complex. User Manual[8]".

10.3.4.1 Proper setting conditions

The rules of proper setting of the frequency meter follow from the description of its operation principle (paragraph 10.3, page 173) . A failure to comply with these rules in every particular case may cause different errors in frequency meter readings or its malfunction. **Rules of proper setting of LTR51 frequency meter**:

Dead band of frequency meter between the upper and lower thresholds should fall within the range of input signal change levels with account for possible noise (i.e. with some reserve).

Frequency meter noise immunity is the higher the wider the dead band *is set by voltage level*

The lower threshold level should not be higher than the upper threshold level. Otherwise, the function of RS-trigger in the level selection diagram will be degenerated when input signal level is - between the prescribed thresholds that, certainly, will lead to *bounce* of the threshold device and additional errors in frequency measuring.

[1] under proper setting conditions considered below

AFC features of submodules H-51Fx, paragraph 10.3, page 174 should always be taken into account.

For periodic signal selected by level by the threshold device of LTR51, measurements of signal frequency exceeding $F_S/2$ kHz at the prescribed sampling frequency F_S kHz (max. 500 kHz) will be incorrect.

For aperiodic signal selected by level by the threshold device of LTR51, any peculiarities of the time diagram less than $(2/F_S)$ ms can be lost in the data acquisition process at the prescribed sampling frequency F_S kHz (max. 500 kHz) .

It is incorrect to apply voltage to the LTR51 input the level of which exceeds the operational input range of signals ± 10 V. For example, this condition can arise due to large noise interference on input signal.

For tasks of precision selection of input signal by level, it is reasonable to apply trial-and-error method in initial setting of the threshold level according to the actual input signal because the initial accuracy of threshold setting is significantly coarser than the device temperature drift in the actual temperature range (Appendix A.8, page 336)

For determination of the signal frequency value, it is necessary to ensure, as a minimum, such a number of adjacent measuring periods that at least one registered *positive edge* be present at the extreme periods.

10.4 Connection of signals

LTR51 module has 16 single-phase (with common ground) voltage inputs. The inputs have group galvanic isolation relative to all circuits of LTR- crate but the ground circuit (common wire) is common for 16 inputs.

In any case, shielded connection of input circuits is preferable.

If high-frequency submodule H-51FH is used, shielded connection is **critically preferable**.

If you apply consistent connection of input circuits (or low-resistance load of 50…600 Ohm), the maximum possible noise immunity will be ensured. In this case, the corresponding load resistors should be soldered in parallel to each input inside DB-37F connector mated with LTR51module. Such low-resistance load is extremely effective even if input cable is not shielded, but this measure can be applied only if the signal source provides such load, and resistors of relevant power are used.

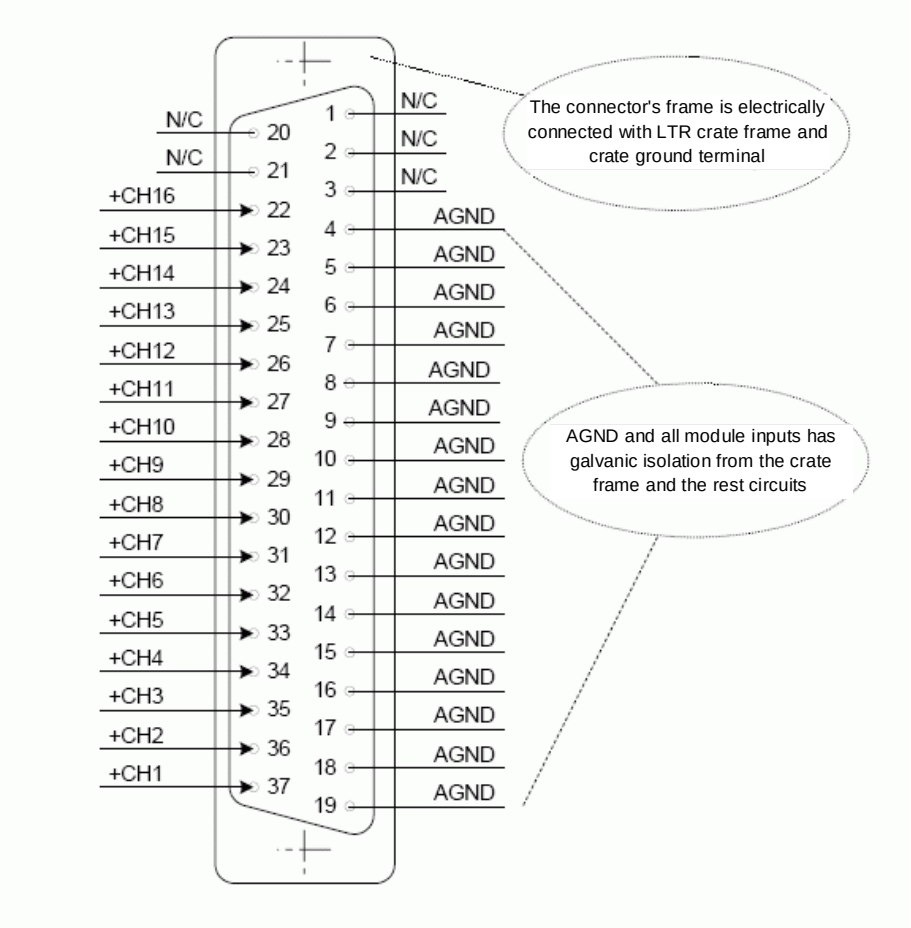


Fig.10-8. LTR51. Signal connector

10.4.1 Input signals connector

Table 10-4. LTR51. Assignment of connector signals

Signal name	Common point	Direction	Description
+CH<1...16>	AGND	Input	Input of measuring channel 1…16
AGND	-	-	Analog ground Common point for connection of input circuits of LTR51module
N/C	-	-	Not connected

Table10-5. LTR51. Correspondence of LTR51 channels to slots of H-51x submodules

Slot	Submodule channel	LTR51 physical channel
1	1	+CH1
1	2	+CH2
2	1	+CH3
2	2	+CH4
3	1	+CH5
3	2	+CH6

Slot	Submodule channel	LTR51 physical channel
4	1	+CH7
4	2	+CH8
5	1	+CH9
5	2	+CH10
6	1	+CH11
6	2	+CH12
7	1	+CH13
7	2	+CH14
8	1	+CH15
8	2	+CH16

Geometrical arrangement of H-51x submodule slots forming a mezzanine subsystem of H-51 module is shown in Fig.10-2.

10.4.2 Signal characteristics

The characteristics of galvanic isolation in LTR are given in Appendix A.12, page 167.

Table10-6. LTR51. Input characteristics. Switched-on condition

Signal	Type	Input impedance	Maximum permissible value at input
+CH<1…16>	Analog input	more than 100 kOhm[1]	±18 V relative to AGND

Table10-7. LTR51. Input characteristics. Switched-off condition

Signal	Type	Input impedance	Maximum permissible value at input
+CH<1…16>	Analog input	min. 1 kOhm	±15 V relative to AGND

[1] at DC input voltage; with increase of input frequency, input impedance decreases and is equal to several kOhm at the passband limit.

Chapter 11. LTR22 ADC module

11.1 General description of LTR22

Fig.11-1. LTR22 view

11.1.1 Device application

LTR22 ADC module is designed for creation of multichannel data acquisition systems at production companies and laboratories. Main areas of LTR22 application: **audio processing, vibrometry, phasemetry** and other applications connected with digitizing of signals within the audio-frequency range where high spectrometic accuracy of signal variable component digitizing is critical.

11.1.2 General information about LTR22

- LTR22 has 4 sigma-delta ADC channels
- Each channel of LTR22 has **a high-quality differential high-resistance input with high common mode rejection.**
- **The required input voltage subrange is set in software individually for each channel from the following** range: ±10 V, ±3 V, ±1 V, ±0.3 V, ±0.1 V, ±0.03 V . It is noteworthy that the common-mode signal *range* is ±10 V in any of these subranges.
- For these four channels, either the signal constant component **compensation mode (AC mode)or** normal mode **without compensation** (DC+AC mode) is set in software simultaneously. In the AC mode, the lower AFC limit is about 0.7 Hz at 3 dB level. The AC mode is used for digitizing of the lower variable component of input signal at a relatively high constant component (up to ±10 V in all subranges).

- For the four channels, the capability to measure **own zero** of LTR22 is set in software simultaneously that allows, if necessary, for compensating relatively large temperature drift of sigma-delta ADC[1].
- **ADC frequency spectrum** in Hertz (for 4 -channels, the same frequencies are set): 3472; 3720; 4006; 4340; 4735; 5208; 5580; 5787; 6010; 6510; 7102; 7440; 7812,5; 8681; 9766; 10417; 11161; 13021; 13021; 15625; 17361; 19531; 26042; 26042; 39062,5; 52083; 78125. Precise values of these frequencies are determined according to the formula(11-1).
- **Built-in digital anti-aliasing filters** with upper AFC cut-off frequency set at the level of half ADC specified frequency.
- Program-accessible logic **signs of LTR22 ADC word size overflow** by the input signal are transmitted for each ADC sample individually for each channel.
- LTR22 is functionally similar to H-22[2] but LTR22 does not have RS-485 charge amplifier control interface because in LTR, RS-485 is a part of LTR43 module (paragraph 8.1, page 143)
- In LTR22, all 4 channels of one LTR22 module are synchronous and have no relative phase shift [3]
- Within one LTR crate, relative phase shift of data acquisition between LTR22 modules will always be constant in time because the the source of ADC reference frequency is the *single reference generator of LTR crate*
- **Synchronization signal input** SYN_IN for sending a common synchronization signal to several LTR22 modules allows for phasing of internal data collection pipelines [4]in ADC as well as for synchronizing the events of data output to LTR interface. For example, in one LTR-U-16 crate up to 64 channels of synchronous data collection can be arranged.
- **Synchronization signal output** SYN_OUT allows for:
  - implementing a synchronization circuit several LTR22 modules based on the "master-slave" principle. In this case, one "master" module will send a synchronization signal - from SYN_OUT output for itself and for the rest "slave" modules;
  - monitoring ADC frequency and phase of each LTR22 module, if required.
- It is assumed that the operation of data correction with account for calibration factors using the line correction method is performed by user computer (library functions are provided).
- Each data sample format has a sign of the instantaneous value of the signal reaching the limit of the ADC word size which allows for recording events of ADC overload separately for each channel.
- Each data sample format contains the information about the channel number and subrange of input voltage set for this channel.
- **Signals at LTR22 user connector are galvanically isolated** from the ground (frame) of LTR crate and from other LTR modules (signals are not galvanically isolated from each other).

11.1.3 LTR22 module configuration

The basic configuration of LTR22 is described in paragraph2.4, page29.

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[1] this is a relative disadvantage of audio sigma-delta ADC relative to, for example, progressive approximation ADC.

[2] crate system H-2000

[3] for comparison: H-22 had phase shift for a quarter of ADC frequency period between pairs of channels

[4] sigma-delta ADC has a deep pipelined architecture

11.2 Installation and set-up

During LTR22 installation in crate, observe the module installation rules common for LTR system, see paragraph 3.6.2.2, page.52

LTR22 board has one process 6-pin connector. **Do not put jumpers on process connectors and make any external connections to them!**

11.3 Overview of LTR22 hardware components and operation principles

11.3.1 Block diagram

The block diagram of LTR22 hardware engaged in data collection is shown in Fig.11-2 .

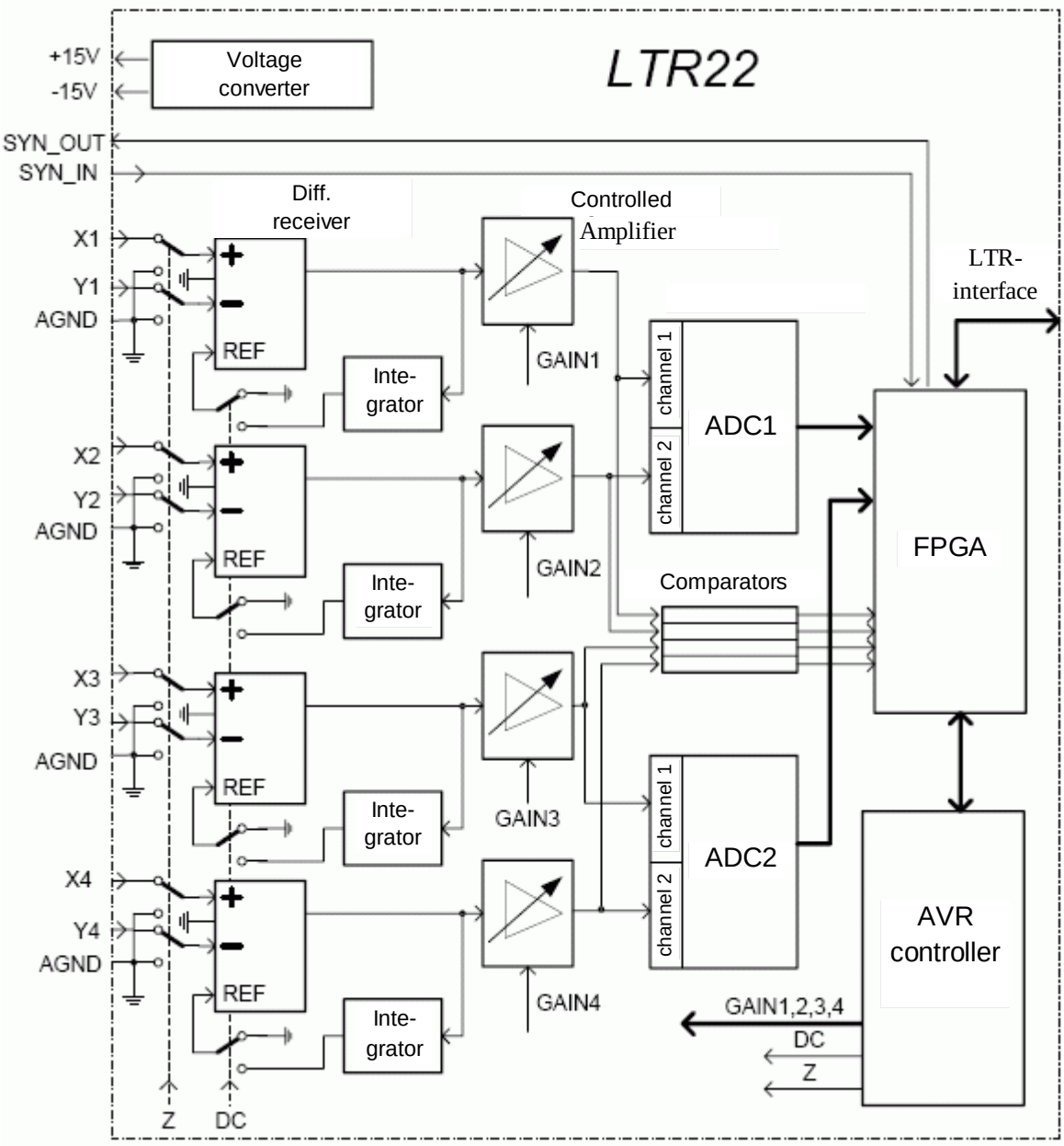


Fig.11-2. LTR22. Block diagram

LTR22 module has four identical signal processing channels. Input signal of i- channel is sent to the differential input – signals X_i, Y_i relative to AGND (for signal connection issues, see paragraph 11.4, page 179).

According to the classification given in [2], analog inputs of LTR22 are differential, *bipolar voltage inputs with group galvanic isolation*.

Differential input signal of each channel goes through a *static switch* to a high-quality differential receiver ensuring high common mode rejection. *Input switch*(signal *Z*) controlled by AVR micro controller is only used for a special mode of measuring own input offset voltage and can be installed prior to the simultaneous data acquisition for 4- channels. *It is essential that the input switch is not used in the dynamic mode and thus does not create switching noise.*

DC signal can be sent by software from *AVR* to switch the feedback of differential receivers for all 4-channels simultaneously: thus, in the special *mode of AC compensation of signal constant* component, the integrator is connected into the feedback circuit of the differential receiver, and in the *DC+AC* mode, the differential receiver reference voltage input is connected to the AGND circuit and no compensation occurs which corresponds to the normal operating mode.

The signal comes from the *differential receiver* output to the *controlled amplifier of the respective* channel with individual amplifier gain control performed by the micro controller ($GAIN_i$ signals). Thus, six input signal subranges are implemented in each channel.

The scaled signal *is fed to AD1870 ADC inputs* from controlled amplifier outputs. The four ADC channels digitize signals received from *controlled amplifier outputs of* the respective channel. There is a digital anti-aliasing filter in the internal architecture of *ADC channel which* blocks frequency components of input signal exceeding half of ADC sampling frequency and ensures thereby high spectral transformation fidelity required for such class of ADC.

It is important that all channels can operate at single programmed frequency only.

ADC frequency spectrum from 3472 Hz to 78125 Hz is created by division of the reference frequency of *the single reference frequency generator of* LTR- crate (Appendix A.16, page. 359) by the product of counting numbers according to formula:

$$F_{ADC} = \frac{2*10^7}{128*n*k} \qquad \textbf{(11-1)}$$

where n = 1, 2, …, 15; k = 2, 3

Each channel of AD1870 ADC chip has an amplitude-frequency response characteristic of the input digital filter shown in Fig. 11-3[1].

[1] according to *Analog Devices*

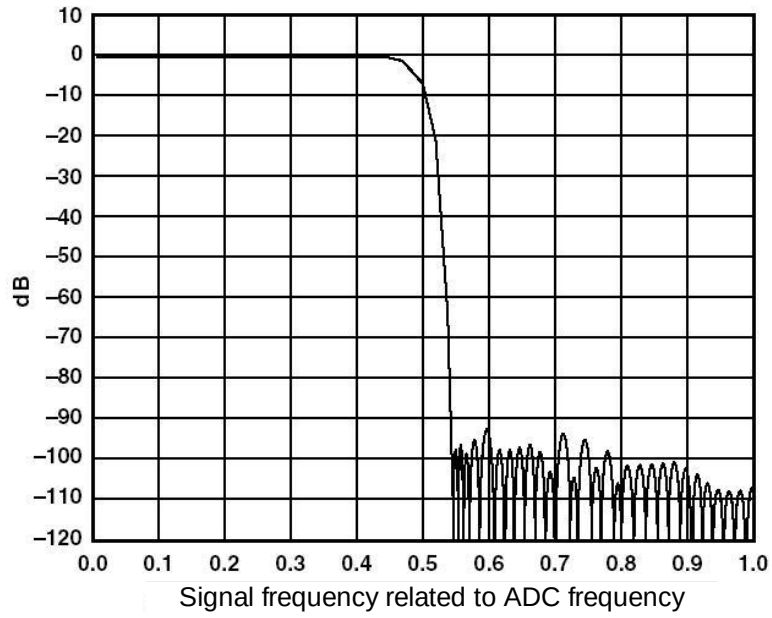


Fig.11-3. LTR22. AFC of digital filter in ADC AD1870.

The task of packaging digital data samples from 4-ADC channels into data packets of the *LTR-interface*(paragraph 11.3.2.1, page 181) is performed by FPGA without AVR engagement.

It is significant that in LTR22 you can disable by software the data output from any unused channels with decreasing the total speed of data transmission via LTR crate.

Dual-threshold *comparators* compare values of signal voltage fed to AD1870 input to cut-off reference voltages of the input range of this ADC. Logic signals of *ADC word size overflow* which are individual for each channel are fed to FPGA from the comparators output. FPGA inserts these signs in each *data packet* and they are program-accessible for the user. To learn more about the overflow signs, see paragraph 11.3.1.1, page 181.

It should be noted that the time of data delay τ_d from the time of ADC sampling till output to LTR-crate depends on ADC set frequency F_{ADC} and is calculated according to the formula:

$$\tau_d \approx \frac{37}{F_{ADC}} \qquad (11\text{-}1)$$

Like in the rest of LTR- modules, the LTR22 initialization process is run in accordance with the permitted command sequence graph (paragraph 4.6.3, page 83 and Fig. Fig. 4-10, page 89). In LTR22, common reset signal for both AD1870 ADCs is set by the RESET command and clyared by the STOP command. At the moment of clearing of AD1870 ADC reset signal, phases of input sigma-delta converters inside AD1870 are synchronized, after which the internal autocalibrating process of AD1870 starts and lasts for τ_k

$$\tau_k = \frac{8192}{F_{ADC}} \qquad (11\text{-}2)$$

and further start of data output to LTR-crate will be performed together with the pre-synchronized pair of bi-channel ADCs.

! Unlike progressive approximation chips in ADC (see LTR11), it is impossible to start data collection in pipelined sigma-delta ADCs simultaneously, therefore, ADCs in LTR22 are started after the module energizing, and the data stream is controlled by permitting the data output to LTR- crate.

In the course of multi-module sinchronization (paragraph 11.3.1.4, page 182) the reset signal of AD1870 ADC in different LTR modules is synchronized from an external signal sent to the SYNC_IN input.

11.3.1.1 Meaning and logic of signs of ADC word size overflow

LTR22 has program-accessible signs of ADC word size overflow for each channel (paragraph 11.3.2.1, page 182). The purpose of these signs is to indicate an event when the peak value of AD1870 ADC input signal approaches one of the ADC word size overflow limits (the upper and lower limits do not differ). Such information is required in such data collection applications where signal contains impulse components able to overflow the input range and, hence, internal arithmetic of the sigma-delta ADC. If overflow signs were not analyzed, then such impulse actions on ADC would lead to distortion of digitized signal seemingly unexplainable for the user.

If an overflow sign is identified in the corresponding channel, this literally means that - "active data section distorionless digitizing is not assured" because the signal peak value is near to the ADC word size limit.

It should be noted that ADC codes range corresponding to the selected input signal subrange including calibration factors (paragraph 11.3.1.2, page 182), is always narrower than the clean range of ADC codes. For this reason, there can be no overflow sign when a signal has exceeded the input signal subrange but has not yet crossed the ADC word size overflow operating limit.

The logic of overflow signs is as follows:

- Overflow signs in a stream of data packets (paragraph 11.3.2.1, page 182) are always in advance of coresponding samples for the time τ_d, because ADC samples are produced from LTR22 with a pipeline delay equal to τ_d, and overflow signs are inserted into the data stream without delay.
- Even if duration of the impulse in an input signal which has caused the overflow is short relative to the ADC frequency period, the overflow sign will always be present in at least one data packet sent from LTR22.
- The overflow sign will be present in the data packet until the overflow cause exists. The sign will disappear when the overflow cause is eliminated.

11.3.1.2 Calibration principle used in LTR22

A pair of calibration factors is recorded separately for each channel and for each input signal range into the flash-memory of LTR22 AVR module by the manufacturer. Calibration factors which are "read only" for the user are provided for linear data correction in the user program ensuring the claimed accuracy of DC measurement (Appendix A.9, page 337).

11.3.1.3 Phase delay in LTR22

As was stated above, LTR22 can be used for multichannel phasemetry purposes. For such applications:

- in LTR22, relative phase delay between any channels of the same module in the DC+AC mode is almost equal to zero[1].
- *In the AC mode, an additional phase dispersion* occurs between channels of the same LTR22 module due to approaching the lower AFC cutoff frequency limit.
- For extra accurate measuring of phase difference, it should be taken into account that an additional insignificant phase dispersion occurs at frequencies of tens kilohertz between

[1] The typical error of phase difference between channels of the same LTR22 module in the DC+AC mode at a frequency of 10 kHz measured by L-Card makes 0.03° and for frequencies of hundreds kilohertz it makes thousandths of degree.

channels of the same LTR22 module which are set for different input voltage ranges in the AC or DC+AC mode.

! The smallest phase delay dispersion in channels of the same LTR22 can be achieved in the DC+AC mode at the same set input voltage subranges.

- A small minimum relative phase delay can only be achieved *between LTR22 modules* - when different LTR22 modules are integrated by SYNC_IN inputs into a common synchronization circuit and *ADC phasing operation is carried out prior to the* start of data acquisition at the receipt of a synchronization signal at SYNC_IN and then data acquisition is started synchronously in response to the repeated synchronization resignal at SYNC_IN. For more detail on LTR22 multimodule synchronization, see paragraph 11.3.1.4, page 183.

11.3.1.4 LTR22 multimodule synchronization

The deep pipeline architecture of AD1870 ADC requires that data acquisition processes of different LTR22 modules be synchronized in two steps:

1) **ADC synchronization:** synchronization of input AD1870 sigma-delta converter phases in different LTR22 modules. According to the formula(11-2), this process lasts for a significant amount of time and, therefore, must be performed as a separate step.

2) **Synchronization of the start of data output to LTR interface.** Naturally, each data collection channel in LTR at the upper software level has independent buffering and in case of synchronous start of data output the time scale is referenced to the start of the data stream of each LTR22 channel. In addition, according to the formula (11-1), the 38-th data sample from the beginning of data stream corresponds to the synchronization start moment , and 37 first samples will contain the historical data.

Options of sending a single synchronization signal to SYN_IN inputs in multi-module connections of LTR22 are presented in Fig. 11-8. If necessary, one LTR22 can be designated as the master unit by using its SYN_OUT output for synchronization signal sending. This diagram provides for connection of up to 16 LTR22 modules within one 16-slot- LTR crate.

Any TTL-signal source may be designated as the master unit as well, including LTR43 module.

In LTR22 inter-crate synchronization option, frequency difference between generators of different crates should be taken into account (see the parameters in Appendix A.16, page 359).

In accordance with the above synchronization principle, **an individual LTR22 module has the following program procedures related to the start of data acquisition process:**

- Asynchronous start of data output to LTR- crate (in this case, channels of this particular LTR22 module are synchronized only).
- ADC synchronization at an external synchronization signal at SYN_IN input (LTR22 is in the "slave" mode)
- ADC synchronization at an external synchronization signal with an option for generation of a synchronization impulse at the SYN_OUT output (LTR22 is in the "master" mode)
- Synchronous start of data output at an external synchronization signal at the SYN_IN input (LTR22 is in the "slave" mode)
- Synchronous start of data output at an external synchronization signal with an option for generation of a synchronization impulse at the SYN_OUT output (LTR22 is in the "master" mode)

Physically, synchronization at the SIN_IN input is**TTL** edge-triggered. The initial state at the TTL-output SYN_OUT in the "master" mode *is* active zero and Z-state in the "slave" mode (with

pull-up resistor to zero). Synchronization pulse duration at the SYN_OUT output in the "slave" mode *is* several microseconds. See the characteristics of LTR22 signals in paragraph 11.4.

Note: SYN_IN and SYN_OUT synchronization signals are in principle compatible with synchronization signals of other LTR modules, in particular, LTR41, LTR42, LTR43. This allows for creating other inter-module synchronization options.

11.3.2 LTR22 module control

11.3.2.1 Basic commands of LTR- interface in application to LTR22 module

The protocol of LTR- modules is described in paragraph 4.6,page 82. Hardware-dependent part of this protocol in the context of LTR22 is detailed herein. Complete description of LTR22 commands is given in the document *"LTR Crate System. Programmer's Manual"*[1] .

As well as for the rest modules, STOP, RESET, PROGR commands are purely hardware commands at which the micro controller in LTR22 module is passive. When host-computer sends the very first INSTR command, LTR22 switches-over to the *operating cycle in which the* micro controller is activated and implements all data collection and management processes in LTR22.

Since LTR22 *is* ADC, it does not support data stream to output and *DATA data packets may not be sent to LTR22*.

Let us consider in details the DATA data packet format in the context of LTR22 module.

LTR22 ADC data packet			
0	**NNNV VVCC**	**sddd dddd**	**dddd dddd**
<24>	<23..16>	<15..8>	<7..0>

Where **NNNVVVCC** is the control byte and **sddddddddddddddd** *is* a 16-bit ADC sample in additional code with **"s"** character.

In **NNNVVVCC** control byte, the fields are interpreted as follows:

- **NNN***is* ADC sequence rolling sample counter value;
- **CC***is* channel number code;
- **VVV***is* the field of range and ADC word size overflow sign:
  - 0 – subrange ±1 V
  - 1 – subrange ±0.3 V
  - 2 – subrange ±0.1 V
  - 3 – subrange ±0.03 V
  - 4 – subrange ±10 V
  - 5 – subrange ±3 V
  - 6 *is* a reserved value
  - 7 *is* ADC word size overflow state in this channel.

If there is no ADC word size overflow, bit field **VVV** codes the defined range in this ADC channel. Otherwise, the overflow state is indicated (see paragraph 11.3.1.1).

LTR22 hardware assigns zero value to the sequence ADC rolling sample counter when the module is initialized by the RESET command. The counter is incremented every time when DATA packet is sent from LTR.

11.4 Connection of signals

Read the general rules of signals connection in paragraph3.6.6 , page . 58

LTR22 module has DRB-37M panel-mount connector for connection of input signals. External connections to LTR22 should be implemented by connecting signal circuits to the cable part of the connector (DB-37F type). Application of signals is given in Table11-1, and the view of the panel-mounted connector is presented in Fig.11-4 .

Table11-1. Application of LTR22 user connector signals

Signal name	Common point	Direc-tion	Description
AGND	–	–	Analog ground
X1, X2, X3, X4	AGND	Input	– Uninverting voltage input of channels 1…4 – Operating voltage range: ±10 V
Y1, Y2, Y3, Y4	AGND	Input	– Inverting voltage input of channels 1…4 – Operating voltage range: ±10 V
SYN_IN	AGND	Input	LTR22 synchronization input. Compatible with output logic level TTL/CMOS-of elements with power voltageof 3.3V/+5 V. If it is not required to use the external synchronization input, it can be left unconnected. The input has a 20 kOhm pull-up resistor to the AGND circuit
SYN_OUT	AGND	Output	LTR22 synchronization output. Has output logic level LVTTL-of elements with power voltage of +3.3 V, "by default" is in Z-state with a kOhm pull-up resistor to the AGND circuit.
n/c	–	–	The contact is not connected

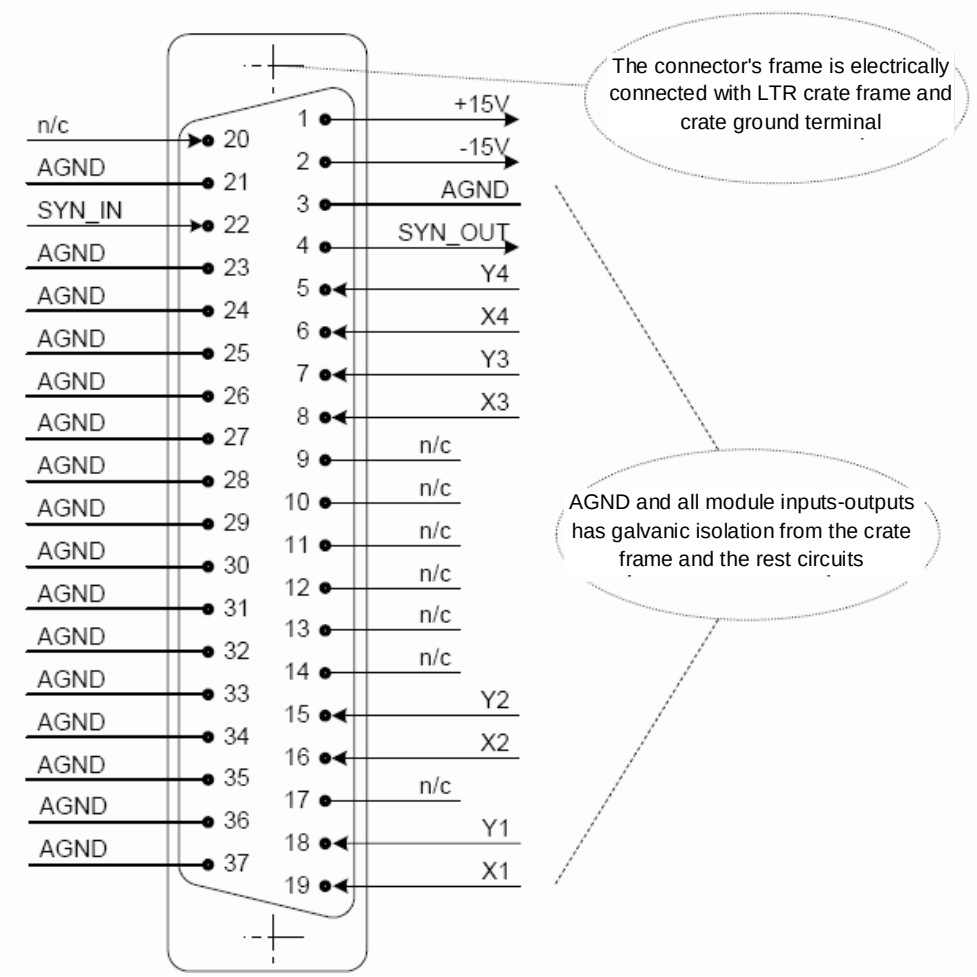


Fig.11-4. Input signals at LTR22 module connector

11.4.1 Characteristics of signal line inputs and outputs

When connecting LTR22 module to your system, strictly observe the parameters specified in tables of this section.

The manufacturer shall not be warranty liable for LTR22 failure caused by violation of maximum permissible operation conditions.

The following symbols are given in tables of this section:

AI is analog input,

DI is digital input,

DOZ is digital output with the *third state*,

P is external device power output.

Note that impedance of *input lines is greater in the* LTR22 operating mode than in the switched-off *module state*. See information about the *switched-off module state* in section4.8.

The characteristics of galvanic isolation in LTR are given in Appendix A.18.

11.4.2 LTR22 operating mode

LTR22 module installed in LTR crate has the following characteristics of input and output signal lines after LTR crate is powered on:

Table11-2. Maximum permissible conditions, LTR22 module is switched-on.

Signal	Type	Input impedance	Maximum permissible conditions	Pull-up resistor
X1, X2, X3, X4, Y1, Y2, Y3, Y4	AI	– More than 10 MOhm	±20 V relative to AGND, ±27 V – in short-time mode (1 s)	
SYN_IN	DI	20 kOhm	-0.5…+5.2 V relative to AGND	20 kOhm to zero
SYN_OUT	DOZ		Output current ±20 mA	20 kOhm to zero
+15 V, -15 V	P		Load current of 50 mA relativeto AGND foreach output in the continuous operation mode. Typical short circuit - current of 320 mA is permissible for max. 1 second	

No certainty of the state of the unconnected inputs X1, X2, X3, X4, Y1, Y2, Y3, Y4 is guaranteed.

The potential at unconnected high-resistance inputs is determined by nano-ampere leakage-currents which may be different in different modules.

11.4.3 LTR switched-off state

See *information about the* switched-off module state in section4.8.

In this mode, LTR22 module is de-energized and impedance of analog and digital input lines is low in comparison with the operating mode

Table11-3. Maximum permissible conditions, LTR22 module is switched-off.

Signal	Type	Input impedance	Maximum permissible conditions
X1, X2, X3, X4, Y1, Y2, Y3, Y4	AI	min. 1 kOhm	±20 V relative to AGND, ±27 V in the short-time mode (1 s)
SYN_IN	DI	min. 1 kOhm	-0.5…+5.2 V relative to AGND
SYN_OUT	DOZ	–	-0.5…+5.2 V relative to AGND at current max. 20 mA
+15 V, -15 V	P	–	–

11.4.4 Internal protection circuit of ADC inputs.

In LTR22, analog inputs X and Y have an internal protection circuit shown in the figure below. These inputs are high-resistance in the operation mode when input voltage does not achieve the threshold value of ±12 V at input X or Y. When voltage exceeds the threshold of ±12 V, input resistance drops to 1 kOhm because an internal diode signal limiting circuit comes into operation.

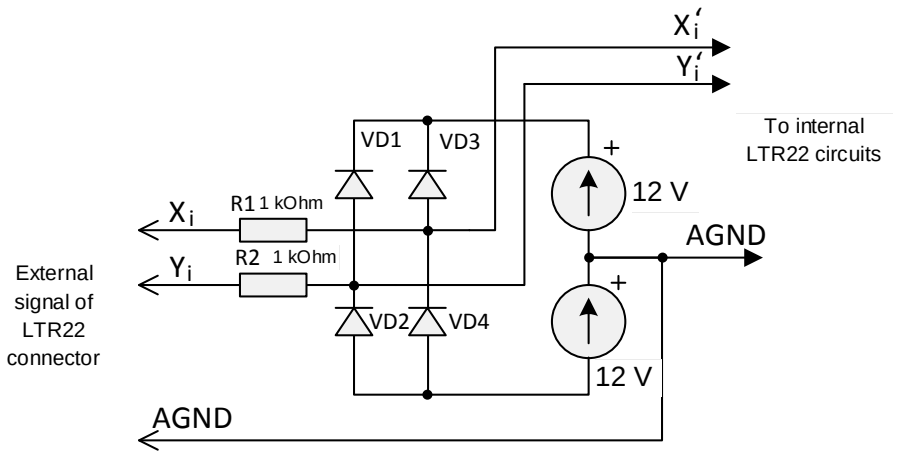


Fig.11-5. LTR22. Equivalent input protection circuit.

This feature of LTR22 inputs should be taken into account if LTR22 signal input range can potentially be exceeded in your connections.

11.4.5 Equivalent electric diagram of ADC input circuit.

The issue of LTR22 input impact on a measuring circuit arises for applications providing for signals measuring in high-resistance circuits and at relatively high frequencies. To evaluate this impact, consider an equivalent electric diagram of input circuits for LTR22 *operation mode*.

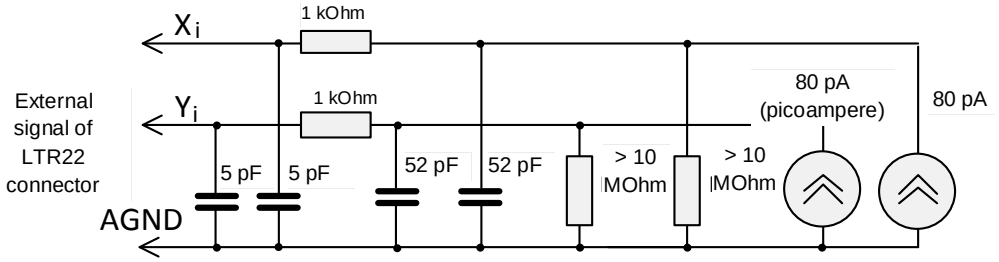
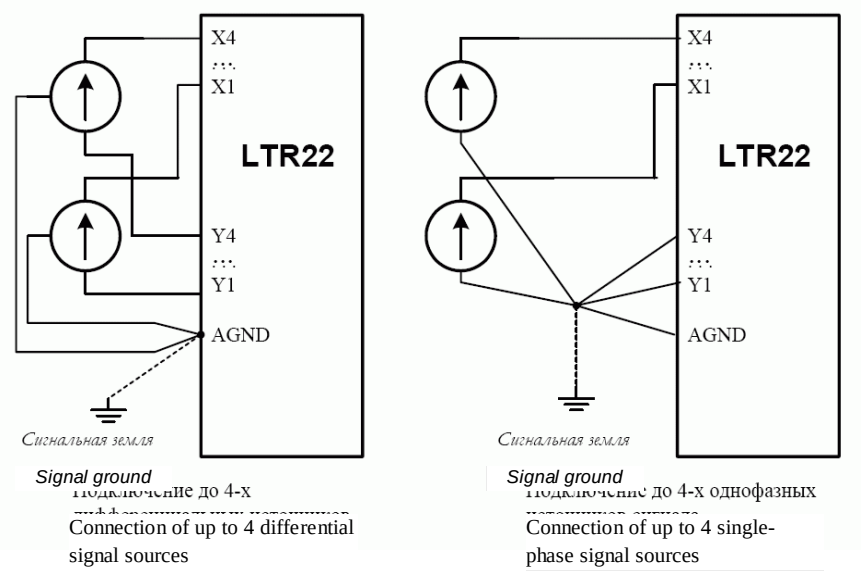


Fig.11-6. LTR22. Equivalent electric diagram of input circuits.

Note: All parameters of this equivalent diagram are obtained by calculation using *typical values* of characteristics of applied electronic components specified in their documentation, for normal measuring conditions of LTR22. Current sources used in the diagram are own input current of LTR22 differential receiver unit (fig.11-2, page 179). The direction of this current direction is not regulated and is shown conventionally.

11.4.6 Examples of input signal connections

Two most typical connection diagrams for input analog signals are given in Fig. **Ошибка! Источник ссылки не найден.**[1]. Combined variants of differential and single-phase source connections are also possible.



Connection of up to 4 differential signal sources

Connection of up to 4 single-phase signal sources

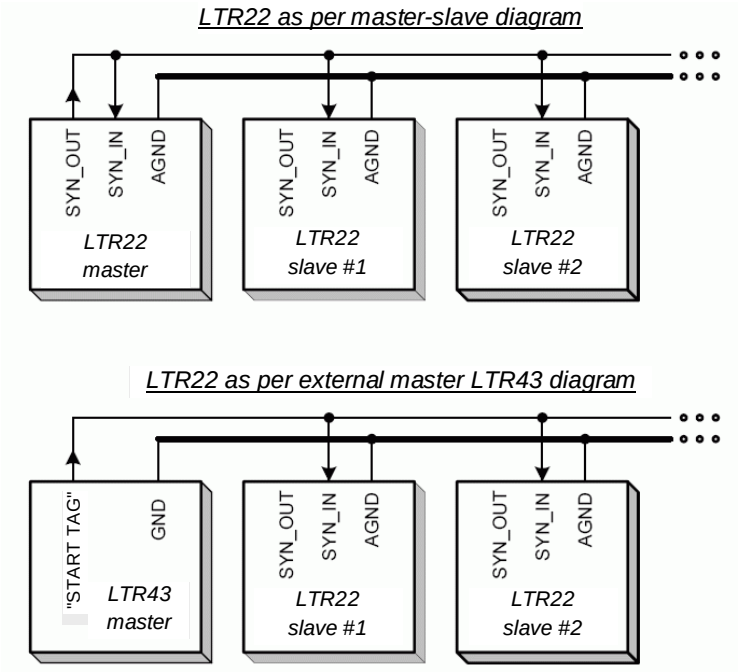
Fig.11-7. Signal sources connections to LTR22

If it is required to change the converted signal polarity relative to the physically issued signal, the connection of circuits X and Y should be changed in the corresponding channel.

Examples of synchronization line connections in multi-module configurations are shown in Fig. 11-8, page 190.

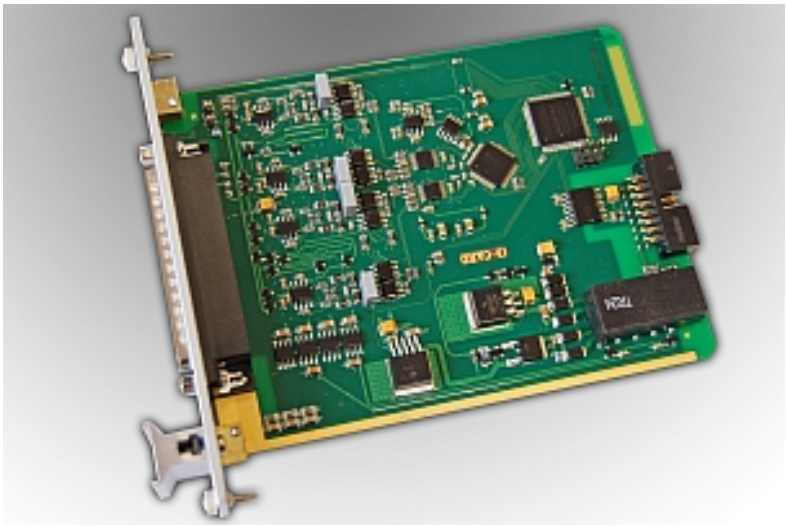
[1] The issues on measuring units connecting are described in detail in the article [2]

Fig.11-8. Connections in case of LTR22 multi-module synchronization



Chapter 12. LTR24 ADC module

12.1 General description of LTR24



12.1.1 Device application

LTR24 is a 4-channel sigma-delta ADC with parallel independent channels (without channels switching). LTR24 is intended for using in different audio applications requiring high-quality digitalization of an alternating signal with high spectral fidelity of conversion, wide dynamic range and a large signal-to-noise ratio. In its class, LTR24 sigma-delta ADC is distinguished by high accuracy of direct current voltage measurement. Main areas of LTR24 application: **vibrometry, phasemetry, acoustics, seismometry, audio processing**[1]**, general-purpose laboratory ADC for researching physical processes.**

It can be said that LTR24 outperforms its predecessor LTR22 in the most important technical characteristics, is comparable to LTR11 in direct current accuracy, and outclasses LTR11 in terms of resolution capability.

LTR24-2 modification has additional inputs for connection of ICP-sensors and an option for connection of single resistance strain gauges into a 4-wire circuit for both tensometry and vibrometry applications (resistance variable component measurement).

[1] LTR24 does not support standard audio-conversion frequencies.

12.1.2 LTR24-1 and LTR24-2 modifications.

After the release of the first batches of the product marked “LTR24”, a decision was made on further introduction of LTR24-1 and LTR24-2 modifications. Differences between the modifications are described in the table below:

Modification	Differences
LTR24	LTR24 connector pins are partially compatible with LTR22 in AGND circuits. This modification has been discontinued since April, 2013. In the future, LTR24-1 and LTR42-2 modifications will be released only.
LTR24-1	LTR24-1 connector pins are fully compatible with LTR22. In other characteristics and properties, LTR24-1 and LTR24 modifications are equivalent.
LTR24-2	Connector pins are fully compatible with LTR22, dead (unconnected) pins are used for additional functions. As compared to LTR24-1 and LTR24, LTR24-2 modification has 4 additional inputs for connection of ICP -sensors and an option for connection of single resistance strain gauges into a 4-wire circuit.

! Hereinafter in this manual a reference to "LTR24" include all its modifications at once, unless module modifications are the case: LTR24, LTR24-1, LTR24-2.

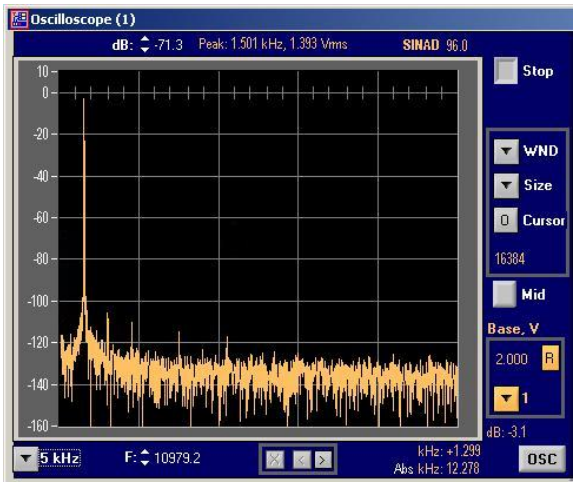
12.1.3 General information about LTR24

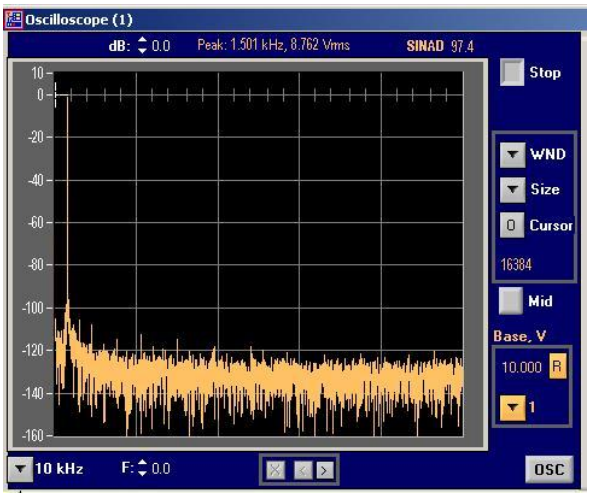
- LTR24 contains 4 channels of sigma-delta ADC of 24-bit width.
- Each channel of LTR24 **has a high-quality differential high-resistance input with high common mode rejection.**
- LTR24-2 modification has 4 additional inputs for connection of ICP-sensors or resistance strain gauges. The input of each of 4 channels in LTR24-2 can be independently configured by software for measuring signals from a differential input or ICP-sensor.
- LTR24-2 has 4 2.86 mA or 10 mA sources of stable current for power supply to 4 resistance strain gauges. 2.86 mA or 10 mA current is set for the 4 current sources simultaneously.
- LTR24-2 modification has a special mode for short circuit or breakage identification in the ICP-sensor circuit (simultaneously in the four channels).
- **The required input voltage subrange is set in software individually for each channel**: “±10V”, “±2 V” for the differential input and “~5 V”, “~1 V” for the ICP input. The common-mode *signal range is ±10 V* in any of these subranges.
- Separately for each **channel, either the signal constant component compensation mode (AC mode) or** normal mode **without compensation** (DC+AC mode) is set in software. In the AC mode, the lower AFC limit is about 0.48 Hz at 3 dB level. The AC mode is used, as a rule, for digitizing of the lower variable component of input signal at a relatively high constant component (p.12.3.9).
- **The capability to measure own zero shift of LTR24 differential input** is set in software simultaneously for four channels, which allows, if required, for compensating the residual ADC zero shift immediately prior to measuring.
- **ADC frequency spectrum** in Hertz (for 4-channels, the same frequencies are set): 117188; 78125; 58594; 39063; 29297; 19531; 14648; 9766; 7324; 4883; 3662; 2441; 1831; 1221; 916; 610. ADC conversion frequencies are obtained by dividing the frequency of the single reference generator of LTR crate. LTR24 has a limitation on capability to set the 24-bit data format due to the interface bandwidth limitations for some upper conversion frequencies depending on the number of channels used. However, the 20-bit data format can be set without any restrictions, see table12-1.
- **Inboard digital anti-aliasing filters** with upper AFC cutoff frequency equal to 0.45 of set ADC frequency.
- Program-accessible **logic signs of LTR24 ADC word size overflow** by the input signal are transmitted individually for each channel for each ADC sample (only when configured for the 24-bit ADC output format).
- Connector pins of LTR24-1, LTR24-2 are fully compatible with LTR22 but synchronization signals at the connector are not used.
- All 4 channels of LTR24 module are synchronous and have no relative phase shift.
- In the "AC + DC" mode, LTR24 has a linear phase-frequency characteristic (PFC) (this is important for some vibrometry applications). In the "AC" mode, PFC is linear except for the low-frequency band (less than 5 Hz), where a constant component compensation mechanism has an active effect on AFC.

- Within one LTR crate, the relative phase shift of data acquisition between LTR24 modules will always be constant in *time because the single reference generator of LTR crate is an ADC frequency reference source* (Appendix A.16, page 359).
- Within the same LTR-EU crate, synchronous command issuing to all LTR24 modules installed in the crate will be possible (paragraph4.7.1, page 93) that will allow to phase internal data collection [1]pipelines in ADC and to synchronize the moments of data output to the LTR interface. This capability is to be expanded to LTR-EU by updating FPGA crate-controller firmware.
- It is planned to implement a technical capability (paragraph 4.7.1, page 93) in LTR-EU crates which will allow for synchronous starting of several LTR24 and LTR35 DAC modules to form a multi-channel synchronous DAC-ADC system for measuring through characteristics of pipelines, conducting vibrometry tests, etc.
- A possibility of redundant connection of more than one LTR24 to the same signal sources is supported.
- It is assumed that the operation of data correction with account for calibration factors using the line correction method is performed by user computer (library functions are provided).
- LTR24 supports 20- or 24-bit data transmission format (single-length or double-lenght LTR word, respectively).
- In the double-length word from LTR24 there is also a sign of instantaneous value of the signal reaching the ADC word size which allows for recording ADC overload events for each channel separately, and there are also data about the channel number, input voltage subrange set for this channel, and data continuity rolling counter.
- In single-length word from LTR24, except for data, the channel number and data continuity sign are only contained.
- **Signals at LTR24 user connector** are galvanically isolated from the ground (frame) of LTR crate and from other LTR modules (signals are not galvanically isolated from each other).

[1] sigma-delta ADC has a deep pipelined architecture

12.1.4 Spectral characteristics of LTR24.





The signal amplitude spectrum described above are cleared when a 1.3 kHz sine signal is sent to LTR24 differential inputs if "2V" (spectrum on the left) and "10V" (spectrum on the right) subranges are set. The "0 dB" level on the spectrum corresponds to the signal peak amplitude in the set subrange. FFT (fast Fourier transformation) for 20,000 points with a Blackman-Harris window is used.

12.1.5 LTR24 module configuration

The basic configuration of LTR24 is described in paragraph 2.4 , page 29.

12.2 Installation and set-up

During LTR24 installation in crate, observe the module installation rules common for LTR system, see paragraph3.6.2.2, page 52.

LTR24 board has one process 6-pin connector **Do not put jumpers on process connectors and make any external connections to them!**

12.3 Overview of LTR24 hardware components and operation principles

LTR24 is ADC based on **Texas Instruments ADS1274** converter chip with four parallel synchronous data digitizing channels.

16 data acquisition frequency grid (ADC conversion frequencies) is implemented for each channel:

$$F_{ADC} = \frac{60 * 10^6\ Hz}{256 * n}, \qquad (12\text{-}1)$$

$$where\ n = \{2,3,4,6,8,12,16,24,32,48,64,96,128,192,256,384\}$$

Data acquisition frequencies (ADC conversion frequencies) are always equal across all channels. Data acquisition from any of four channels may be allowed or denied. Either 20-bit or 24-bit data format can be assigned for all channels. The combinations of ADC data width, number of channels and ADS1274 converter modes supported in LTR24 are presented in the table below.

Table12-1. Possible operation modes of LTR24

ADC ADS1274 data collection frequency, Fdata, kHz	Parameter *Oversampling Ratio* of the converter	Mode of the converter	Supported combination of ADC data format and number of channels	
			ADC data width	
			20 bits	24 bits
			Number of channels (special case: LTR-U-1)	
117.188	64	high-speed	1÷4 (1)	1÷2 (0)
78.1250	64	high-speed	1÷4 (1÷2)	1÷3 (1)
58.5938	64	high-speed	1÷4 (1÷3)	1÷4 (1)
39.0625	128	High-Resolution	1÷4	1÷4 (1÷2)
29.2969	128	High-Resolution	1÷4	1÷4 (1÷3)
19.5313	128	High-Resolution	1÷4	
14.6484	128	High-Resolution	1÷4	
9.76563	128	High-Resolution	1÷4	
7.32422	128	High-Resolution	1÷4	
4.88281	128	High-Resolution	1÷4	
3.66211	128	High-Resolution	1÷4	
2.44141	128	High-Resolution	1÷4	
1.83105	128	High-Resolution	1÷4	
1.22070	128	High-Resolution	1÷4	
0.915527	128	High-Resolution	1÷4	
0.610352	128	High-Resolution	1÷4	

Note:

1. 4 bytes at the upper software level correspond to the 20-bit data format and 8 bytes correspond to the 24-bit format.

2. The set of physical channels may vary within the total number set.

3. In brackets, the number of channels for the special case of LTR-U-1-4 crate with limited USB 1.1 (full-speed) interface throughput is specified in the table.

Unused ADC channels can be switched-off in software for saving data transmission traffic.

The **Oversampling Ratio** parameter indicated in the table above implicitly means internal converter averaging ratio: the higher it is the larger is the converter resolution. The **Oversampling Ratio** is not user-programmable and is selected automatically depending on the set data acquisition frequency.

For the user, the difference between the High-Speed and High-Resolution modes is actually a converter group delay difference: in the High-Speed mode, it is equal to 38 ADC conversion periods and in the High-Resolution mode, to 39 ADC conversion periods. This difference should be taken into account only if a particular synchronization principle is applied, the user solves the problem to obtain a synchronization time accuracy comparable to the ADC conversion period. The High-Speed and High-Resolution modes are not set independently; the setting of these modes is always strictly dependent on the assigned conversion frequencies according to table12-1.

12.3.1 LTR24 (LTR24-1) block diagram.

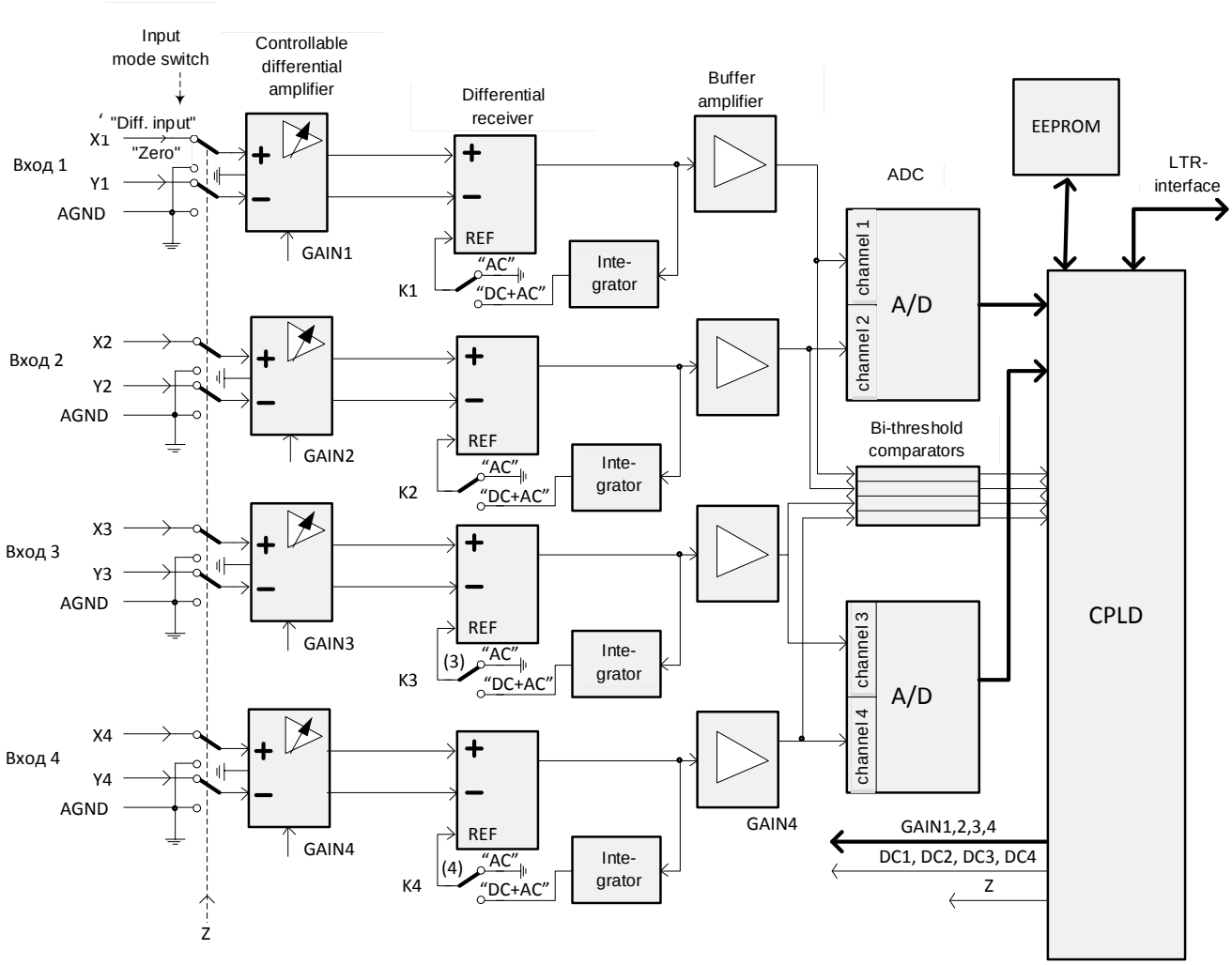


Fig.12-1. LTR24 (LTR24-1). Block diagram

LTR24 block diagram includes four identical conversion channels. Each channel of LTR24 contains:

- High-quality high-resistance differential input with high common-mode rejection ratio allowing for "tune out" strongly from the signal common-mode interference component (paragraph 12.3.3). Protection circuits are installed at “X” and “Y” inputs relative to AGND circuit (paragraph 12.4.4, page 210).
- *Input switch* of modes of measurement of signals from differential input ("Dif. input") and own zero ("Zero") which does not generate any transition processes on LTR24 input lines in the normal operating mode. If it is necessary to prevent zero shift under steady temperature conditions to the maximum possible extent, the user can set "Zero" test *mode* prior to the measuring session, under which zero voltages are fed to LTR24 channel inputs. However, ADC readings will correspond to ADC inherent offset voltage under current settings of LTR24. At the upper software level, full compensation of ADC residual zero shift can be ensured by deducting this shift voltage value from the readings obtained in the nearest measuring session after the data adjustment using factory calibration factors. *"Zero" test measurement mode is set for four channels simultaneously*.
- Controllable differential amplifier with a wide dynamic range implements two measurement [1]subranges in LTR24: “±2 V”, “±10 V”.
- Differential receiver implementing the common-mode rejection function, and, in conjunction with the integrator and the "DC/DC+AC" switch, implementing the DC component compensation function, if the "AC" mode is enabled (paragraph 12.3.9).
- Buffer amplifier creating the required electrical conditions at the input of the ADC for optimal converter operation.
- Bi-threshold comparator recording impulse overload events at the ADC input.
- ADC (A/D) – 4-channel ADC ADS1274.
- EEPROM – 0.5 MB non-volatile memory for storage of calibration factors, serial numbers and other process information.
- CPLD – programmable digital chip (no option for remote firmware updating). The digital control part of LTR24 is fully implemented on the CPLD basis.

12.3.2 LTR24-2 functionalities.

Block diagram of this modification differs from other ones with extended input switching functionality. "ICP-input" and "ICP-test" modes are also added to the "Dif. input" and "Zero" modes:

- "ICP input" is an *operating measurement mode* for measuring signals from ICP sensor connected to ICP1- ICP4 input of the corresponding channel. *LTR24-2 allows for setting "Dif. input" and "ICP input" modes independently for each of the four channels.* "AC" mode is used only because the variable component of the signal is measured at the ICP input.

[1] Note that the implementation of higher numbers of measurement subranges makes no common sense at 24-bit ADC bit width and high linearity of the conversion inherent in sigma-delta ADCs of this class.

- "ICP test" mode is a *test mode* to monitor offset voltage in the ICP-sensor circuit which allows for detecting extreme events of breakage or short circuit in the ICP sensor circuit. *In LTR24-2, "ICP test" and "Zero" modes can be set independently for each of the four channels.* "DC+AC" mode is used only because the constant component of the signal is measured.
- LTR24-2 can be configured either for operating input modes ("Dif. input", "ICP-input") or for test modes ("ICP test", "Zero"). *Combined setting of operating and test modes at different inputs is impossible*. However, "Dif. input"/"ICP-input" modes can be combined in different channels that allows to connect up to 8 signal sources (4 ICP + 4 dif.), but in this case readings can only be taken from any four sources in one session.

A simplified diagram of module input circuits is shown on the fragment of the block diagram of input circuits of channel 1 of LTR24-2 (fig.12-2) module.

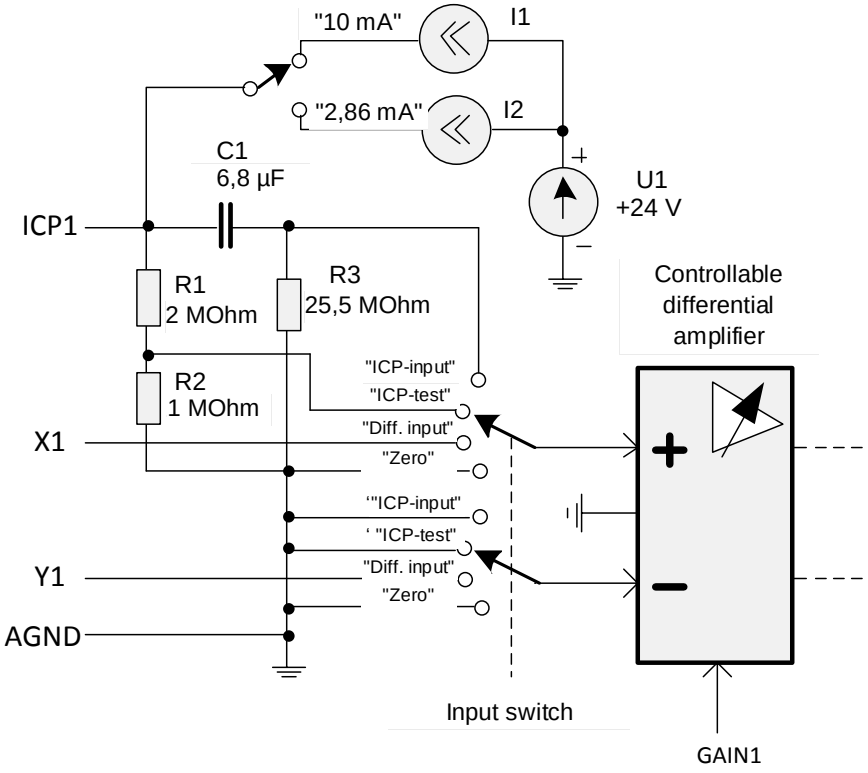


Fig.12-2. LTR24-2. Block diagram fragment (input-output signals of channel 1)

Internal module power supply U1 (+24V) is used for power supply to sensors circuits.

Current generators I1, I2 allow to maintain constant current in ICP1 sensor circuit. In each channel, current generators are different but *current values "2.86 mA" or "10 mA" can be set the same only for four channels.*

Differentiating circuit C1 - R3 separates the higher constant component of offset voltage in sensor circuit and supplies the variable component to the amplifier input when the switch is in "ICP input" state.

High-resistance voltage divider R1-R2 with voltage division ratio of 1:3 supplies the divided voltage to the amplifier input in the ICP sensor circuit when the switch is in "ICP test" state. If the sensor circuit is broken (or the sensor is not connected), measured voltage in the ICP sensor circuit in the "ICP-test" mode will reach +24 V (based on 1:3 division ratio). If a short circuit occurs in the sensor circuit, measured mean voltage will be about zero (or significantly less than the minimum possible offset voltage at the sensor output based on its nameplate data and taking into account 1:3 division ratio).

12.3.3 LTR24 application.

In the *"Dif. input" mode*, LTR24 measures voltage applied between differential inputs X and Y of the respective channel. For correct measurements, X and Y voltage values relative to AGND circuit must fall within the operating range, see Appendix A.10 on page 339. ±10 V measurement range is divided into two subranges of "±10 V" and "2 V". In "AC+DC" mode, the frequency bandwidth is from 0 to the half of ADC conversion frequency. In "AC" mode, the lower limit of the frequency bandwidth is equal to (0.48 ± 0.6) Hz at 3 dB level and the upper limit is the same as in "AC+DC" mode.

In *"Zero" mode*, LTR24 measures inherent offset voltage (additive error voltage) of differential input.

In *"ICP-input" mode*, LTR24-2 measures the variable voltage component in the ICP-sensor circuit within bandwidth from 1.3 Hz (paragraph 12.3.9, page 203) to the half of ADC set conversion frequency. The actual measurement range of the variable component of ±10 V or ±2 V (peak values) is actually divided into two measuring variable component mean square value subranges of "~5 V" and "~1 V". The peak (maximum) values range of ±10 V for the variable component of the signal is maintained at ICP-sensor offset voltage (paragraph12.3.4) equal to 10 V. If the physical ICP sensor ensures 8 to 12 V offset voltage, the amplitude range of the ICP input signal variable component will make ± 8 V.

In *"ICP test" mode* , LTR24-2 measures offset voltage in the ICP sensor circuit for detecting breakage and short circuit events in the sensor circuit. The measurement range for *"ICP test"* input is from 0 to 25 V. This mode is intended for measuring the constant component only in the ICP sensor circuit for test purposes.

LTR24-2 module (in *"Dif. input" mode* with using current source of *"ICP-input" circuit*) may be used forresistance measurement by indirect method , by measured voltage and known current calibrated value (paragraph 12.4.9). In "DC+AC" mode, resistance will be measured with account for the resistance constant component (tensometry) and in "AC" mode, the variable resistance component only will be measured (vibrometry). Standard API libraries provided by L-Card do not support resistance calculation by the indirect method. The accuracy of DC resistance measurement will depend on the selected voltage measurement range and current value. The accuracy of measurement of the variable resistance component will also depend on signal frequency, cable length (capacity) and sensor resistance. Resistance measurement resolution will also depend on the connection quality. It is important to note that the "indirectness" of this method lies also in the fact that the metrological characteristics of the resistance measurement mode are not standardized by L-Card, and this procedure is not included in the LTR24 Verification Procedure.

12.3.4 Brief information about ICP sensors.

The ICP® (Integrated Circuit-Piezoelectric) technology was developed by PCB Piezotronics (http://pcb.com/) and is used for production of vibration, shock, strain gauges, force sensors and pressure sensors. ICP ® sensor is a piezoelectric sensor with a microelectronic charge preamplifier. The integrated amplifier is powered by a two-wire circuit. In this case, the same wires are used

through which a signal is routed from the sensor. An external DC source supplies power to the integrated amplifier which, in turn, converts high-impedance charge signal from the piezoelectric crystal into a low-impedance voltage for subsequent transmission to the data acquisition system. The advantage of such type of sensor is its ease of use, cheap cable and the possibility to pull cable lines for a distance of more than 300 meters. It is important that the ICP sensor with its electronic components always maintains the level of the constant component of the output voltage (offset voltage) within the tolerance limits (in the nominal range of the supply currents).

2.86 mA sensor supply current is a power-efficient mode designed for relatively short cables (tens of meters) or for applications with signal frequency falling in the low-frequency band of audio frequencies.

10 mA sensor supply current is a less power-efficient mode used for applications with long cables (hundreds of meters) or for broadband signals the upper frequency spectrum of which is in the high-frequency band of the audio frequency range and above.

Let us consider the quantitative effect of sensor supply current. The sensor supply current effect $I_п$ mentioned above is actually explained by the [1]cable capacity effect $C_к$ preventing signal voltage changing by more than ΔU_c for a time period of t:

$$\Delta U_c = \frac{I_п * t}{C_к}$$ (Unit of measurement: volt, ampere, second, farad)

In other words, the maximum voltage build-up rate [2] at ICP sensor output $\frac{\Delta U_c}{t}$ is always limited by the value of $\frac{I_п}{C_к}$. The higher is sensor supply current, the greater voltage change rate can be achieved at a given cable capacitance. Cable capacitance $C_к = C_p * L$ is proportional to capacitance per unit length and C_p (фарад/метр) cable length (metre).

It is recommended to use LTR24 together with ICP sensors with offset output voltage from 8 to 12 VDC at +24V power supply voltage (at a wider range of offset voltage, the useful range of peak values for ICP-input is narrowed).

12.3.5 Calibration

Calibration factors are recorded in EEPROM by the manufacturer for each of 4 channels, for each of two measuring subranges, for each of eight ADC conversion frequencies (calibration for each conversion frequency has not been implemented before in other ADCs of LTR family; in this case, such calibration has been necessary to achieve the claimed accuracy).

The data correction operation in accordance with calibration factors should be performed at the upper software level with the use of respective API-functions. This correction is performed mathematically by linear principle (with account for zero and scale shift).

---

[1] The given ratio is a define integral value $U_c(t) = \frac{1}{C_к}\int_0^t I_п(t)dt$ for $I_п(t) = const$. This integraltheoretically describes the current and voltage relations for capacity $C_к$ for a time period of t.

[2] In the strict sense, the above limitation only applies to voltage changing from low to high because voltage changing in the opposite direction is determined by current passing through the low-resistance output of ICP sensor, and the attainable rate of this change is pre-determinedly more rapid.

12.3.6 AFC normalization.

LTR24 has two predefined physical components determining AFC fall at particular frequencies:

1) AFC of analog path is amplitude dependence on input signal frequency.
2) AFC of ADC filter is amplitude dependence on input frequency-to-ADC conversion frequency ratio.

The purpose of AFC normalization is to provide the user with ready normalizing functions of compensating filters allowing to improve the accuracy of measurements in the signal bandwidth up to ¼ of ADC sampling frequency[1]. This capability is built into LTR24 API-library functions. The corresponding values of filter factors are recorded into module EEPROM.

12.3.7 Overflow event signaling at converter input.

The applied ADC ADS1274 or any other sigma-delta ADC has a high-order lowpass filter (LPF) in its architecture determining the AFC upper cutoff frequency. Additionally, it can be stated that LTR24 input analog path has the pass band higher than the ADC AFC cutoff frequency. Based on these circumstances, when LTR24 is used, for example, in vibrometry applications, a short-time overload event is technically possible at the ADC input which will not lead to an unambiguously detectable ADC "off-scaling" but to a distortion of the signal digitization process because the signal is actually limited, though for a short time. And for sure, such limitation will distort the sampled signal spectrum that is critical for a number of applications.

Overflow event signaling at the converter input is performed in LTR24 by inserting an overflow logic sign into the data stream when LTR24 is set for 240-bit data format. The overflow sign appears in case of an overflow with a signal of any polarity. The overflow sign is individual for each of 4 channels.

The overflow sign appears when the input signal exceeds 96÷99% of half converter range for a signal of any polarity. It is noteworthy that in case of setting for one of "±2 V" or "±10 V" subranges when normal data correction is performed in accordance with calibration factors the overflow sign will appear *beyond the set subrange limits* Thus, *the physical sense of overflow signs is achieving converter linearity limits but not exceeding the limits of set voltage subrange*.

It is important that overflow sign is inserted into the data stream in advance of about 39 ADC samples because this is the signal conversion group delay of ADC. This means that:

- when the overflow sign is received in the data stream from LTR24, the real time moment corresponding to the overflow will come in 39 samples later;
- when data acquisition from LTR24 is started, the overflow sign should be ignored for first 39 samples because it corresponds to the time before LTR24 startup.

In case of setting for 20-bit data format, the overflow signs will not be inserted into the data stream because these signs do not fit in this format.

12.3.8 20-bit and 24-bit data formats in LTR24.

Because of the limited LTR module interface capacity, two data formats have been implemented in LTR24:

1) 20-bit data format corresponding to 4 bytes at the upper software level, contains the following fields: 20 bits of ADC data, channel number, bit of data continuity counter and format attribute (see **DATA_20** format in table12-6, page 218).

[1] The correction task in the signal bandwidth from ¼ to ½ of the sampling rate requires that higher-order compensating filters be used but such task is not set.

2) 24-bit data format corresponding to 8 bytes at the upper software level, contains the following fields: 24 bits of ADC data, channel number, data continuity counter and format attribute (see **DATA_24** format in table12-6, page 218).

Accordingly, potential combinations of number of channels and data acquisition frequency are given in table12-1 on page 196 for these data formats.

It should be noted that 24-bit mode has no sense for the vast majority of tasks because the user will not obtain any significant improvement of ADC metrological features for traffic doubling (after the transition from 20 to 24 bits).

However, 24-bit format may be advantageous for specific tasks (for example, correlation analysis for large samples exceeding 1 million samples)[1].

12.3.9 "AC" mode. AFC in the low-frequency band.

Sometimes, a user deals with high constant component of the signal sent to ADC against relatively low variable component. If the constant component is not meaningful for the given task, it would make sense to use the "AC" mode enabled independently for each channel. In the "AC" mode, an AFC fall occurs in the low frequency band with a sharpness of 6 dB/octave which corresponds to the first-order HPF (high-pass filter). The ranges of signal constant component compensation and AFC cutoff frequencies for the "AC" mode are given in Appendix A.10 on page 339. Note that the range of constant component compensation is significantly expanded with the reduction of variable component values relative to the set range.

ADC residual zero shift for the "AC" mode is not calibrated in the process of LTR24 manufacturing.

AFC in the low frequency band for different modes is shown on the diagram below. Here, the transmission ratio (amplitude) is expressed in relative values.

[1] L-Card did not carry out any special quantitative investigation.

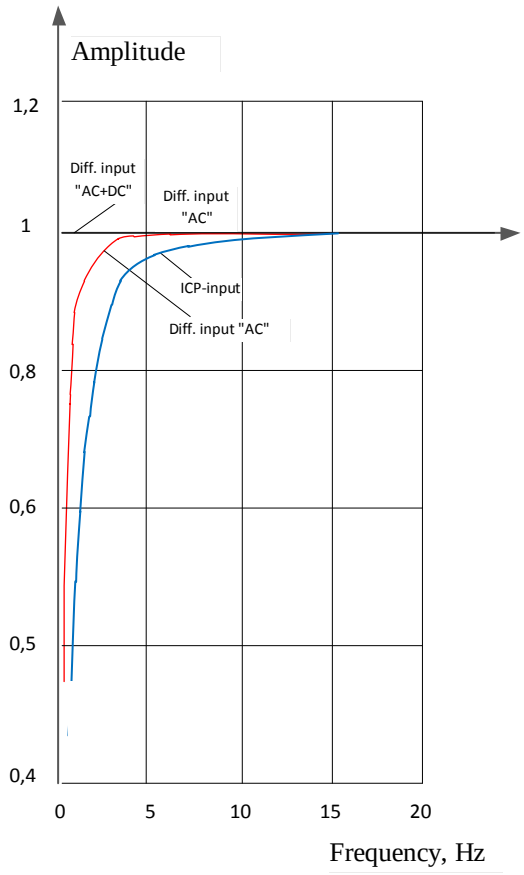


Fig.12-3. AFC in the low-frequency band of LTR24.

No low-frequency cut occurs in "AC+DC" mode of differential input.

In "AC" mode of differential input, the lower frequency bandwidth limit at -3 dB level is equal to 0.48 Hz.

In "ICP-input" mode, the lower frequency bandwidth limit at -3 dB level is equal to 1.3 Hz.

12.3.10 Anti-aliasing filter.

In any mode of its operation, LTR24 effectively suppresses high-frequency components of the signal with a frequency of above the half of the set sampling frequency.

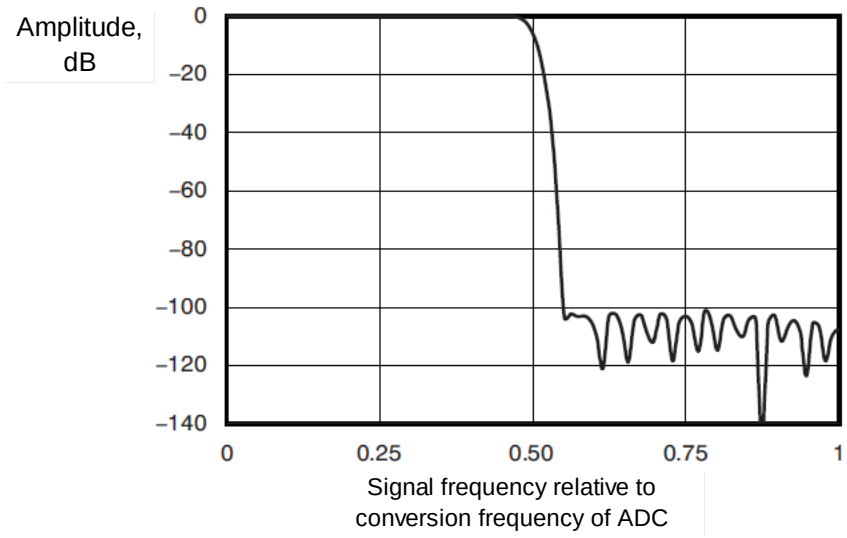


Fig.12-4. AFC of anti-aliasing filter in LTR24

From a practical standpoint, an anti-aliasing filter significantly improves the quality of signal digitizing by eliminating out-of-band high-frequency noise of different nature that improves the signal-to-noise ratio.

Due to the fact that LTR24 bandwidth is strictly bound to ADC conversion frequency and with the increase of conversion frequency internal ADC noise is reduced (and the full dynamic range of ADC is extended), the user is recommended to select the lowest conversion frequency for this task based on the maximum dynamic range criterion.

12.3.11 Module firmware version.

LTR24 contains CPLD, a programmable logic circuit with non-volatile firmware. As the product is upgraded, the firmware can also be upgraded. This firmware can only be updated by L-Card (remote update is not supported). LTR24 firmware version is software-accessible. The history of all LTR24 firmware modifications is given with comments in the table below.

LTR24 firmware version	Comments
0	First (informal) firmware of 8 ADC conversion frequencies for "LTR24" modification
1	Firmware of 16 ADC conversion frequencies for "LTR24" modification
4	Firmware for "LTR24-1" modification
36	Firmware for "LTR24-2" modification
Remaining values to 63	Reserved for future versions

Notes:

A possible firmware version range from 0 to 3 is assigned for "LTR24" modification

A possible firmware version range from 4 to 35 is assigned for "LTR24-1" modification

A possible firmware version range from 36 to 63 is assigned for "LTR24-2" modification

Thus, *LTR24 modification can be definitely identified by the firmware version*.

12.4 Connection of signals

Read the general rules for signal connection, paragraph 3.6.6, page . 58

LTR-24 module has DRB37M panel-mount connector for connection of input signals. External connections to LTR24 should be implemented by connecting signal circuits to the cable part of the connector (DB-37F type). Application of signals is given in Table11-1, and the view of the panel-mounted connector is presented in Fig.11-4 .

Table12-2. Application of LTR24 user connector signals

(see fig.12-5, fig.12-6 after the table)

Signal name	Common point	Direc-tion	Description
AGND	–	–	Analog ground
X1, X2, X3, X4	AGND	Input	– Uninverting voltage input of channels 1…4 – Operating voltage range: ±10 V
Y1, Y2, Y3, Y4	AGND	Input	– Inverting voltage input of channels 1…4 – Operating voltage range: ±10 V
+15V, -15V	AGND	Output	Output for external device power supply Homonymous outputs "+15 V", "-15V" as well as AGND circuit of different LTR24 modules can be connected to perform the redundancy function, see paragraph 12.4.10, page 213. Load current of up to 30mA relative to AGND. When ICP1, ICP2, ICP3, ICP4 circuits are used in LTR24-2 for sensor power supply, the operating load on "+15 V", " -15 V" circuits shall not exceed 10 mA
n/c	–	–	**The contact shall not be connected.** These contacts are not connected inside LTR24 and are reserved for further modifications of LTR24.
n/c / ICP1, n/c / ICP2, n/c / ICP3, n/c / ICP4	AGND	– /Input-output	Dedicated lines for connection of four ICP-sensors (in the "ICP-input" mode in LTR24-2). When an ICP sensor is connected (paragraph 12.4.7, page 0), the circuits simultaneously perform the function of stable current source outputs of ICP- sensors and signal voltage inputs from the sensor. ICP dead line should be left unconnected. In the "dif. input" mode, these circuits can be used as outputs of 10 or 3 mA stable current sources for power supply to external resistance-strain gauges in 4-wire connection diagram. If no connection to ICP inputs is required, the ICP1÷ ICP4 circuits shall not be connected.

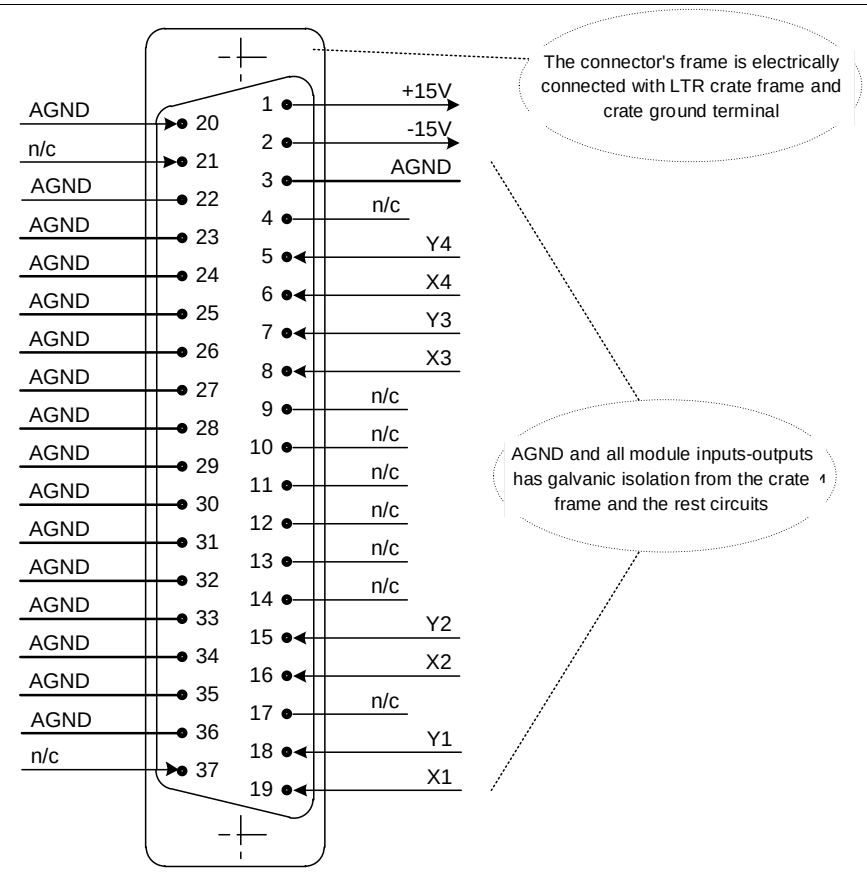
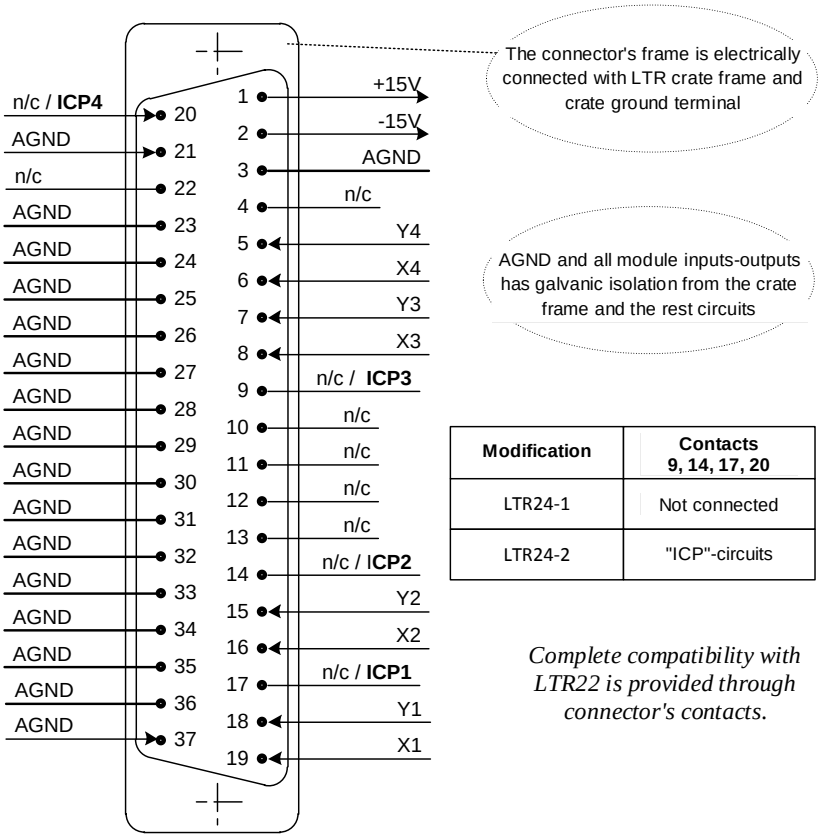


Fig.12-5. Circuits at LTR24 connector.

"LTR24" modification is being discontinued (paragraph 12.1.2, page 192)



Modification	Contacts 9, 14, 17, 20
LTR24-1	Not connected
LTR24-2	"ICP"-circuits

Complete compatibility with LTR22 is provided through connector's contacts.

Fig.12-6. Circuits at the connector of LTR24-1 and LTR24-2 modifications.

12.4.1 Characteristics of signal line inputs and outputs

When connecting LTR24 module to your system, strictly observe the parameters specified in tables of this section.

The manufacturer shall not be warranty liable for LTR24 failure caused by violation of maximum permissible operation conditions.

The following symbols are given in tables of this section:

AI is analog input,

DI is digital input,

DOZ is digital output with the *third state*,

P is external device power output.

ICP is special input for connection of ICP-sensor

Note that impedance of input lines is greater in the *operating mode* than in the *switched-off* state of LTR24 module. See information about the *switched-off module state* in section4.8.

The characteristics of galvanic isolation in LTR are given in Appendix A.18.

12.4.2 LTR24 operating mode

LTR24 module installed in LTR crate has the following characteristics of input and output signal lines after LTR crate is powered on:

Table12-3. Maximum permissible conditions, module LTR24 is switched-on.

Signal	Type	Operation mode	Maximum permissible conditions
X1, X2, X3, X4, Y1, Y2, Y3, Y4	AI	Input resistance more than 10 MOhm at ±10 V relative to AGND under normal conditions	±20 V relative to AGND, ±27 V – in short-time mode (1 s)
+15 V, -15 V	P	Load current of up to 30 mA relative to AGND. When ICP1, ICP2, ICP3, ICP4 circuits are used in LTR24-2 for sensor power supply, the operating load on "+15 V", " -15 V" circuits shall not exceed 10 mA	Load current of 50 mA relativeto AGND foreach output in the continuous operation mode. In LTR24-2, when ICP1, ICP2, ICP3, ICP4 circuits are used for sensor power supply, the maximum permissible continuous current in power circuits "+15 V", " -15 V" shall not exceed 20 mA. Typical short circuit current of 400 mA[1] is permissible for max. 1 second. In the event of a short circuit at outputs "+15 V", "-15 V", this module can be automatically de-energized in the crate with further self-recovery after the short-circuit elimination.

[1] the parameter is not tested in the process of manufacturing

Signal	Type	Operation mode	Maximum permissible conditions
ICP1, ICP2, ICP3, ICP4	ICP	Internal direct current resistance of circuits in ICP1, ICP2, ICP3, ICP4 at a voltage from 0 to 22 V is not more than 3 MOhm. The circuit current is 3 mA (10 mA) at a voltage from 0 to 22 V relative to AGND	From –1 V to +27 V under current no exceeding condition (if external current source is connected erroneously) ±30 mA.

No certainty of the state of the unconnected inputs X1, X2, X3, X4, Y1, Y2, Y3, Y4 is guaranteed.

The potential at unconnected high-resistance inputs is determined by nano-ampere leakage-currents which may be different in different modules.

12.4.3 LTR switched-off state

See *information about the* switched-off module state in section4.8.

In this mode, LTR24 module is deenergized and impedance of analog and digital input lines is low in comparison with the operating mode

Table12-4. Maximum permissible conditions, module LTR24 is switched-off.

Signal	Type	Input impedance	Maximum permissible conditions
X1, X2, X3, X4, Y1, Y2, Y3, Y4	AI	min. 1 kOhm	±20 V relative to AGND
+15 V, -15 V	P	–	–

12.4.4 Internal protection circuit of ADC differential inputs.

Analog inputs X and Y in LTR24 have an internal protection circuit shown in the figure below. These inputs are high-resistance in the operation mode when input voltage does not achieve the threshold value of ±12 V at input X or Y. When voltage exceeds the threshold of ±12 V, input resistance drops to 1 kOhm because an internal diode signal limiting circuit comes into operation which is shown in the figure below.

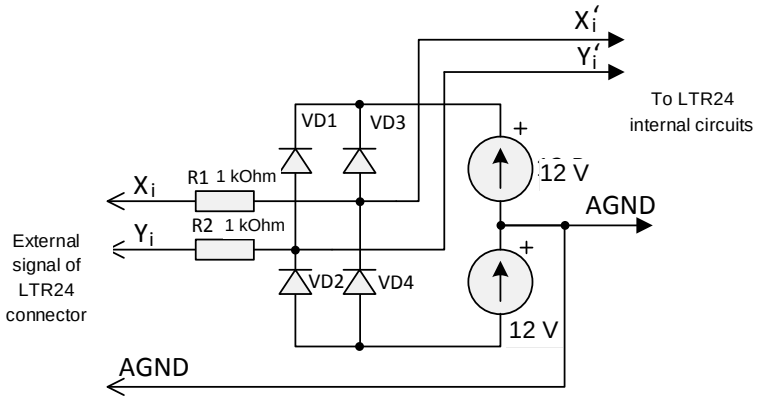


Fig.12-7. LTR24. Equivalent input protection circuit for "X", "Y" inputs (operating mode).

This feature of LTR24 inputs should be taken into account if LTR24 signal input range can potentially be exceeded in your connections.

12.4.5 Equivalent electric diagram of ADC input circuit.

The issue of LTR24 input impact on a measuring circuit arises for applications providing for signals measuring in high-resistance circuits and at relatively high frequencies. To evaluate this impact, consider an equivalent electric diagram of input circuits for LTR24 *operation mode*.

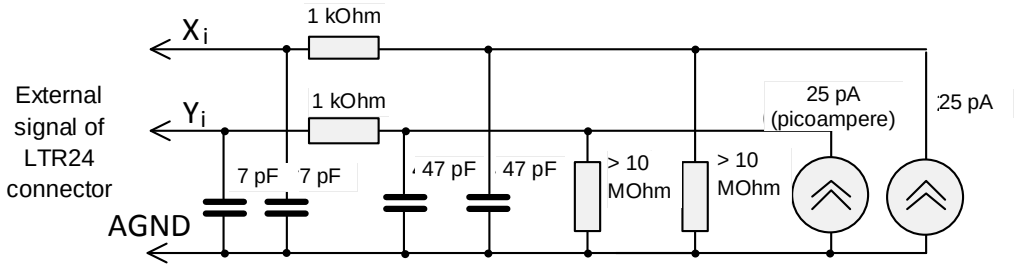


Fig.12-8. LTR24. Equivalent electric diagram of input circuits.

Note: All parameters of this equivalent network are obtained by calculation using *typical values* of characteristics of applied electronic components specified in their documentation for LTR24 measurement *normal conditions*. Current sources used in the diagram are own input current of LTR24 differential amplifier unit (fig.12-1, page 197). The direction of this current is not regulated and is shown conventionally.

12.4.6 Examples of input signal connections

Two most typical connection diagrams for input analog signals are given in Fig. below[1] . Combined variants of differential and single-phase source connections are also possible.

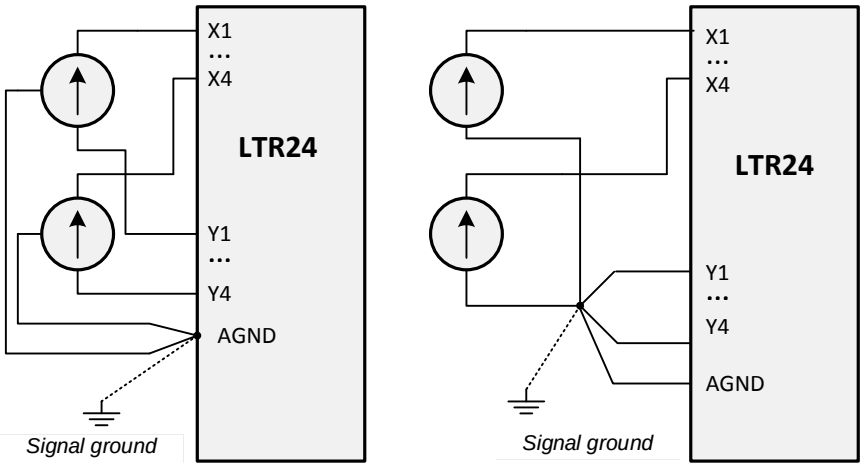


Fig.12-9. Signal sources connections to LTR24

If it is required to change the converted signal polarity relative to the physically issued signal, the connection of circuits X and Y should be changed in the corresponding channel.

[1] The issues on measuring units connecting are described in detail in the article [2]

12.4.7 Connection of isolated ICP-sensors

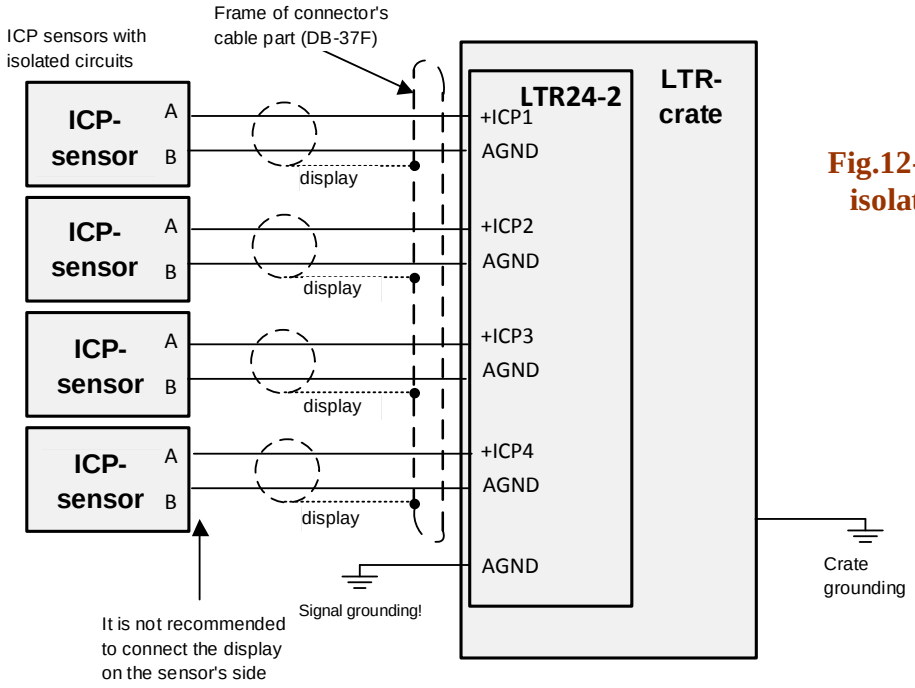


Fig.12-10. Connection of isolated- ICP-sensors (LTR24-2)

12.4.8 Connection of non-isolated ICP-sensors (LTR24-2)

In this case, ICP sensors usually have a coaxial connector connected to the sensor housing and, respectively, to the housing of the structure to which the sensor is attached. In this case, it is not recommended to ground the AGND circuit at LTR24-2 side in order to prevent through current flow via signal cables and the module.

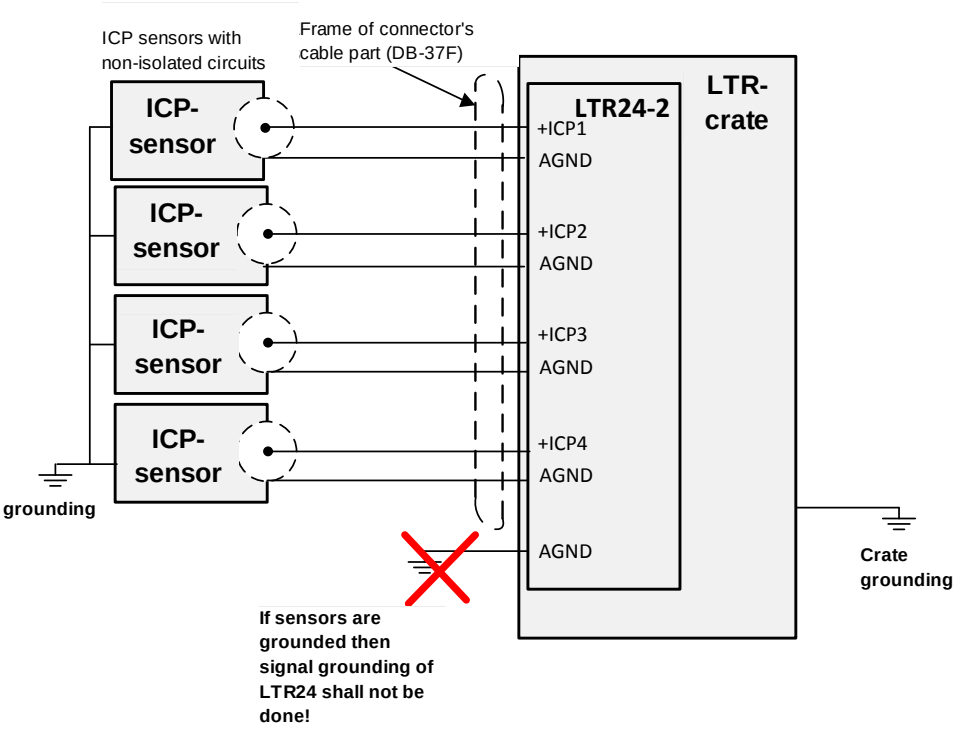


Fig.12-11. Connection of non-isolated ICP-sensors (LTR24-2)

12.4.9 Connection of external resistance strain gauges (LTR24-2)

For this connection diagram (fig.12-12), the voltage measuring mode "Dif. input" should be used and the required stable current of 10/2.86 mA should be set in software (for 4 ICP-inputs simultaneously). The resistance value R can be calculated by the user on his PC as R=U/I, where U is measured voltage and I is calibration current value for the respective channel. Calibrated current value is read from LTR24-2 Flash-memory

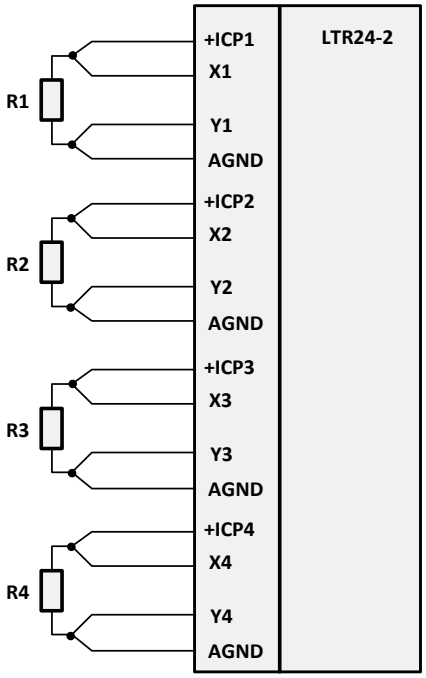


Fig.12-12. LTR24-2 resistance measuring diagram

12.4.10 Redundant connection of LTR24 to differential inputs.

To arrange a redundant (duplicated) connection of LTR24, it is enough to connect different LTR24 modules according to the figure below. Full duplication can be provided if the connected modules belong to different LTR crates.

Redundant connection of ICP inputs (for LTR24-2 modification) is not supported.

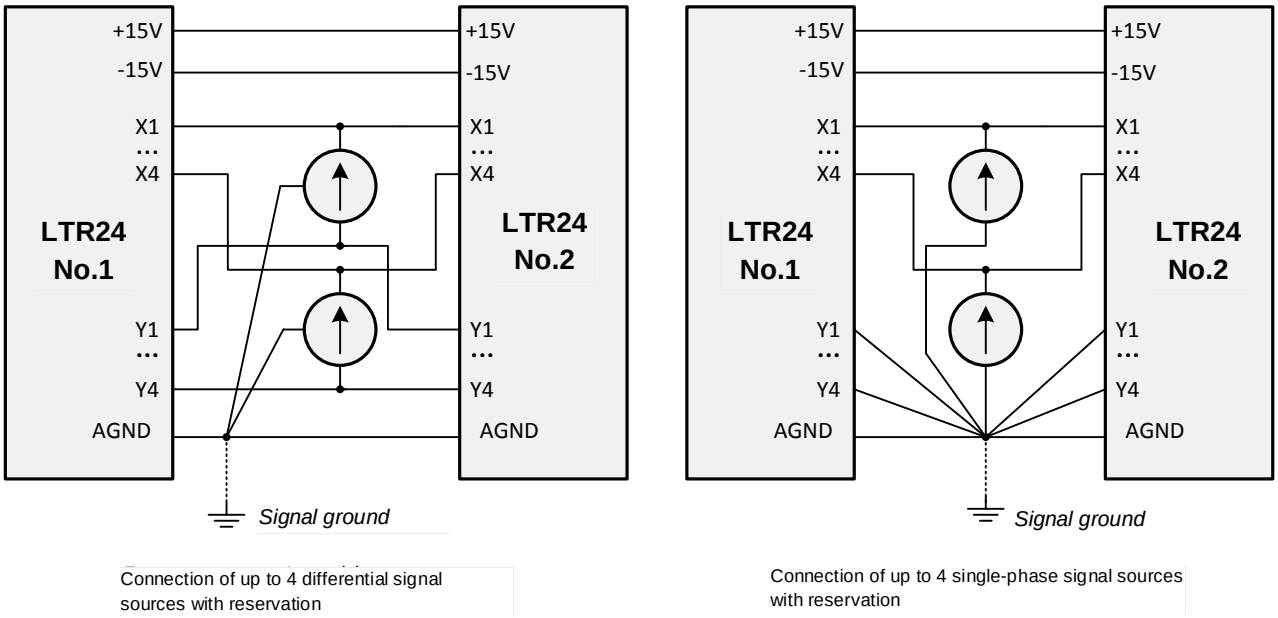


Fig.12-13. Examples of LTR24 redundant connection

These circuits maintain high-impedance state for X and Y inputs of duplicated modules, in which the signal source will not be shorted if at least one LTR24 is energized.

12.5 LTR24 module control (low-level description)

For the majority of users working with LTR via the LTR-server using API functions, information presented in this chapter will be of no interest. However, this information is necessary for "advanced" programmers working with LTR24 at the lower level.

12.5.1.1 LTR24 command system.

Conventions:

- Zero values should be assigned to "x" fields.
- Information in all tables is described from the most-significant to the least-significant byte.
- Channel numbers NN in the data format always form the sequence 0,1,2,3,0,..., from which forbidden channels are deleted.
- Data format must be described using the interface protocol conventions set out in paragraph 4.6, page 82.

Table12-5. LTR24 control commands.

Command/ data to LTR24	Format: bit C, byte 1, byte 2, byte 3	Response	Description
STOP	1 00xxxxxx xxxxxxxx xxxxxxxx	No	

Command/ data to LTR24	**Format: bit C, byte 1, byte 2, byte 3**	**Response**	**Description**
RESET	1 10xxxxxx xxxxxxxx xxxxxxxx	RESET_RESP	**Module reset.** The command immediately returns all module hardware to the initial state (FIFO- buffer is cleared) and the module sends back a module identifier, see Table 14-4. The STOP command must always be issued prior to the RESET command.
ROM_IO *[only in the standby mode]*	1 0110000S DDDDDDDD 00000000	Yes	**Low-level access to serial Flash memory AT25DF041A** according to the principle of one ROM_IO access per **AT25DF041A** time diagram byte. S is CS signal of AT25DF041A (active level is high). Bit-by-bit diagram of **1 byte length is sent to AT25DF041A input:** **DDDDDDDD is** data (high-order bit first). SCK signal (8 pulses) is generated automatically by CPLD hardware. Other commands should not be contained in the command sequence ROM_IO, and the STOP command should be performed after the end of the sequence, see the graph in fig.12-14
INSTR1	1 1110xxxx xx0SxxxF EEEEqqqq	Yes (only if GO=0)	Control of ADC frequency and data format: **qqq<3:0>** – *FREQ_CODE* **(see the table above)** **EEEE<7:4> – Data resolution of physical channels (active drive)** *En_Ch*: <0> - from the first physical channel <1> - from the second physical channel <2>- from the third physical channel <3>- from the fourth physical channel **F<8>** Data output format setting: *Format24* “0” is 20-bit format (LTR single word) “1” is 24-bit data format (LTR double word) Access to this register is denied when data acquisition is started (GO=1)! **S <0> is ADC synchronization permission** *Sync_Mode<0>* 0 is ADC frequency synchronization prohibition. 1 is DC frequency synchronization permission.
INSTR2 GO	1 1101xxxx xxxxxxxx xxxxxxxx	No	Start of data acquisition (GO) Under ADC synchronization prohibition (*Sync_Mode = 0*) the start command will be ignored. Data acquisition should be stopped by the STOP command. Improper for other LTR modules but possible for LTR24 option is full RESET, upon which the data acquisition will be stopped first and then the module will send a response to RESET. *Both variants stop the data acquisition process at the transmitted data boundary of current channel (which was being transmitted at that moment): for 20-bit data format, at the boundary of the 32-bit word; for 24-bit data format, at the boundary of the 64-bit word transmitted.*

<table>
<tr><th>Command/ data to LTR24</th><th>Format: bit C, byte 1, byte 2, byte 3</th><th>Response</th><th>Description</th></tr>
<tr><td>INSTR3 (ANALOG CONTROL)</td><td>1
1100xxxx
xxIHHHHZ
BBBBDDDD</td><td>Yes
(only if GO=0)</td><td>
Analog path control.
DDDD<3:0> Enabling constant component cutoff (at "1" – "AC+DC" mode, at "0" – "AC" mode):
<0> - in the first physical channel
<1>- from the second physical channel
<2>- from the third physical channel
<3>- from the fourth physical channel
BBBB<7:4> – subrange "=10 V"/ "~5 V" (at "1")
or "=2 V"/"~1 V" (at "0") :
<4> - of the first physical channel
<5> - of the second physical channel
<6>- of the third physical channel
<7>- of the fourth physical channel
Z<8> Input switch control (LTR24, LTR24-1):
“0” is test input mode
“1” is operating input mode
For LTR24 and LTR24-1, "Test mode" means "Zero" mode (for all channels)
For LTR24-2, "Test mode" and "Operating mode" provides for extended functions depending on the field HHHH<12:9>, see below.
<table>
<tr><td>H<9></td><td>Z<8></td><td>State of channel 1 switch</td></tr>
<tr><td>1</td><td>0</td><td>"ICP-test" test mode</td></tr>
<tr><td>0</td><td>0</td><td>"Zero" test mode</td></tr>
<tr><td>0</td><td>1</td><td>"Dif. input" operation mode</td></tr>
<tr><td>1</td><td>1</td><td>"ICP-input" operation mode</td></tr>
<tr><td colspan="3"></td></tr>
<tr><td>H<10></td><td>Z<8></td><td>State of channel 2 switch</td></tr>
<tr><td>1</td><td>0</td><td>"ICP-test" test mode</td></tr>
<tr><td>0</td><td>0</td><td>"Zero" test mode</td></tr>
<tr><td>0</td><td>1</td><td>"Dif. input" operation mode</td></tr>
<tr><td>1</td><td>1</td><td>"ICP-input" operation mode</td></tr>
<tr><td colspan="3"></td></tr>
<tr><td>H<11></td><td>Z<8></td><td>State of channel 3 switch</td></tr>
<tr><td>1</td><td>0</td><td>"ICP-test" test mode</td></tr>
<tr><td>0</td><td>0</td><td>"Zero" test mode</td></tr>
<tr><td>0</td><td>1</td><td>"Dif. input" operation mode</td></tr>
<tr><td>1</td><td>1</td><td>"ICP-input" operation mode</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Command/ data to LTR24</th><th>Format: bit C, byte 1, byte 2, byte 3</th><th>Response</th><th colspan="3">Description</th></tr>
<tr><td></td><td></td><td></td><td>H<12></td><td>Z<8></td><td>State of channel 4 switch</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>0</td><td>"ICP-test" test mode</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>0</td><td>"Zero" test mode</td></tr>
<tr><td></td><td></td><td></td><td>0</td><td>1</td><td>"Dif. input" operation mode</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>1</td><td>"ICP-input" operation mode</td></tr>
<tr><td></td><td></td><td></td><td colspan="3">I is current source current (LTR24-2 only) (for 4 channels simultaneously):
0 is "3 mA"
1 is "10 mA"

The INSTR3 command will be performed at any time including data acquisition time ("on-the-fly"), but if GO=1 the confirmation will not arrive!</td></tr>
<tr><td>INSTR4 (STOP_DATA_ACQ)</td><td>1
1111xxxx
xxxxxxxx
xxxxxxxx</td><td>Yes</td><td colspan="3">Data acquisition stop with confirmation</td></tr>
</table>

Table12-6. LTR24 responses to control commands

Command/data from LTR24	Format	Description
RESET_RESP	1 10**V**vvvvv 00011000 00011000	**Response to RESET.** Contains a module identifier: in the second and third byte, decimal "24". State of **V** bit reflects ICP inputs availability (for LTR24-2 modification only): **V** = 0 – ICP inputs are not available (LTR24, LTR24-1 modifications) **V** = 1 – ICP-inputs are available (LTR24-2 modifications). PLD firmware version number of this module is written in **V**vvvvv field –**Version (from 0 to 63), see paragraph** 12.3.11**, page** 206. -
ROM_RESP	1. 01100000 DDDDDDDD XXXXXXXX	**Response to Flash-memory reading.** Sent by the module in response to the ROM_IO command. D is data (diagram from 8-bit EEPROM output).
INSTR1 _RESP	1. 11100000 00000000 0000000P	**Response to INSTR1** **(no response if GO = 1)** P=1 attribute will be contained in the response to the first INSTR1 command after powering-on. In all other cases, P=0.
INSTR3 _RESP	1. 11000000 00000000 00000000	**Response to INSTR3 (no response if GO = 1).**
INSTR4 _RESP	1. 11110000 00000000 00000000	**Response to INSTR4 data stop.**
DATA_20	0. 0PNNDDDD DDDDDDDD DDDDDDDD	NN-channel number P is data continuity counter (P=1 in every fifteenth word, for the rest P=0). If GO=0 the counter is reset to zero. D is data.
DATA_24	0. 10NNCCCC 0000000**O** DDDDDDDD 0. 11NNCCCC DDDDDDDD DDDDDDDD	**O** is overflow sign in NN channel. “1” – overflow “0” – no overflow CCCC is module 15 word count (values from 0 to 14) which is incremeted after each DATA_24 data format. Set to zero if GO=0

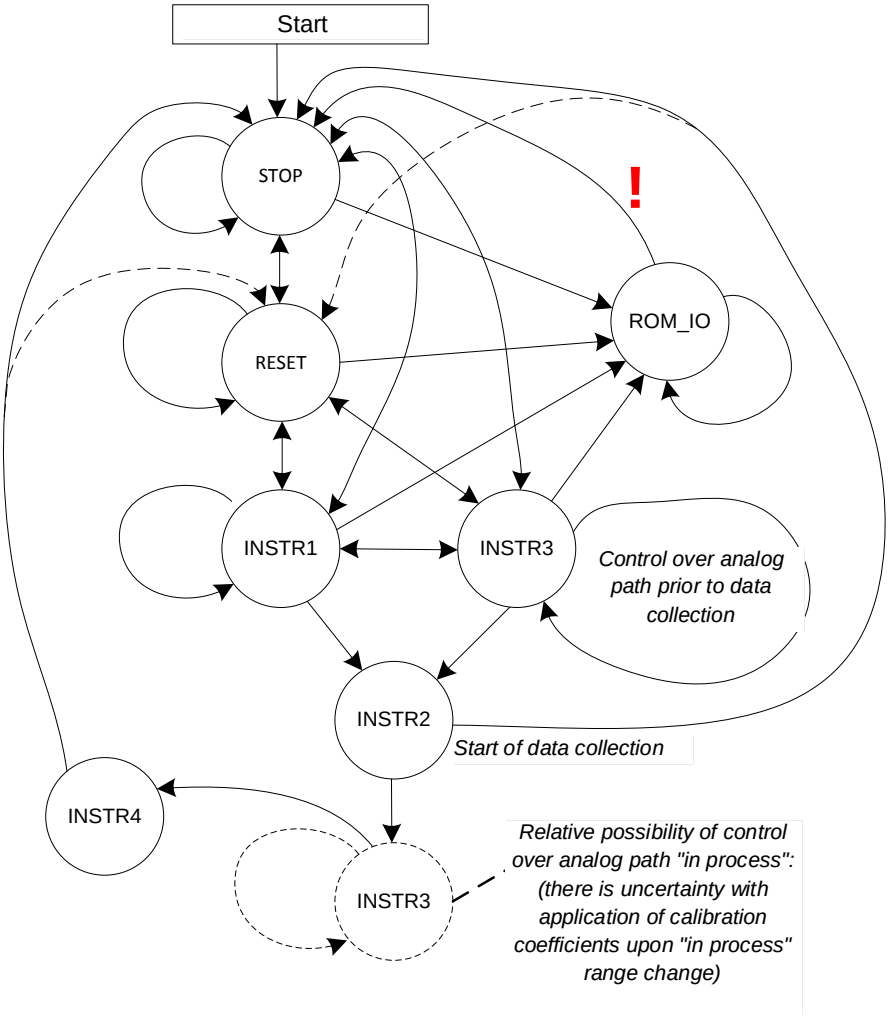


Fig.12-14. Permissible sequence of commands for LTR24 (graph)

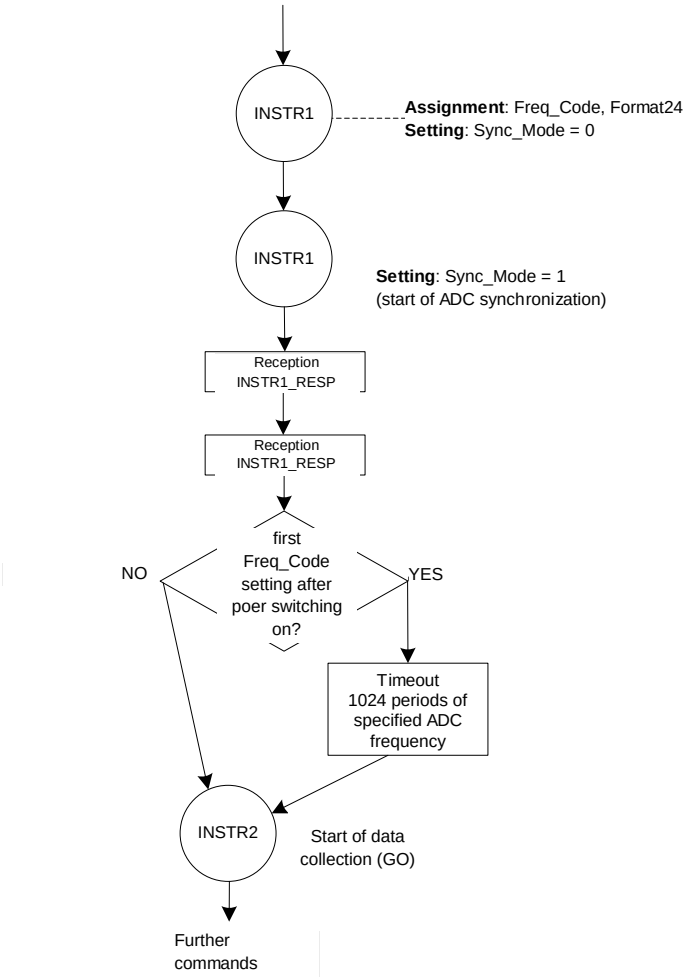


Fig.12-15. LTR24. Fragment of the command sequence for the start of data acquisition

Chapter 13. LTR25 ADC module (announce)

13.1 General description of LTR25

13.1.1 Intended purpose

LTR25 module is a 8-channel 24-bit specialized ADC intended for the use in combination with ICP-sensors (paragraph 12.3.4), for example, vibration converters, in multi-channel data acquisition systems.

LTR25 allows for creating high-quality multi-channel vibrometry systems with relatively low-cost 1st measuring channel.

13.1.2 General information about LTR25

- LTR25 allows for direct and easy connection of up to 8 ICP sensors in a 2-wire circuit.
- External power supply units are not required.
- Auxiliary devices for ICP sensors matching are not required.
- Independent parallel measuring channels.
- 24-bit sigma-delta ADC in each channel.

- 8 conversion frequencies from 610.35 Hz to 78.125 kHz.
- Anti-aliasing filters in ADC path.
- Filter-decimation mechanism in FPGA with programmable factors of finite impulse response filters.
- "On-the-fly" data correction in FPGA in accordance with calibration factors.
- 2.86/10 mA supply current sources of ICP sensors in each channel.
- Independent software recognition of ICP sensor breakage and short circuit events during data acquisition in each measuring channel.
- FPGA auto-loading from the Flash-memory (no time is spent on external loading of FPGA firmware). Software-updated FPGA firmware.
- Multi-purpose 2 MB Flash-memory.
- Large unused computing resource in FPGA Cyclone IV (more than 75%) provides for future implementation of vibration velocity calculations, development of filtration capabilities and implementation of other DSP (digital signal processing) algorithms within LTR25 with both fixed and floating-point arithmetic.

Combinations of conversion frequencies, ADC data format, and number of channels supported in LTR25 are given in the table below.

ADC data acquisition frequency, kHz	**Supported combination of ADC data format and number of channels**	
	ADC data format	
	20 bits	24 bits
	Number of channels (special case: LTR-U-1)	
78.125	1÷6 (1÷2)	1÷3 (1)
39.066	1÷8 (1÷5)	1÷6 (1÷2)
19.531	1÷8	1÷8 (1÷5)
9.7656	1÷8	
4.8828	1÷8	
2.4414	1÷8	
1.2207	1÷8	
0.61035	1÷8	

Note:

1. 4 bytes at the upper software level correspond to the 20-bit data format and 8 bytes correspond to the 24-bit format.

2. The set of physical channels may vary within the total number set.

3. In brackets, the number of channels for the special case of LTR-U-1-4 crate with limited USB 1.1 (full-speed) interface throughput is specified in the table.

13.2 Overview of LTR25 hardware components and operation principles

13.2.1 LTR25 application.

LTR25 measures the voltage variable component in the ICP-sensor circuit in a passband starting from 1.3 Hz. The upper passband frequency is limited by ADC anti-alising filters and FPGA to about a half ADC conversion frequency. The precise values of the passband upper limit are defined by settings.

Actual voltage variable component measuring range is ±10 V (peak values). Considering potential unsinusoidality of input signal, the variable component root mean square measuring range makes "~5 V" at ICP sensor offset voltage (paragraph 12.3.4) equal to 10 V.

In the event that ICP sensor maintains offset voltage from 8 to 1 V, the variable component peak values range for ICP input signal will make ±8 V and voltage root mean square values measuring range will make "~4 V".

.

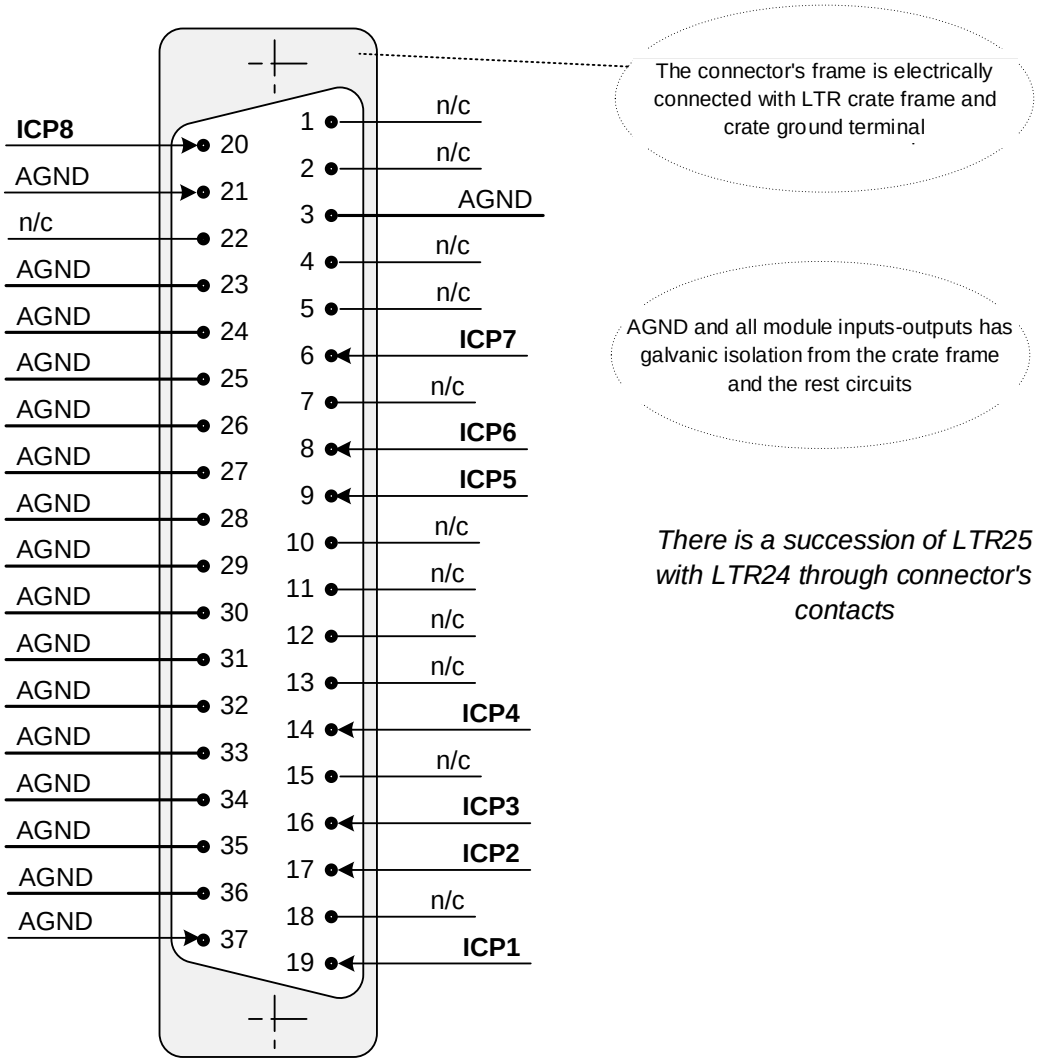
13.3 Connection of signals

Read the general rules for signal connection, paragraph 3.6.6, page 58.

-LTR25 module has DRB37M panel-mount connector for connection of input signals. External connections to LTR25 should be implemented by connecting signal circuits to the cable part of the connector (DB-37F type). Application of signals is given in paragraph 12.3.

Table13-1. Application of LTR25 user connector signals

Signal name	Common point	Direc-tion	Description
AGND	–	–	Analog ground
ICP1, ICP2, ICP3, ICP4, ICP5, ICP6, ICP7, ICP8	AGND	Input-output	Dedicated lines for connection of eight ICP-sensors. When an ICP sensor is connected, the circuits are simultaneously used as power stable current source outputs of ICP- sensors and signal voltage inputs from the sensor. ICP dead line should be left unconnected.
n/c	–	–	**The contact shall not be connected.** These contacts are not connected inside LTR25 and are reserved for further modifications of LTR25.



There is a succession of LTR25 with LTR24 through connector's contacts

13.3.1 Characteristics of signal line inputs and outputs

! When connecting LTR25 module to your system, strictly observe the parameters specified in tables of this section.

The manufacturer shall not be warranty liable for LTR25 failure caused by violation of maximum permissible operation conditions .

The following symbols are given in tables of this section:

ICP is special input for connection of ICP-sensor

The characteristics of galvanic isolation in LTR are given in Appendix A.18.

13.3.2 LTR25 operating mode

LTR25 module installed in LTR crate has the following characteristics of input and output signal lines after LTR crate is powered on:

Table13-2. Maximum permissible conditions, module LTR25 is switched-on.

Signal	Type	Operation mode	Maximum permissible conditions
ICP1, ICP2, ICP3, ICP4, ICP5, ICP6, ICP7, ICP8	ICP	Internal direct current resistance of circuits in ICP1- ICP8 at voltage from 0 to 22 V is not more than 5 MOhm. The circuit current is 3 mA (10 mA) at a voltage from 0 to 22 V relative to AGND	From –1 V to +27 V under current no exceeding condition (if external current source is connected erroneously) ±30 mA.

13.3.3 Connection of isolated ICP-sensors

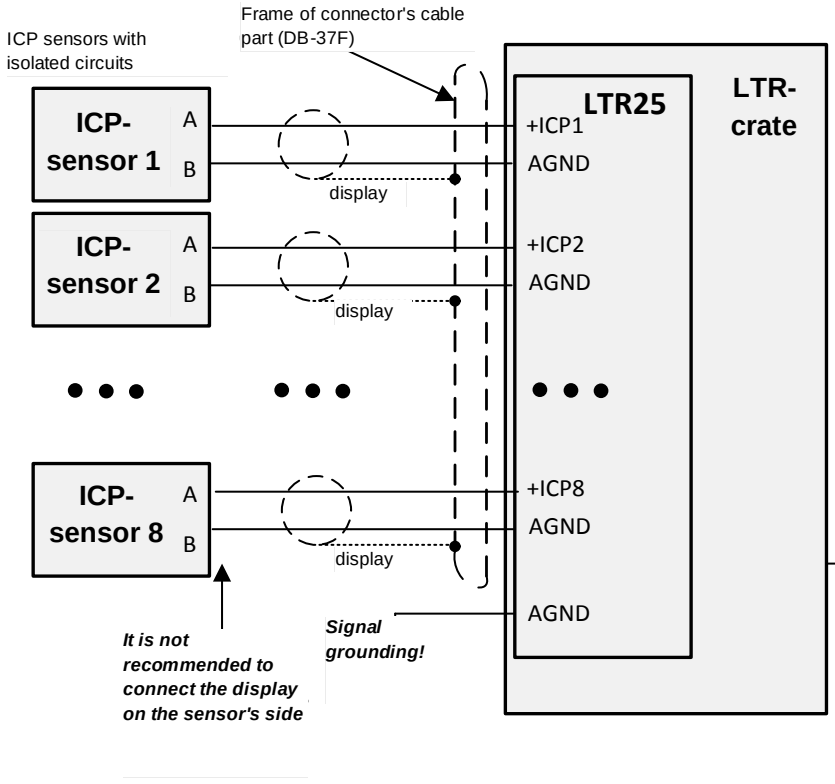


Fig.13-1. Connection of isolated ICP-sensors (LTR25)

13.3.4 Connection of non-isolated ICP sensors

In this case, ICP sensors usually have a coaxial connector connected to the sensor housing and, respectively, to the housing of the structure to which the sensor is attached. In this case, it is not recommended to ground the AGND circuit at LTR25 side in order to prevent through current flow via signal cables and the module.

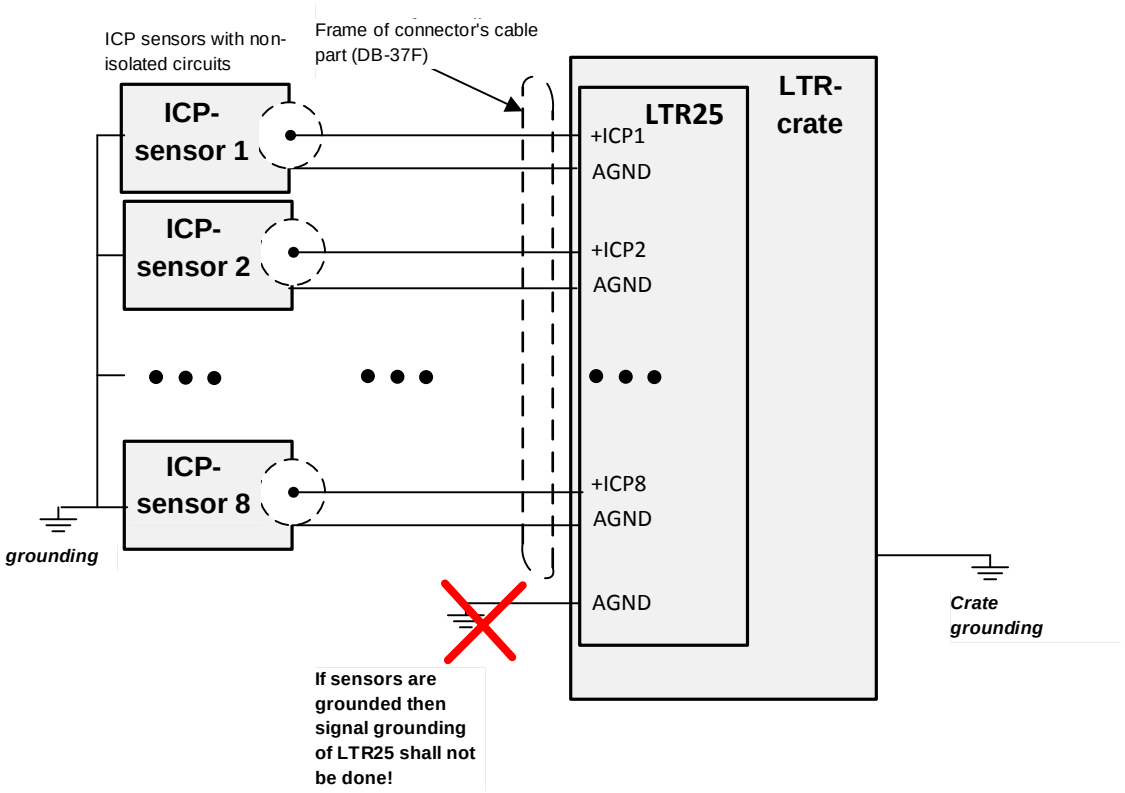


Fig.13-2. Connection of non-isolated ICP sensors (LTR25)

Chapter 14. LTR34 DAC module

14.1 General description of LTR34

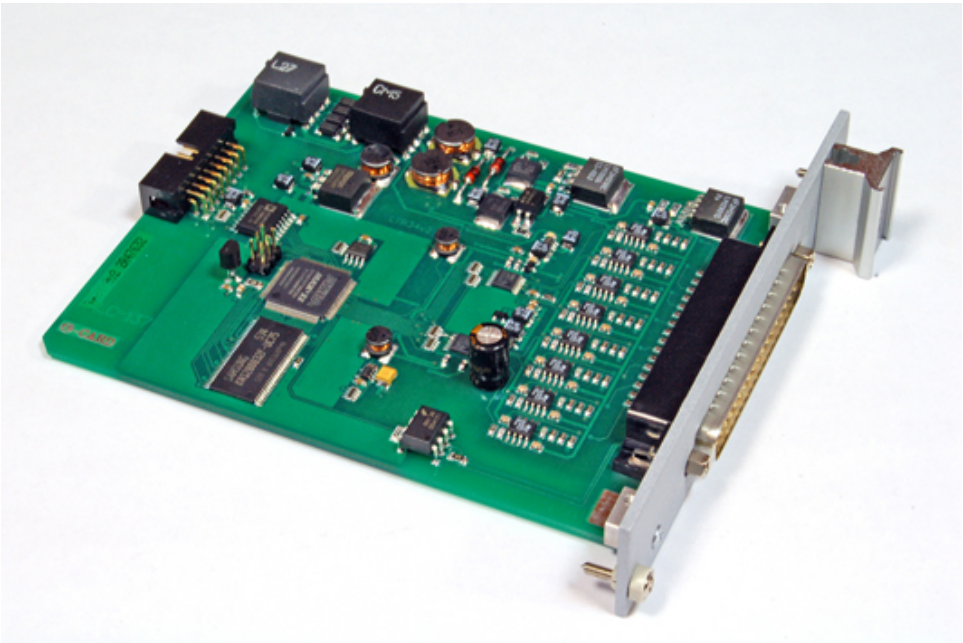


Fig.14-1. LTR34-8 view

14.1.1 Device application

Modules LTR34-4, LTR34-8 are 4- and 8-channel (respectively) digital-analog converters-(DAC)with 16-bit capacity. DAC is intended for extensive range of tasks requiring high-quality AC or DC voltage reproduction in synchronous or asynchronous modes, with data stream output (up to 500 kS/s) or in the in the self-excited oscillator mode with periodic signal generation and pre-pumping of digital signal of to 2 million samples in DAC buffer.

Both design versions of*LTR34 module* (-4 and -8) are identical in their configuration and parameters but different in the number of board-mounted channels and, thus, in the cost.

Comments to LTR34 application are given in paragraph 14.1.3, page 228.

14.1.2 General information about LTR34

- A reasonable balance is achieved between the DAC quality for direct and alternating current. DAC is based on a converter with low glitch energy, low temperature drift, small - differential non-linearity (less significant digit beat).
- Data output modes for DAC channels: *asynchronous output to selected channels, synchronous stream output* in 1-, 2-, 4- and 8- channel modes, *synchronous generation of periodic signal* (pre-recorded in LTR34 buffer) in 1-, 2-, 4- and 8-channel modes.

- *The frequency of samples synchronous output in DAC channel* Fs = F/N, where F is programmable common *frequency of data input* (61 frequency values in total) from the range of 500 kHz, 400 kHz, 333 kHz, …, 31.7 kHz, 31.25 kHz, N is number of used channels N = 1, 2, 4 or 8. For all channels, equal Fs frequency is set. The formula (14-1) defining the frequency spectrum is given on page 234.
- Each channel has two outputs: 1:1 and 1:10. Output signal ranges for each channel: ±10 V in 1:1 output, ±1 V in 1:10 output.
- *Automated periodic signal generation mode allows for pre-recording* of 2 to 2,000,000 samples into the DAC buffer, and then starting a synchronous cyclical sample output from the DAC *buffer without data swapping from PC* (self-exciting oscillation mode). What is more, from 2 to 2/N samples (equal dimensions for each channel) can be recorded in the buffer for each DAC channel. In particular, the fastest signal which can be reproduced by LTR34 is the square signal with a period of 4 usec in the single-channel mode, *and the slowest signal in the active oscillator mode with full buffer using can have a period of 64 s in the single-channel mode and about 8 min in the eight-channel mode.*
- *A huge number of signal period values which can be reproduced in the periodic signal autogeneration mode* : you can set a number of points per signal period (from 2 to 2 million), number of signal periods in the buffer (from 1 to 1 million), the value of *data output common frequencies F* (up to the 61-st value), the number of output channels (N = 1, 2, 4, 8).
- *Single-phase outputs of LTR34 are* galvanically isolated from LTR crate ground and from other modules. AGND common wire circuit is common for all outputs.
- *An external start input with a galvanic optoisolator* allows for starting synchronous data output by an external synchronization signal.

Complete specifications are given in Appendix A.12, page 348. Comments to LTR34 application are given in paragraph 14.1.3 , page 228 .

! Functionally, LTR34 is not equipped with micro controller and is a pure hardware module unlike other LTR-modules. In view of this, the low-level description of LTR34 is presented in this manual, and the Programmer's Manual only deals with the issues of upper-level LTR34 programming.

14.1.3 Comments to LTR34 application

LTR34 DAC is designed for tasks of high-quality reproduction of both direct and alternating voltages of signal with a frequency of up to 1-3 kHz in the output stream mode or in the periodic signal auto-generation mode. Unlike audio sigma-delta DAC[1], LTR34 has better DC performance but worse variable signals reproduction characteristics for frequencies higher than several kilohertz.

When LTR34 is used in control systems, *it should be noted that* at the moment of LTR crate powering-on a short-term transition process can occur at LTR34 outputs with an amplitude of up to 50% of the output range (in the steady mode, initial state of the outputs is close to zero voltage).

14.1.4 LTR34 module configuration

The basic configuration of LTR34 is described in paragraph2.4, page 29.

[1] for example, DAC H-34 of H-2000 system

14.2 Overview of LTR34 hardware components and operation principles

14.2.1 Block diagram

LTR34 physically contains:

- FPGA (specific FPGA loading after powering-on is not required). All digital logical units of LTR34 are implemented in FPGA.
- FIFO-data buffer for 2097151 samples (2 megasamples minus one word). The buffer is used as a standard FIFO for stream data output or can be "looped" from output to input for the periodic signal auto-generation mode. Physically, the FIFO- buffer is implemented on SDRAM basis with all addressing and control logic in FPGA.
- 2 KB Flash-memory for storing calibration factors and serial numbers. Read-only access is *permitted for* the user.

4- or 8-channel DAC. DAC is implemented on the basis of 4-channel DAC chips of DAC8555IPW[1] type and output buffer amplifiers providing an output signal range of ±10 V and ±1 V at outputs 1:1 and 1:10, respectively.

- Components of LTR -interface galvanic isolator.
- Secondary power source for power supply to internal module units.

The following functional units are shown on the block diagram (Fig. 14-2):

- *Packet Receipt Logic* and *Packet Sending Logic* implement the hardware protocol of LTR- module.
- The *RESET command processing* unit processes RESET commands coming to the module and sends the module identifier in response.
- *CONTROL Register* stores commands coming to the module.
- *START/STOP Logic* executes data output start-stop commands in DAC in conjunction with the External Start Logic.
- FIFO receives data packets for DAC and command packets for Flash-memory from the *Packet Receipt Logic* (terms and definitions related to commands and data are given in paragraph 4.6.2, page 83).
- *DAC1 Interface*, *DAC2 Interface* implement a protocol of data transmission from the -FIFO-buffer to DAC1 and DAC2 chips of DAC8555IPW type.
- Programmable *DAC Frequency Divider* sets the rate of data take-off from the FIFO-buffer to DAC and generates the parallel data strobing signal at DAC outputs.
- *STATUS Generation Logic* periodically generates STATUS response packets from LTR34 which contain information about the amount of accumulated data, FIFO- buffer overflow and underrun features in LTR34 and has a software capability to enable, if desired, an echo*data mode* when a data sample which has been output to DAC1 and DAC2 comes back in STATUS- packets. The latter option can be used to test data loop transmission.

LTR34 control issues are considered in detail in paragraph 14.4, page 229.

[1] manufactured by Texas Instruments Inc.

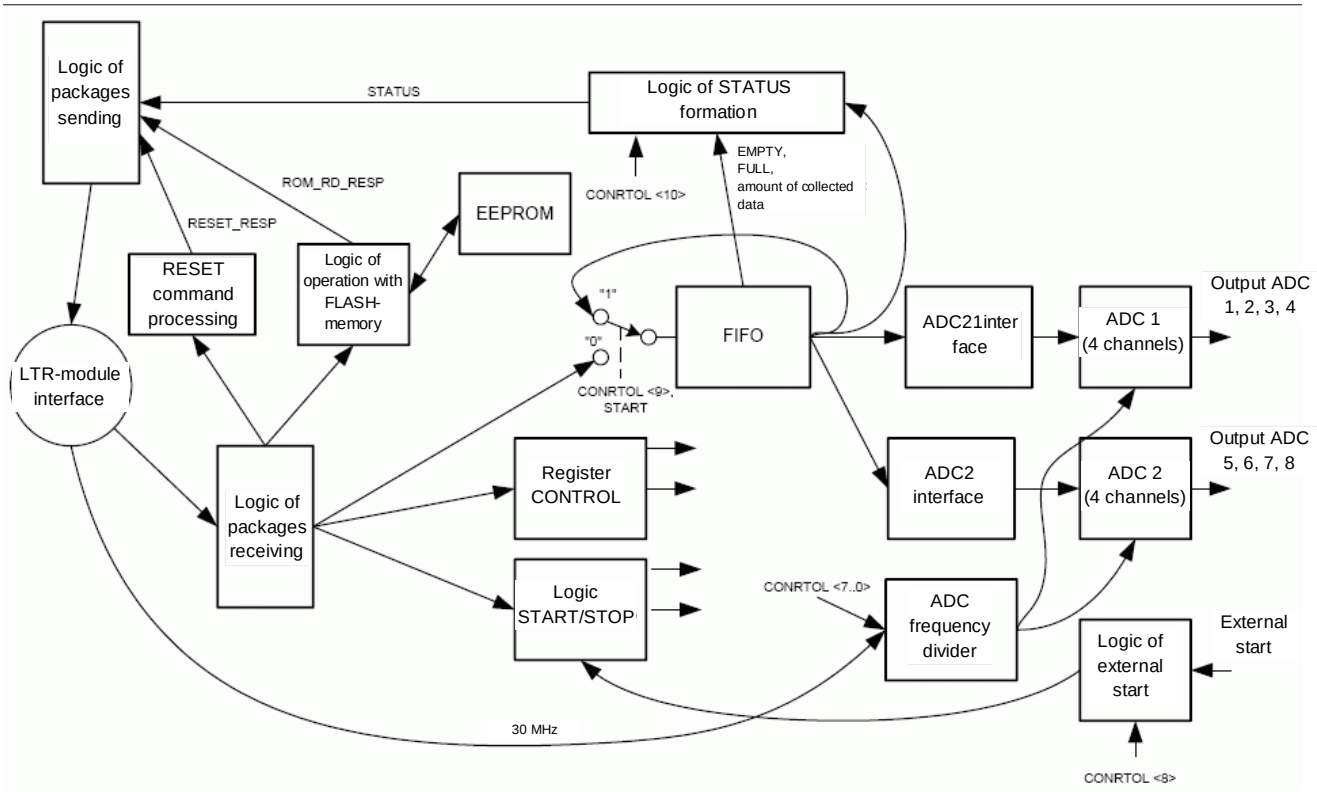


Fig.14-2. LTR34 module block diagram

14.2.2 Important issues of data stream arrangement when working with DAC

Specific issues described herein relate only to arrangement of synchronous (without data loss) data output stream to DAC by the user.

In the description of the architecture of LTR crate controllers, namely, in the section dealing with data paths (fig. 4-1. arrangement of ltr010 crate

, page 70), it was said that *data stream to LTR* modules is buffered in a single (i.e. one) input FIFO- buffer (allowing for buffering of at least 1 million 32-bit words-). This input FIFO buffer (as well as the output FIFO buffer) is intended for smoothing potential peaks of uneven transmission rate during data transmission via USB. Data packets passing through the input FIFO buffer get in order of their arrival to 16 small input FIFO buffers (with a size of ten 32-bit words per channel).

A *waiting event* can in principle occur in LTR controller when there is no space in a small output FIFO of the i-th channel for the next packet of the i-th channel, in which case LTR crate controller will wait until a transmission is performed to LTR- module of the i-th channel and free space appears in the small FIFO. *Waiting events* as such do not lead to data loss but sharply decelerate the output stream to LTR modules.

In LTR- crates without synchronous output to DAC, *waiting events* occur rarely and pass on unnoticed.

In LTR-crates with synchronous stream output to at least one -LTR34, *a waiting event* will occur certainly during the data transmission to another LTR module if *the data stream is not arranged by blending data to different LTR- modules according to the rate of transmission to LTR-modules,* namely: it is recommended to blend eight (or less) 32-bit words of one channel with words of other channel according to the rate of transmission to these channels (or rather: words from different channels should be blended according to the time of their arrival).

This feature should be primarily taken into account by those ambitious users who will apply stream output to LTR34 by programming LTR- crate directly without using the ideology of working with a LTR- module via server software proposed by L-Card.

When working with a LTR module via server software, such server software performs the data blending function which prevents the occurrence of a *waiting event* .

14.3 Connection of signals

Read the general rules for signal connection, paragraph 3.6.6, page 58.

LTR34 module has -DRB37M panel-mount connector for connection of input signals. External connections to LTR34 should be implemented by connecting signal circuits to the cable part of the connector (DB-37F type). Application of signals is given in Table14-1, and the view of the panel-mounted connector is presented in Fig.14-3.

Table14-1. Application of LTR34 user connector signals

Signal name	**Common** point	**Dir**ection	**Description**
AGND	-	-	Analog ground
OUT1 1:1 … OUT8 1:1	AGND	Output	Single-phase voltage outputs of channels 1…8, volatge range: ±10 V
OUT1 1:10 … OUT8 1:10	AGND	Output	Single-phase voltage outputs of channels 1…8, volatge range: ±1 V
START+	START-	Input	DAC external start synchronization input with individual optical galvanic isolation. Input voltage range -0.5...+5.5 V to START+ relative to START-. The input is compatible with TTL-outputs of 5-V logic. For example, if to connect START- to the common wire circuit (GND) of TTL-output of synchronization pulse source and to connect START+ to the output of this source, the start will occur on logic signal fall (1→0).
n/c			Unconnected connector contacts

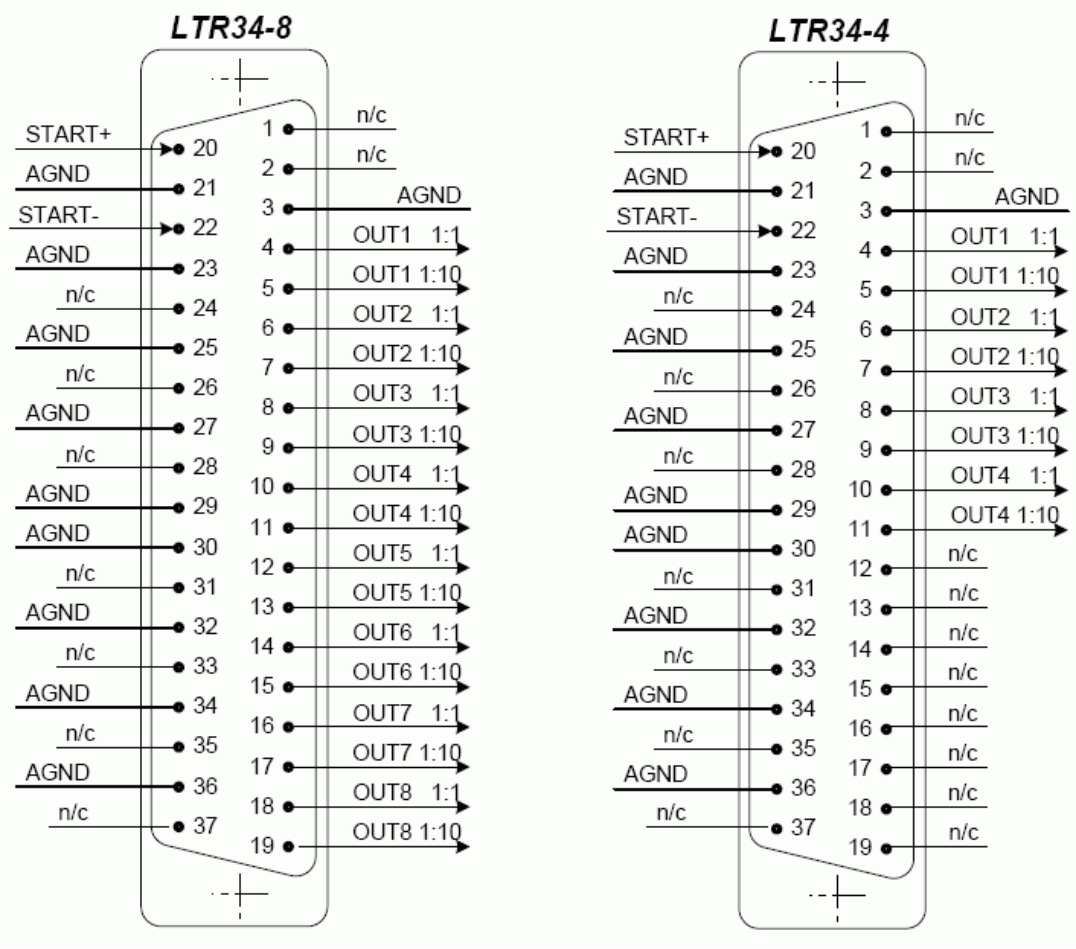


Fig.14-3. Signals at LTR34-4 and LTR34-8 module connectors

14.3.1 Characteristics of signal line inputs and outputs

! When connecting LTR34 module to your system, strictly observe the parameters specified in tables of this section.

The manufacturer shall not be warranty liable for LTR34 failure caused by violation of maximum permissible operation conditions.

The characteristics of galvanic isolation in LTR are given in AppendixA.18, page362.

The following abbreviations are used in tables of this section:

AO – analog output

DI – digital input.

14.3.2 LTR34 operating mode

LTR34 module installed in LTR crate has the following characteristics of input and output signal lines after LTR crate is powered on:

Table14-2. Maximum permissible conditions

Signal	Type	Maximum permissible conditions at input	Maximum permissible conditions at output
OUT1 1:1 … OUT8 1:1	AO		outputs are resistant to short circuit on AGND
OUT1 1:10 … OUT8 1:10	AO		outputs are resistant to short circuit on AGND
START+, START-	DI	-4…+9 V at START+ relative to START-	

14.4 Low-level description of LTR34

14.4.1 Command system

LTR34 can be in one of the two following states:

- *WAITING* – state of waiting for commands receipt, control and setting of LTR 34, EEPROM programming, and module FIFO- buffer pre-loading with data. This state always occurs after powering-on.
- *OPERATION*(operating cycle)– DAC output state subject to the pre-settings. The module switches over to this state on the START command.

In the operating cycle, LTR34 can receive either data for FIFO- buffer swapping in the process of data output to DAC (data swapping is not performed in the periodic signal generation mode) or the STOP command to stop data output to DAC and to transfer module to the *WAITING* state.

Table14-3. LTR34. Formats of input commands and data.

Command/ data to LTR34	Format: bit C, byte 1, byte 2, byte 3	Response	Description
STOP	1 00xxxxxx xxxxxxxx xxxxxxxx	no	**Module stop.** The command stops data stream from the module and switches it over to the *WAITING state*. Command without response.
RESET	1 10xxxxxx xxxxxxxx xxxxxxxx	RESET_RESP	**Module reset.** The command immediately returns all module hardware to the initial state (FIFO -buffer is cleared), and the module sends back a module identifier, see Table14-4. The STOP command must always be issued prior to the RESET command.
ROM_IO *[only in the standby mode]*	1 011000xx 00000000 00000000	yes	**Low-level access to EEPROM.** A response packet is sent to the EEPROM command, see Table 14-3. This command is ignored by the module in the *OPERATION*state. L-Card provides end user functions of reading from EEPROM using the ROM_IO command sequence. The function of recording in EEPROM is not provided to user.

Command/ data to LTR34	**Format: bit C, byte 1, byte 2, byte 3**	**Response**	**Description**
CONTROL *[only in standby mode]*	1 11100000 nn00LSGE ffffffff	no	**DAC settings recording:** **ffffffff** *is* CODE frequency code defining the sampling frequency F_s of a DAC channel (in Hertz): $$F_s = \frac{2*10^6}{(64-CODE)*N} \qquad (14\text{-}1)$$ where CODE=0,1,2,3,...,60; *N*=1,2,4,8. **E** *is* external start enable **G** *is* ring buffer enable (a generator function) **S** *is* a type of confirmation commands from the module: • **S**=0 *is* echo from each data sample • **S**=l *is* sending of the full buffer status every 1024 samples issued by DAC **nn** codes N number of channels used for output to DAC: • **nn**=0 *is* output to one channel (N=1) • **nn**=l *is* output to two channels (N=2) • **nn**=2 *is* output to four channels (N=4) • **nn**=3 *is* output to eight channels (N=8) **L** *is* FIFO buffer clearing control: • **L**=0 – no FIFO clearing • **L**=l – FIFO clearing (should be issued prior to dataupdating in the FIFO buffer)
START *[only in the standby mode]*	1 110xxxxx xxxxxxxx xxxxxxxx	status	**Module start**. On the command, the module switches over to the *OPERATION* state and data output to DAC starts subject to the pre-settings. Starting of periodical sending the STATUS information on the module state is the response to the START command, see Table14-4. Module shutdown is performed with switching over to the standby mode on the STOP command and stop of periodic sending STATUS responses. In the external start mode (set by the CONTROL command), the process of data output to DAC outputs triggered by the START command will physically start when the START signal edge comes to the external connector.

Command/ data to LTR34	**Format: bit C, byte 1, byte 2, byte 3**	**Response**	**Description**
DATA	`0 0000CCC0 DDDDDDDD DDDDDDDD`	status	**DAC data**. In the *WAITING* mode, initial buffer pumping is performed, while in the *OPERATION* mode, the buffer is swapped to ensure the continuous synchronous output to DAC. **D…D** *are* 16-bit data, **CCC** *are* codes numbers of channels: • 0– channel 1, • 1– channel 2, • ... • 15 – channel 16.

Table 14-4. LTR34. Formats of output commands and data.

Command/data from LTR34	**Format**	**Description**
RESET_RESP	`1.10gggggg.00100010. 00100010`	**Response to RESET.** Contains a module identifier: decimal "34" in the second and third byte. The `gggggg` field contains the number of FPGA firmware version for this module.
ROM_RESP	`1.01100000.00000000. 0000000x`	**Response to EEPROM reading.** Sent by the module in response to the ROM_IO command.
STATUS_PERIOD	`1.110ExxxF.0000ZZZZ. ZZZZZZZZ`	**FIFO buffer status periodic -signaling:** **E** –*EMPTY* signal **F** – *FULL* signal **Z**<11…0> *is* the amount of data accumulated in the FIFO buffer, in kilosamples **Z**=0, …, 2048. For details, see paragraph 14.4.1.1.
STATUS_ECHO	`1.111ECCCF.DDDDDDDD. DDDDDDDD`	**Data echo and short status of the FIFO-buffer:** **E** –*EMPTY* signal **F** –*FULL* signal **D**…D<15…0> – echo of data samples recorded in DAC **CCC**<15…0> – echo of DAC channel number of the corresponding sample For details, see paragraph 14.4.1.1

14.4.1.1 STATUS FIFO-of the buffer in details

Bit **E** is the *EMPTY* signal. **E**=**1** signals on the full FIFO buffer underrun error in the process of- data output to DAC which has caused an unpredictable delay in data output to DAC (the last set DAC output status is saved)

Bit **F** is the *FULL* signal. **F**=1 signals on the full FIFO buffer overflow -error in the process of data output to DAC that results in the loss of those data samples which have not been recorded in the FIFO- buffer due to its overflow.

Zero states of **E** and **F** indicate that no FIFO buffer errors have been recorded for the STATUS output period-.

Field **Z**<11…0> is amount of data accumulated in the FIFO-buffer rounded to kilosamples (downwards), **Z** = 0, …, 2048. In particular, **Z** = 0 corresponds to an amount less than 1 kilosample.

LTR34 module sends every subsequent command STATUS_PERIOD after reading 1K data samples from the FIFO buffer. Thus, LTR server software can support the required amount of data preventing buffer underrun for synchronous streaming data collection mode by monitoring the amount of data sent to LTR34 buffer and receiving the amount of data read out from LTR34 buffer.

14.4.2 Permissible sequence of LTR34 commands

The permissible sequence of commands is defined by the graph in Fig.14-4, page 237. If this sequence is not complied with, proper operation of LTR34 will not be guaranteed.

14.4.3 Permissible sequence of LTR34 synchronous data output

Since in LTR34 there is only one common FIFO buffer (common for all channels), this naturally limits the sequence of data samples for different channels which must correspond to the time of samples output in accordance with the set number of channels (1, 2, 4, or 8).

For example, in 4-channel mode, data can be sent in channels 1, 3, 6, 8 in the sequence of 4 samples from each channel. For example, the following sequence of channels in the data stream is permissible:

…, 3, 1, 6, 8, 3, 1, 6, 8, 3, 1, 6, 8, …

and even the sequence with permutation inside the quadruples (because these data quadruples will in any case appear at DAC outputs in parallel) is permissible:

…, 3, 1, 6, 8, 1, 3, 8, 6, 3, 6, 1, 8, …

but the following sequence is completely unacceptable:

…, 1, 1, 6, 8, 3, 3, 6, 8, 3, 6, 1, 8, …

as this will lead to missing of one sample from the 1-st and 3-rd channel.

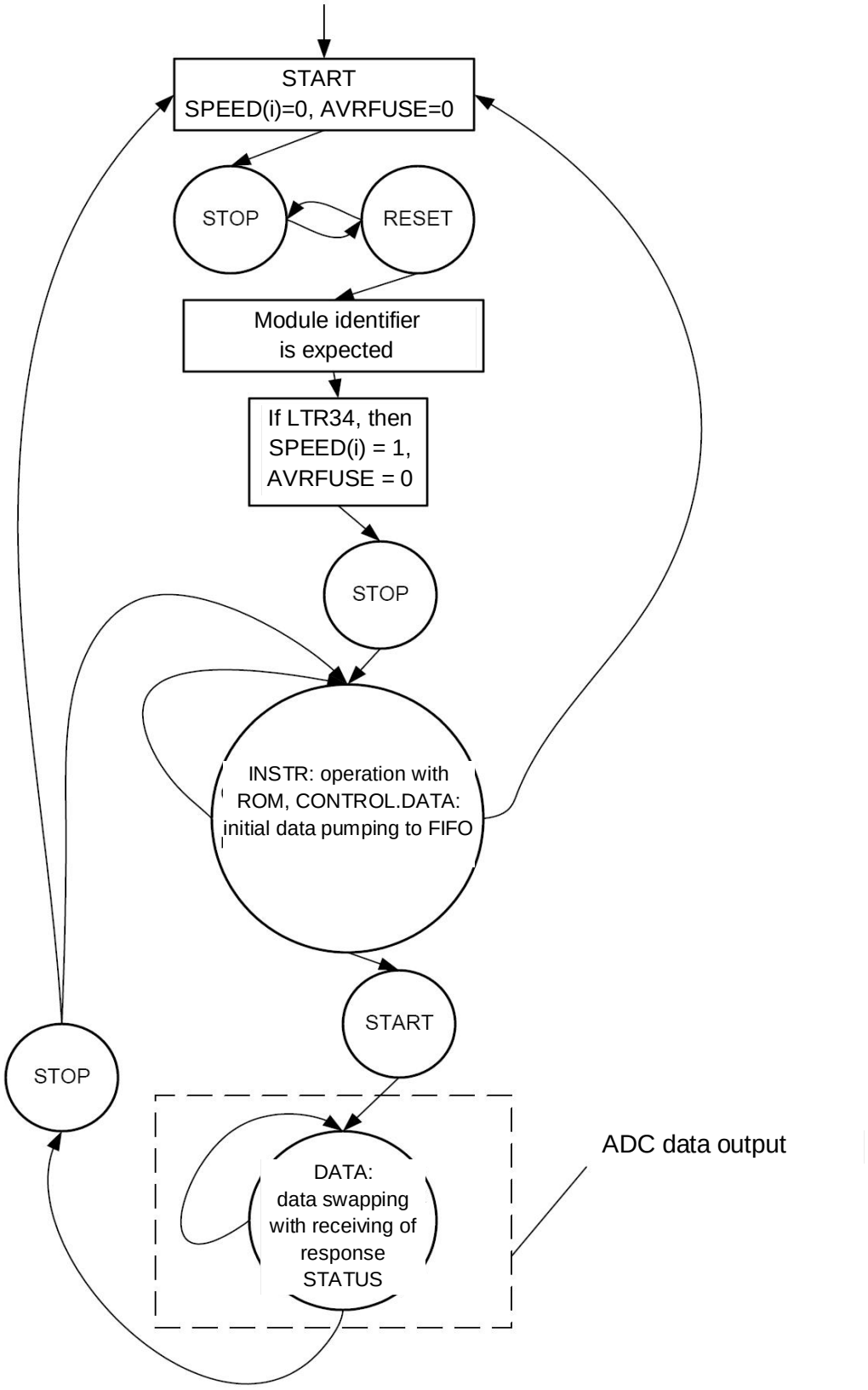


Fig.14-4. Graph. Permissible sequence of LTR34 commands

Chapter 15. LTR35 DAC module

15.1 Intended purpose

LTR35 is intended for high-quality 9-cahnnel signal reproduction. Among 9 channels: 8 channels for DC/AC voltage reproduction within the audio-ultrasonic frequency range up to 96 kHz (with a sampling rate of up to 192 kHz) and 1 channel for synchronous digital output (8 bits) with the same sampling frequency. There is a modification of LTR35 with only digital synchronous 16-bit output with a sampling rate of up to 192 kHz.

Areas of application: active acoustics and vibrometry, technological test oscillator, functional generator, technical systems for phase and frequency control. LTR35 in combination with LTR22, LTR24, LTR25 can be used for measuring through characteristics of audio, ultrasonic analogue paths within the signal dynamic range of more than 100 dB, as well as for testing DC voltage transmission paths. LTR35-2 modification can be used in ICP sensor signal imitation applications. The digital output channel can be used to generate synchronization signals with set time characteristics.

15.2 General description of LTR35.

LTR35 is a 8-channel DAC with the following specifications:

- DAC bit depth is 24 bits.
- DAC is a high-quality sigma-delta DAC with internal signal interpolation (PCM4104[1]) and an analog output active filter (no "steps" in the form of the signal at DAC output, extremely low inherent noise, interferencies and non-linear distortions). Maximum conversion frequency is 192 kHz.
- LTR35 modifications:

Modification	Number of DAC channels	Outputs of each DAC channel (output range)	Number of digital lines of parallel data output	Number of input digital lines
LTR35-1-8:	8	1:1 (±10 V) 1:5 (±2 V)	8	2
LTR35-1-4:	4	1:1 (±10 V) 1:5 (±2 V)	8	2
LTR35-2-8:	8	1:1 (-2...+20 V) 1:10 (-0.2…+2 V)	8	2
LTR35-3-0:	0	–	16	2

- Interpolating DAC allows to obtain high-quality sinusoidal signal of up to 96 kHz at output (even at a ratio of 2 points per signal period!) and allows reproducing signals in the frequency band from 0 to 96 kHz with high spectral fidelity.
- 32 MB buffer memory, FPGA Cyclone III, 8 MB Flash-memory on the board.

[1] Texas Instruments

- Active analog second-order LPF in each DAC channel for suppression of high-frequency noise.
- Wide dynamic range of DAC signal (more than 110 dB), high signal-to-noise ratio (about 100 dB).
- 4- or 8-byte per sample data format.
- Modes:

✓ Streaming 9-channel (8 analog channels + 1 digital channel). The streaming mode rate is limited to 400 or 200 thousand samples per second depending on the data format (4 or 8 bytes per sample, respectively).

✓ Cyclic autogenerator (8 analog channels + 1 digital channel) with the function of recording the next cyclic signal without interrupting the reproduction of the previous signal with switching to the next signal with an exact "matching" of its phase - up to 192 kHz for each channel.

✓ 4 independent "arithmetic" sources of the pair sinusoidal signal calculated in LTR35 FPGA. Each of the 4 sources can be set to its inherent frequency and initial phase. A sinusoidal (cosine) signal can be fed to any of the 8 channels of LTR34 from any of the 4 "arithmetic" sources while the remaining channels can operate either all in stream mode or all in a cyclic mode. Frequency of the arithmetic source can be controlled asynchronously "on-the-fly." Arithmetic sources have a 32-bit accuracy of angle setting and calculation.

✓ It is planned (at a second stage) to implement a sliding frequency mode (SWIP generator) in the FPGA firmware.

- Conversion frequency: up to 194 kHz per channel. Conversion frequency is controlled by a PLL with frequency grid setting in Hz units.
- 8 (16) digital outputs that can be used, for example, to generate pulses of the set phase and duration with a sampling period equal to the set DAC frequency (192 kHz maximum). Digital output is considered as the 9th output channel which can be operated in the same way as the rest of DAC channels (in the ring or streaming mode for all channels). LTR35-3-0 modification with 16 digital lines can also be used to generate an arbitrary flow or cyclic diagram.
- 2 external digital synchronization inputs.
- Output signal "on-the-fly" calibration using FPGA.
- Possibility to create a data output/acquisition synchronous system: LTR35 together with ADC of LTR22, LTR24, LTR25 for testing DC-AC paths.
- Galvanic isolation of all signal circuits at LTR35 connector relative to the case and the grounding circuit of the crate.

15.3 Overview of the hardware components and operation principles

A simplified block diagram for LTR35-1-8 is given in the figure below. 32 MB SDRAM-based data buffer has 8M x 32 structure. In LTR35, the data buffer can work in 2 alternative modes:

1) Ring 2-page mode (each page 4M x 32), allowing to record data from the reading page to the recording page during cyclic reproduction of DAC data. Upon the end of recording, LTR35 hardware receives the memory page changing command and waits until data reading process reaches the initial reproduction address and after that pages and records are swapped. **Ring 2-page mode allows, during reproduction of a signal from one memory page, to record the next cyclic signal to another buffer memory page.**

LTR35 will ensure the precise "gluing" of the old and new signal relative to the initial phase on the memory page changing command.

2) **Streaming mode where the whole space of the 8Mx32 buffer is used as a FIFO buffer implementing the "stream DAC" function with continuous data spooling from the upper software level** .

LTR35 asynchronous mode is considered as a stream mode option where the FIFO buffer is in the underrun state most of the time, and DAC outputs reproduce the last value recorded in this channel. This mode allows to set DAC outputs in the required state from time to time without strict time referencing of such setting.

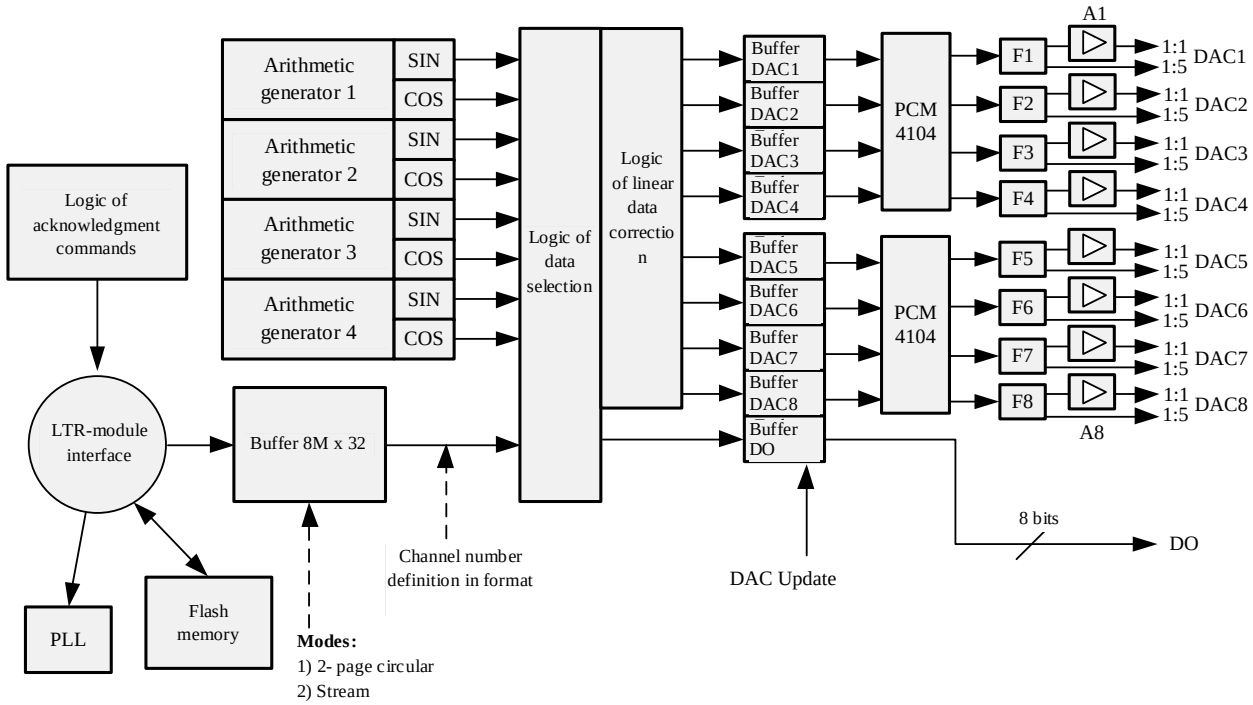


Fig.15-1. LTR35-1-8. Block diagram.

Physical channel number from 1 up to 9 and data report assigned for it are always recorded in the 32-bit data buffer in any LTR35 mode. Channel numbers from1 up to 8 correspond to respective DAC channels, and channel with number 9 corresponds to the digital output. In the process of data reading from the buffer, LTR35 hardware always analyzes the channel number to record a sample in the output register of the respective buffer channel (DAC1…8 buffer, DO buffer). DAC output update signal generation (DAC Update) is set "upon reading of the desired channel number from the buffer" that allows to consider the data sample with this channel number as a sample after the receipt of which DAC outputs (and DO outputs) will be updated.

LTR35 contains four "arithmetic" signal generators, each of which calculates new sine and cosine values including programmable initial phase and phase increment from sample to sample during one DAC conversion period. The bit depth of setting the initial phase and increment of angle is 32 bits and the bit depth of calculated sine-cosine is 24 bits. Each of 4 "arithmetic" generators can be set independently in its initial phase and frequency.

The *Data selection logic* allows for strict signal source assigning to each output of 9 channels (DAC1…8, DO): either the data buffer or sine/cosine of one of 4 arithmetic generators.

The linear data correction logic allows for setting the scale and zero offset for the relevant DAC1…8 output not only with account for calibration factors but for the desired amplitude and zero offset at DAC1…8 outputs.

In 8 MB Flash-memory, calibration factors, FPGA firmware, serial number of the product and other process data are stored.

Frequency synthesizer (PLL) allows to obtain the required conversion frequency (output frequency for DO digital output) for all LTR35 channels. PLL is synchronized with the *single reference generator of LTR* crate (Appendix A.16, page 359). The recommended conversion frequency of 192 kHz is the maximum permissible conversion frequency for each LTR35 DAC channel. LTR35 functionality allows for obtaining a conversion frequency from 24 kHz to 192 kHz (but in the first SW implementation the fixed conversion frequency is of 192 kHz has been implemented).

Output registers "DAC1…8, DO buffers" always save the last recorded state.

The digital output channel in LTR35 architecture is conventionally considered as the "9th DAC channel-", and data are output synchronously with the rest of DAC channels to the digital output (with the accuracy of fixed output delay, paragraph 15.3.1, page 241)

"By default", the voltage at DAC outputs is close to zero, and DO outputs are swtiched over to Z-state. For certainty of the initial state of the control digital lines, it is assumed that the *external user circuit of digital line load should contain pull-up resistors to logical "zero" or "one"*. Z-state of the outputs is controlled simultaneously for 8 outputs, and Z-state control bits are coded in each data sample format, paragraph 15.3.2, page 241.

Unlike LTR35-1-8, LTR35-1-4 modification has only 4 outputs from DAC1 to DAC4 and one 4-channel PCM4104 converter instead of two.

Second-order active anti-aliasing filters with upper cutoff frequency of about 250 kHz are connected to the outputs of PCM4104 converter. These anti-aliasing filters suppress high-frequency noise effectively. The signal is sent to output 1:5 of this channel (±2 V) from the anti-aliasing filter output and to the respective amplifier (A1…A8) with the voltage transfer ratio of 5 which output 1:1 provides the signal reproduction range within ±10 V.

LTR35-2-8 modification differs from LTR35-1-8 with the voltage transfer ratio of 10 amplifiers (A1…A8) and with the asymmetric signal output range at outputs 1:10 (-0.2…+2 V) and outputs 1:1 (-2...+20 V).

LTR35-3-0 modification differs from LTR35-1-8 with absence of analog channels DAC1…DAC8; the number of output digital lines in LTR35-3-0 is expanded to 16 (the most significant byte with independent control of the most significant byte Z-state is added).

15.3.1 Output delay at DAC outputs relative to DO output.

This delay is generally determined by the group delay of PCM4104 equal to 29 DAC conversion periods. This delay can be taken into account in software, if required.

15.3.2 Control of Z-state of DO outputs.

In addition to the less and most significant byte data, there are two active state enable bits of the less and most significant byte output in the data sample format of the 9th physical channel (digital output). These signals control digital outputs during this sample reproduction directly, with one essential point: output enable of about 50 nanoseconds is delayed relative to the data sampling time that automatically ensures correct output switching from Z-state to "1" or "0". However, when programming the switching from the active state to Z-state for the i-th sample, it is necessary that the previous data state be saved in the i-th sample format with simultaneous setting of output restriction in the i-th data sample format.

15.3.3 Convention for calibration of DAC outputs 1:1/1:5 or 1:1/1:10.

Each channel of LTR35 has pair outputs 1:1/1:5 or 1:1/1:10 depending on LTR35 modification. LTR35 hardware provides about 1% accuracy of signal ratio at pair outputs 1:1/1:5

or 1:1/1:10 of the respective DAC channel. The purpose of the convention for calibration of DAC outputs 1:1/1:5 or 1:1/1:10 is that the current data correction operation based on the calibration factors should be applied to one of the pair DAC outputs that the user is connected to (LTR35 accuracy characteristics are given in Appendix A.13, page 350).

However, this convention does not exclude simultaneous using of the second pair output at which uncalibrated voltage will be present with about 1% accuracy (for direct current volatge) relative to the expected voltage.

15.4 LTR35 project development.

LTR35 product is in its nature a "to grow into" project. Rich unutilised resources of FPGA Cyclone III provide the possibility of implementing additional necessary service functionality (as respective orders are received).

15.5 Connection of signals

Read the general rules for signal connection, paragraph 3.6.6, page 58.

LTR35 module has DRB-37M panel-mount connector for connection of input signals. External connections to LTR35 should be implemented by connecting signal circuits to the cable part of the connector (DB-37F type). Application of signals is given in

table16-2, and the view of the panel-mounted connector is presented in fig.15-2.

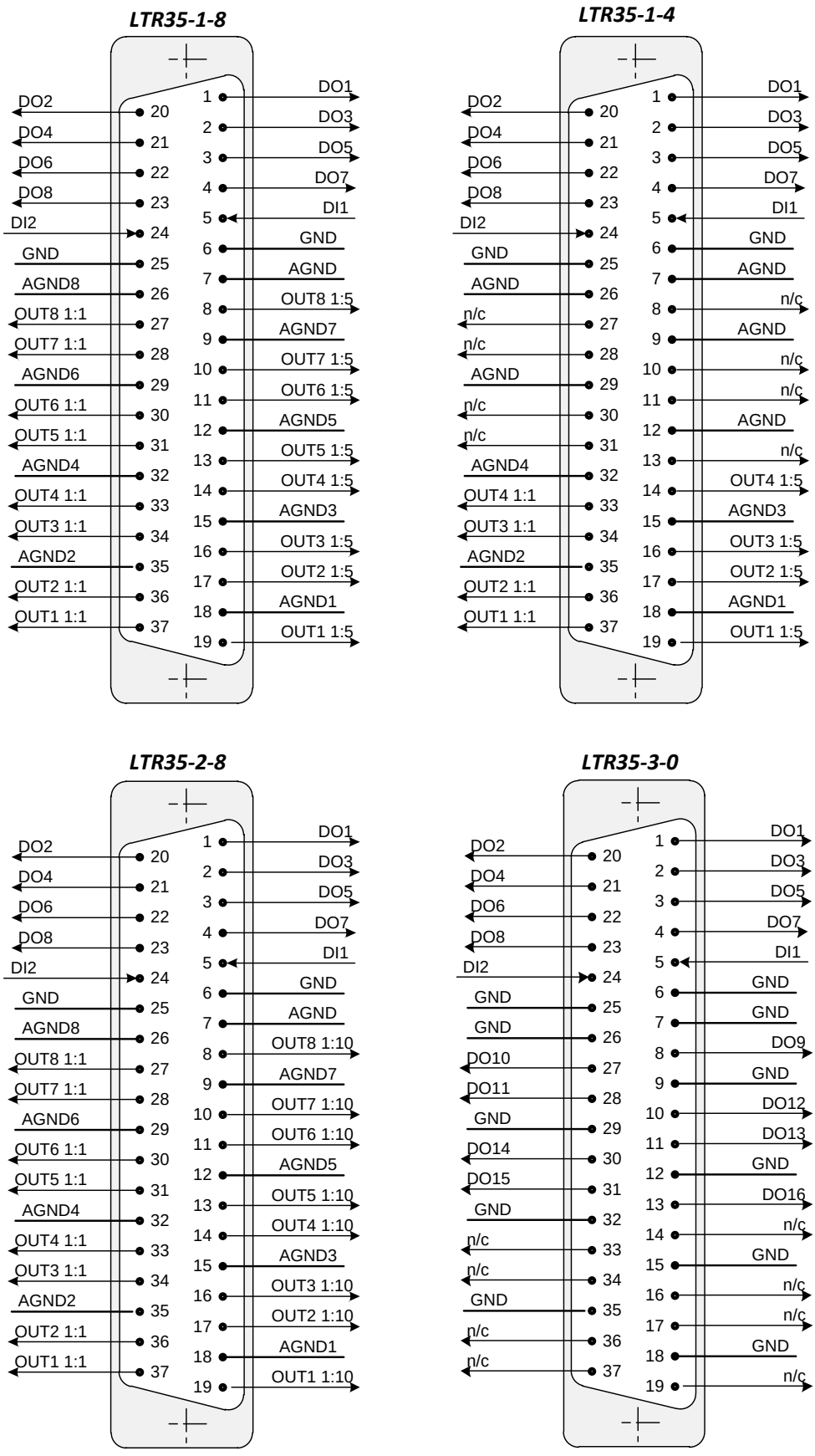


Fig.15-2. LTR35 connector contacts.

Table15-1. Description of user connector signals for LTR35

Signal name	Common point	Direction	Description
OUT1 1:1 ... OUT8 1:1	AGND1 ... AGND8	Output	DAC channel outputs 1:1 from 1 to 8. For LTR35-1, the output voltage range is ±10V. For LTR35-2, the output voltage range is −2…+20 V
OUT1 1:5 ... OUT8 1:5	AGND1 ... AGND8	Output	DAC channel outputs 1:5 from 1 to 8. The output voltage range is ±2 V
OUT1 1:10 ... OUT8 1:10	AGND1 ... AGND8	Output	DAC channel outputs 1:10 from 1 to 8. The output voltage range is −0.2…+2 V
DO1 ... DO8	GND	Output	Digital parallel outputs (the less-significant byte) with common output enable control. The outputs have initial Z-state. Output digital levels are 0-3.3V. In the powered-off state, the outputs continue to be in the high-impedance state within the operating voltage range. Output lines resistance is 100 Ohm.
DO9 ... DO16	GND	Output	Digital parallel outputs (the most-significant byte) with common output enable control. The outputs have initial Z-state. Output digital levels are 3.3 V. In the powered-off state, the outputs continue to be in the high-impedance state within the operating voltage range. Output lines resistance is 100 Ohm.
DI1 … DI2	GND	Input	Digital multi-function inputs with input levels of 3.3 V.
AGND1 ... AGND8	–	–	"Common wire" circuits for connection of output load circuits of the respective channel (paragraph 15.5.3)
AGND	–	–	"Analog ground" circuit for connections not associated with any specific channel load currents (paragraph 15.5.3)
GND	–	–	"Digital ground" circuit for connection of load current circuit of DO digital outputs (paragraph 15.5.3)

15.5.1 Characteristics of signal line inputs and outputs

! When connecting LTR35 module to your system, strictly observe the parameters specified in tables of this section.

The manufacturer shall not be warranty liable for LTR35 failure caused by violation of maximum permissible operation conditions .

The characteristics of galvanic isolation in LTR are given in Appendix A.18, page 362.

The following abbreviations are used in tables of this section:

AO – analog output

DI – digital input.

DO – digital output.

15.5.2 LTR35 maximum permissible conditions

LTR35 module installed in LTR crate has the following characteristics of input and output signal lines after LTR crate is powered on:

Table15-2. Maximum permissible conditions

Signal	Type	Operating conditions	Maximum permissible conditions
OUT1 1:1 … OUT8 1:1	AO	LTR35-1: less than 10 mA for each output	LTR35-1: 20 mA for each output under the condition that the total current [1]for all LTR35 outputs does not exceed 160 mA. LTR35-2: 12 mA for each output under the condition that the total current[2]for all LTR35 outputs does not exceed 96 mA. Outputs are resistant to a short-time short circuit on AGND Short circuit of more than two analog outputs is inadmissible.
OUT1 1:5 … OUT8 1:5 OUT1 1:10 … OUT8 1:10	AO	less than 10 mA for each output	20 mA for each output under the condition that the total current for all LTR35 outputs does not exceed 160 mA. Outputs are resistant to a short-time short circuit on AGND Short circuit of more than two analog outputs is inadmissible.
DI1 … DI2	DI	0…+3.3 V	Maximum permissible voltage at input -5…+7 V
DO1 … DO16	DO	Less than 8 mA for each output	Maximum permissible voltage at output is -0.5…+6.5 V. Peak current is max. 20 mA.

15.5.3 AGND, AGND1…AGND8, GND circuits and their connection.

It should be noted at once that the circuits AGND, AGND1 ... AGND8, GND are interconnected inside the LTR35 module. At the same time, all contacts at any LTR module connector are isolated relative to the crate frame and grounding circuit.

LTR35 contains different voltage sources (analog (DAC) and digital (DO) output signals) with "common wires" which are interconnected inside LTR35 module. To minimize the mutual influence of external load circuits of these sources, the principle of maximum separation of current loops of load circuits should be followed (L. [2], page367) . In other words, if it is possible to separate current loops in the load circuit of each analog or digital output in load circuits that you are

[1] Here and elsewhere in this table: sum of currents is taken per module without accounting for current direction.

[2] Here and elsewhere in this table: sum of currents is taken per module without accounting for current direction.

going to connect to LTR35, then these load circuits should be connected relative to AGND1 ... AGND8 circuit of the corresponding LTR35 DAC output or relative to GND which is common for all digital outputs. If the "common wire" connection is not associated with the current loop of particular analog output, it is recommended to engage AGND circuit. We separate the names of AGND, AGND1…AGND8, GND circuits to solve the task of separating load circuit current loops even though they are short-circuited inside LTR35. If current loops can not be separated, then it is recommended to connect AGND circuits of the respective channel at LTR35 connector. Note that in the event when current loops of analog and digital load circuit can not be separated, this event is the most critical in terms of possible influence of digital output circuits on analog ones.

Chapter 16. LTR114 universal high-precision ADC

! Here you can find the preliminary information about LTR114 module.
Certification of this product as part of LTR is planned.

16.1 General description of LTR114.

Fig.16-1. LTR114 module. View.

16.1.1 Device application

LTR114 is intended for high-precision digitization of signals with ADC conversion frequency of up to 4 kHz in a wide voltage range: *from millivolt signal sources to 10-volt ones*, measuring the resistance of *single strain gauges and thermistors* (quarter-bridge circuits) with the use of an *internal current source*. Connection of full-bridge *sensors to an external power source is possible*.

In particular, LTR114 is intended for low-temperature measurements with the use of thermistors. *The method of switched (interruptible) current supply to measuring channels allows to set LTR114 thermistor for ultra-low power dissipation values.*

LTR114 is adapted for operating not only with closely located signal sources but with those located at distances of tens of meters.

LTR114 channels can be flexibly configured for measuring voltage or resistance due to the unique LTR architecture based on 24-bit ADC and 16-channel switch.

For users familiar with LC-114 and LC-116 modules in LTC system (now discontinued), new LTR114 module is not only a functional substitution of [1]LC-114 and LC-116 for tasks involving

[1] Full compatibility with LC-114, LC-116 modules connector contacts is not provided.

measurement of resistance of quarter-bridge circuits but also an extended versatility as compared to its predecessors.

16.1.2 General information about LTR114

LTR114 module has the following functions:

- 24-bit 4 kHz ADC has a differential input with dynamic switching option for up to 16 -channels, with ±10 V, ±2 V, ±0.4 V input subranges specified by software independently for each channel.
- Resistance measurement with dynamic switching of up to 8 channels using a 4-wire diagram (up to 8 channels may serve as a switchable current source for a 4-wire resistance measurement diagram). Resistance measurement ranges: 0÷400 Ohm (at I=1.0 mA), 0÷1200 Ohm (at I=0.33 mA), 0÷4000 Ohm (at I=0.1 mA). Resistance measurement modes: - standard mode (up to 4 kHz), − alternating reference current mode (up to 2 kHz).
- Basic reduced measurement errors: 0.01% for voltage measurement, 0.03% for resistance measurement.
- Set ADC frequency of up to 4 kHz is divided between the polled voltage and resistance measurement channels according to the cyclic order of the channels polling pre-recorded in the control table for up to 128 channel numbers.
- LTR114 implements the following possible ratios between the numbers of voltage/resistance measurement channels: 16/0, 14/1, 12/2, 10/3, 8/4, 6/5, 4/6, 2/7, 0/8 (of course, smaller numbers of measurement channels in the above-mentioned pairs are also implementable)
- Auxiliary service function: check for a breakage or short circuit of external signal lines
- Functions of the external universal interface line: - Support of the "1-wire" interface (in particular, for DS18S20 **external temperature sensor** for determining the "cold junction" temperature). - Synchronization of data acquisition among several LTR114 modules based on the "master-slave" principle.
- When data acquisition is disabled, a procedure of check for breakage or short circuit of external signal lines can be carried out for all LTR114 channels. In particular, this function is required when multi-channel measuring systems (test stands) are used as built-in equipment for testing the operability of the lines from the sensors.
- Unlike its predecessors (LC-114, LC-116 modules), LTR114 implements current switching by measured resistance strain gauges and thermistors. The overall switching at LTR114 input is performed using modern analog switches with low charge injection causing relative low switching inaccuracy of measurements. At the same time, the unstable nature of current passage via a measured resistor significantly reduces measurement errors related to its heating. In particular, this fact is critically important for low-temperature measurements.

16.1.3 LTR114 module configuration

The basic configuration of LTR114 is described in paragraph 2.4, page 29.

16.2 Overview of the hardware components and operation principles

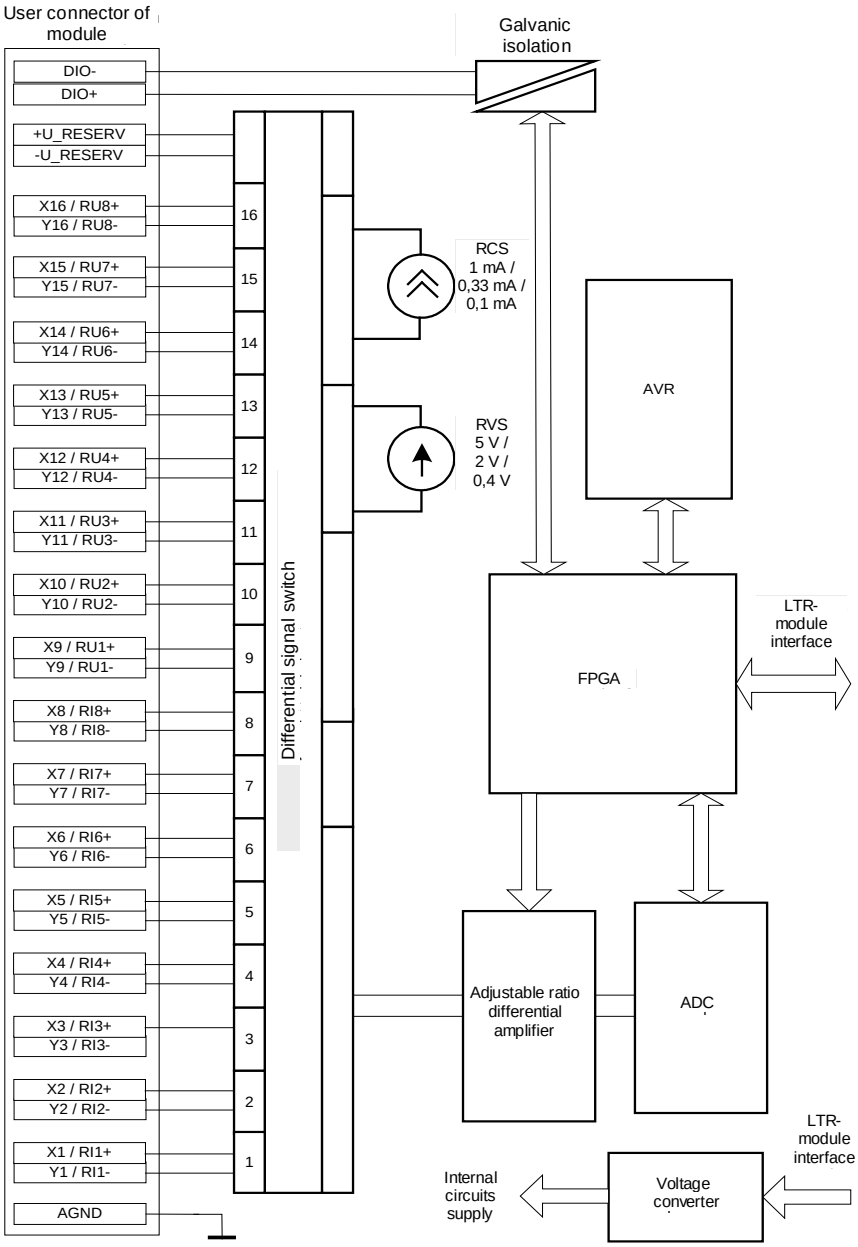


Fig.16-2. LTR114 block diagram

16.2.1 Block diagram.

LTR114 (fig.16-2) block diagram comprises:

- 37-pin user connector (the description is given in table16-2, fig.16-4)
- Differential signal switch
- Reference voltage source (RVS) with controlled output voltage of 4.2 V, 2 V, 0.4 V
- Reference current source (RCS) with controlled output current of 1 mA, 0.33 mA, 0.1 mA
- Differential amplifier with regulated transmission ratio

- LTC2440-type ADC[1]
- ATMEGA128 AVR controller[2] (there is the possibility of user firmware update in accordance with official updates of L-Card)
- FPGA with hard control logic (no external loading required, not user-updated)
- Local unit of DIO-, DIO+ universal digital line galvanic isolation
- Galvanically isolated LTR module interface with control signals and power circuits.
- Internal supply voltage converter
- Control unit of signal circuits (not shown in Fig. fig.16-2). Its equivalent diagram is described in paragraph . 16.4

16.2.2 General principle of operation.

16.2.2.1 Reference voltage and current sources

RVS and RCS are high-stable sources of voltage and current serving as a "metrological base" for this module. During LTR114 verification in L-Card[3], precise RVS (4.2 V, 2 V, 0.4 V) and RCS (1 mA, 0.33 mA, 0.1 mA) indications are measured at signal connector pins and recorded in AVR controller non-volatile memory.

During normal *voltage measuring*, if the auto-calibration mode is set, LTR114 module uses module RVS for test measurements and reconciles ADC code readings with the recorded RVS voltage value.

During normal *resistance measuring in a* 4-wire circuit, RCS supplies current to the current circuit and LTR114 measures voltage in the voltage circuit using RVS for checking readings in the auto-calibration mode.

Internal RVS voltages 4.2 V, 2 V, 0.4 V can be measured using an external high-precision voltmeter with input resistance of min. 10 GOhm and an isolated input. The external voltmeter can be connected to pins 22 and 3 of the signal connector (REF-, REF+ circuits, respectively). LTR114 must be set for a corresponding program mode for occurrence of RVS voltage at these pins.

RCS current can be measured directly in the current branch of a 4-wire resistance measuring circuit within the corresponding resistance subrange (actually, test ampere gauge is used on instead of a measured resistor). It is significant that internal resistance of the test ampere gauge should not exceed the corresponding value of LTR114 resistance measuring subrange.

16.2.2.2 ADC features

LTR114 block diagram is based on a 24-bit sigma-delta ADC with programmable data acquisition frequency to resolution ratio. It is important to note that, unlike other sigma-delta ADCs (for example, applied in the LTR22 module), the internal filter setting period in LTC2440 ADC does not exceed one data acquisition period. This feature has made it is possible to implement a block diagram with input channel switch operating at ADC data acquisition frequency.

ADC resolution depends on the programmable *OSR* factor (oversampling rate) which can be set from the range of 64, 128,256, 512, 1024, 2048, 4096, 8192, 16384, 32768. In this case, ADC conversion time T_{CONV} (in milliseconds) is determined according to the formula

[1] Linear Technology Corporation

[2] Atmel Corporation

[3] or in the relevant accredited organization

$$T_{CONV} = \frac{40 * OSR + 170}{F_0}$$

Here F_0 is set in kilohertz and can have a value of 15,000 kHz or 7,500 kHz (the frequency F_0 is programmed).

The higher *OSR value is set*, the larger is the effective number of ADC significant bits.

Implemented period of acquisition of the 1st data sample T_{ADC} must always exceed the ADC conversion T_{CONV} time.

Time $T_{ADC} - T_{CONV}$ is the time allotted to the establishment of the transient process after switching in the input lines. The longer is the length of the cable connected to LTR114 and the higher is the internal resistance of the signal source, the more time it will take to establish the transient process in the input lines. Hence, time $T_{ADC} - T_{CONV}$ can make an effect on the inter-channel passage value.

During the *internal synchronization* of LTR114, the data collection period is set in software, while the acquisition frequency is T_{ADC} the product of division of the frequency $F_{ADC} = \frac{1}{T_{ADC}}$ of the single reference generator of LTR crate (Appendix A.16).

During *external synchronization* (from a synchronization pulse on DIO line), the minimum value of the data acquisition period is 250 μs, and the maximum period (from the hardware point of view) is not defined[1].

ADC conversion path AFC depends directly on OSR and F_0 programmable parameters. Based on fig.16-3, this AFC has salient minimums (filter zeroes) at points F_n on the frequency axis. Dependence on F_n OSR and F_0 is defined by the formula (frequencies F_n and F_0 are given in Hertz here):

$$F_n = \frac{F_0}{5 * OSR}$$

Basic frequency spectrum of LTR114 ADC and converter parameters interrelations are summarized in table 16-1. If necessary, many other parameter combinations F_0, OSR, F_{ADC} may be used to create a narrower frequency spectrum with other combinations of characteristics F_n and $T_{ADC} - T_{CONV}$. These options are provided to the user *at the level of library functions*.

From a practical perspective, it is obvious that frequency F_{ADC}=5 Hz $F_n = 46$ Гц) is he most useful because signal interferences will be suppressed to a significant extent at circuit frequency of 50 Hz and at divisible circuit frequencies.

[1] from the software point of view, the maximum data collection period can be practically limited by preset time-out values in the upper-level library functions.

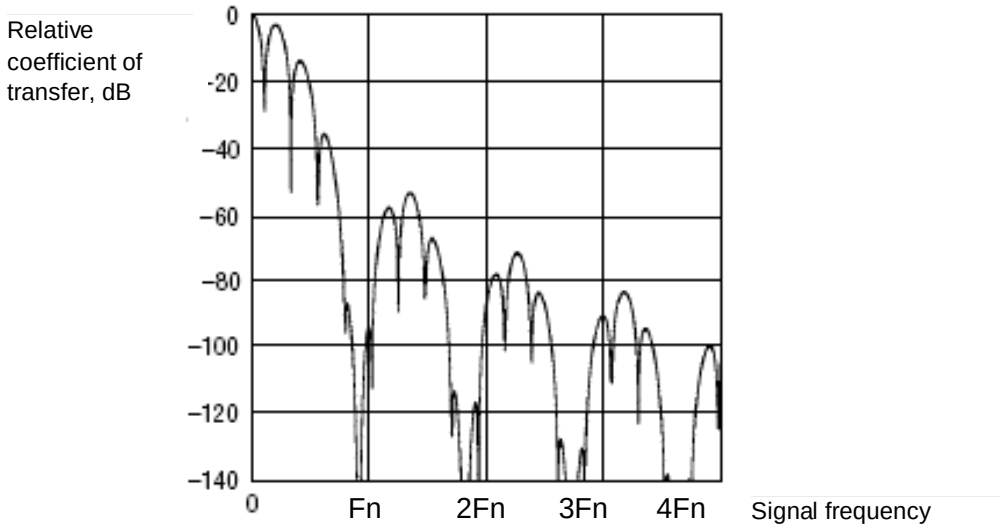


Fig.16-3. AFC

Table 16-1. LTR114. Basic ADC frequency spectrum and parameter interrelations

F_{ADC}, Hz	OSR	T_{ADC}, ms	T_{CONV}, ms	$T_{ADC} - T_{CONV}$	F_0, kHz	F_n, Hz
4,000	64	0.25	0.18	0.07	15,000	43,956
2,000	128	0.5	0.35	0.15	15,000	22,684
1,000	256	1	0.69	0.31	15,000	11,527
500	512	2	1.38	0.62	15,000	5,811
200	1,024	5	2.74	2.26	15,000	2,918
100	2,048	10	5.47	4.53	15,000	1,462
50	4,096	20	10.93	9.07	15,000	732
25	8,192	40	21.86	18.14	15,000	366
16	16,384	62.5	43.7	18.8	15,000	183
8	32,768	125	87.39	37.61	15,000	92
5	32,768	200	163.86	36.14	7,500	46

When LTR114 is used in the multi-channel mode (as well as in the continuous auto-calibration mode), the data acquisition frequency in an individual channel will be divided frequency F_{ADC} depending on multiple poll divisibility of this channel within a data acquisition frame and on set inter-frame delay value. Let us consider in more detail the issues related to switching, auto-calibration modes, and frame-by-frame data acquisition arrangement.

16.2.2.3 Input switch and switching capabilities

Electronic switch (fig.16-2) is used for switching of:

- differential voltage measuring signals from LTR114 module user connector (from a selected channel) to the differential input of an amplifier;
- RCS output to the current circuit of a 4-wire current measuring circuit of the selected measuring channel.
- RVS voltages in both polarities (and inherent zero voltage) to the amplifier input to enable the auto-calibration function during voltage measuring;

- test current supply for checking the operability of input lines.

LTR114 module has 16 physical differential measuring channels, numbered from 1 to 16.

Channels 1-8 of LTR114 module serve as a differential ADC input and alternatively as a switched current source to measure resistance in a 4-wire connection diagram (any channel can be set for this function).

Channels 9-16 of LTR114 module serve as a differential ADC input and alternatively as a voltage meter in a 4-wire resistance measuring diagram.

Each pair of channel numbers listed below can be used either in a 4-wire resistance measuring diagram or as two independent ADC inputs: 1-9, 2-10, 3-11, 4-12, 5-13, 6-14, 7-15, 8-16. Other combinations of physical channels in a 4-wire measuring diagram are impossible. This means that LTR114 implements the following number of voltage/resistance measuring channels ratios: 16/0, 14/1, 12/2, 10/3, 8/4, 6/5, 4/6, 2/7, 0/8 (of course, smaller numbers of measurement channels in the above-mentioned pairs are also implementable).

16.2.2.4 Auto-calibration modes

LTR114 supports the following auto-calibration modes:

- **One-time auto-calibration at the start of data acquisition**. In this mode, ADC readings are automatically reconciled with RVS only once at the moment of start of data acquisition. This mode allows for further data collecting with zero inter-frame delay (perhaps, to obtain the maximum frequencies of data acquisition). However, to compensate the temperature and long-time instability of LTR114 and ADC analog path in this mode it is required to restart data acquisition after long operation or after sharp changes in temperature conditions.
- **Continuous auto-calibration**. In this mode, ADC readings are automatically reconciled with RVS on a continuous basis, but for this purpose the user must set at least one period of inter-frame delay. Using the inter-frame delay, LTR114 will consequently reconcile the readings with RVS in each voltage measuring subrange. In this mode, device temperature error is minimal.

It is important to note that LTR114 hardware itself and AVR controller do not perform any arithmetic data processing (uncorrected ADC codes are fed from LTR114 module to the LTR interface), and data correction is performed by the upper-level library functions (but, in principle, the data correction feature can be implemented at the level of LTR-EU crate controller based on Blackfin processor, if the data processing process should be closed at the crate controller level for implementation of real-time algorithms).

High-level data correction procedure uses calibration factors read from LTR114 stored in the flash memory of the AVR controller and recorded by the manufacturer during verification (factory calibration). Calibration factors are RVS and RCS values within all subranges (paragraph 16.2.2.1).

16.2.2.5 Frame-by-frame data acquisition arrangement

Traditionally, in all ADCs with channel switching functionality (for example, in LTR11) **L-Card** uses frame-by-frame principle of physical channels polling arrangement with controlled inter-frame delay . In LTR114, *frame size can be* set within the range from 1 to 128 ADC samples. This means that the user can record his own channel polling sequence in the *control table* with the set size from 1 to 128 channel numbers prior to the start of data acquisition. When each next data sample is collected, the internal control logic of LTR114 input switch polls the control table from the first number to the last one (and then to the first one in the cycle) and sends the corresponding control signals to the switch processing the specified channel polling sequence.

To obtain more opportunities for ensuring low data acquisition frequencies in an individual physical channel, an inter-frame delay method is used in LTR114. Channels polling for set zero inter-frame delay is carried out exactly as described above. For non-zero inter-frame delay following polling of the last channel number from the control table (i.e. at the end of frame), set number of delays is inserted before the first number polling (each delay is equal to set ADC start frequency period). For LTR114, this inter-frame delay is used for internal mechanism of *continuous auto-calibration*, if this mode is set.

Inter-frame delay can be set within the range from 0 to 65535 ADC conversion cycles.

16.2.2.6 Alternating resistance measuring mode

This mode is traditionally used for compensation of thermal electromotive force of external circuit contact connections (for example, a similar mode is used in LTR212(M)). The sense of this mode is simple: for a short time (during which the temperature mode can be considered steady), two consecutive measurements of resistance are carried out for current of the same magnitude but of the opposite direction, and then the obtained result is averaged.

To implement this mode, two consecutive measurements of the same channel within the same range but for currents of different directions should be included in the control table of LTR114 (the issue of data averaging at the upper level is discussed in the programmer's manual[1]). As a consequence, the measurement accuracy will be increase but the frequency of data acquisition on the resistance measurement channel will be decreased.

16.2.2.7 Multi-frequency mode.

The control table with size of up to 128 logic channels allows to set different divisibility of physical channels polling within a frame. For example, if physical channels are written in a control table for 4 channels as follows: 1,2,1,3. The data can be received for channel 1 twice as fast as for channels 2 and 3.

16.2.2.8 Power dissipated with a thermistor.

In particular, LTR114 is intended for low-temperature measurements with the use of thermistors. The method of switched (interruptible) current supply to measuring channels allows to set LTR114 for ultra-low power dissipation values at the thermistor. Let us further consider the issue of dissipated power calculation.

If I is current passing through the thermistor (0.1 mA, 0.33 mA or 1 mA), R is thermistor resistance (Ohm), n is number of polls of this channel within the frame (from 0 to m ADC conversion periods), m is set poll size from 1 to 128 ADC conversion periods, d is inter-frame delay set mode from 0 to 65535 ADC conversion periods, then the average power (W) dissipated at the thermistor is calculated according to the formula:

$$P = I^2 R \frac{n}{m + d}$$

Naturally, this averaged assessment should be used when the sensor temperature time constant exceeds the ADC set period $T_{ADC} = \frac{1}{F_{ADC}}$. In particular, thermosensors of some types will become overheated for a period of 200 msec (5Hz ADC frequency), therefore, in this case the ADC frequency should be increased.

16.2.2.9 Working with thermosensor DS18S20

The data acquisition logic from external digital thermosensor is independent from the ADC data acquisition logic. AVT controller in LTR114 working in the background low-priority mode implements DS18S20 polling diagram sending the obtained temperature measurement samples to LTR-module interface in a specific format allowing for logical separation of temperature samples

from other data. The controller sends temperature measurement samples to LTR interface as they become available, implementing a quasi-periodic data acquisition mode with average polling period of approximately 1 second. Temperature detector connection is considered in paragraph 16.3.8.

16.2.3 Module LTR114 control

Module control as related to main interface commands STOP, RESET, PROGR, INSTR (paragraph 4.6.3) is the same as in other LTR modules with AVR controller, for example, LTR11 (paragraph 5.3.3.1). Specific control commands at the library functions level are described in the *Programmer's Manual*[1].

16.3 Connection of signals

Assignment of LTR114 connector contacts is given in fig.16-4. Symbol "/" divides alternative functions of signals preset by the module software configuration (prior to the start of data acquisition). A brief description of all signals functions is given in

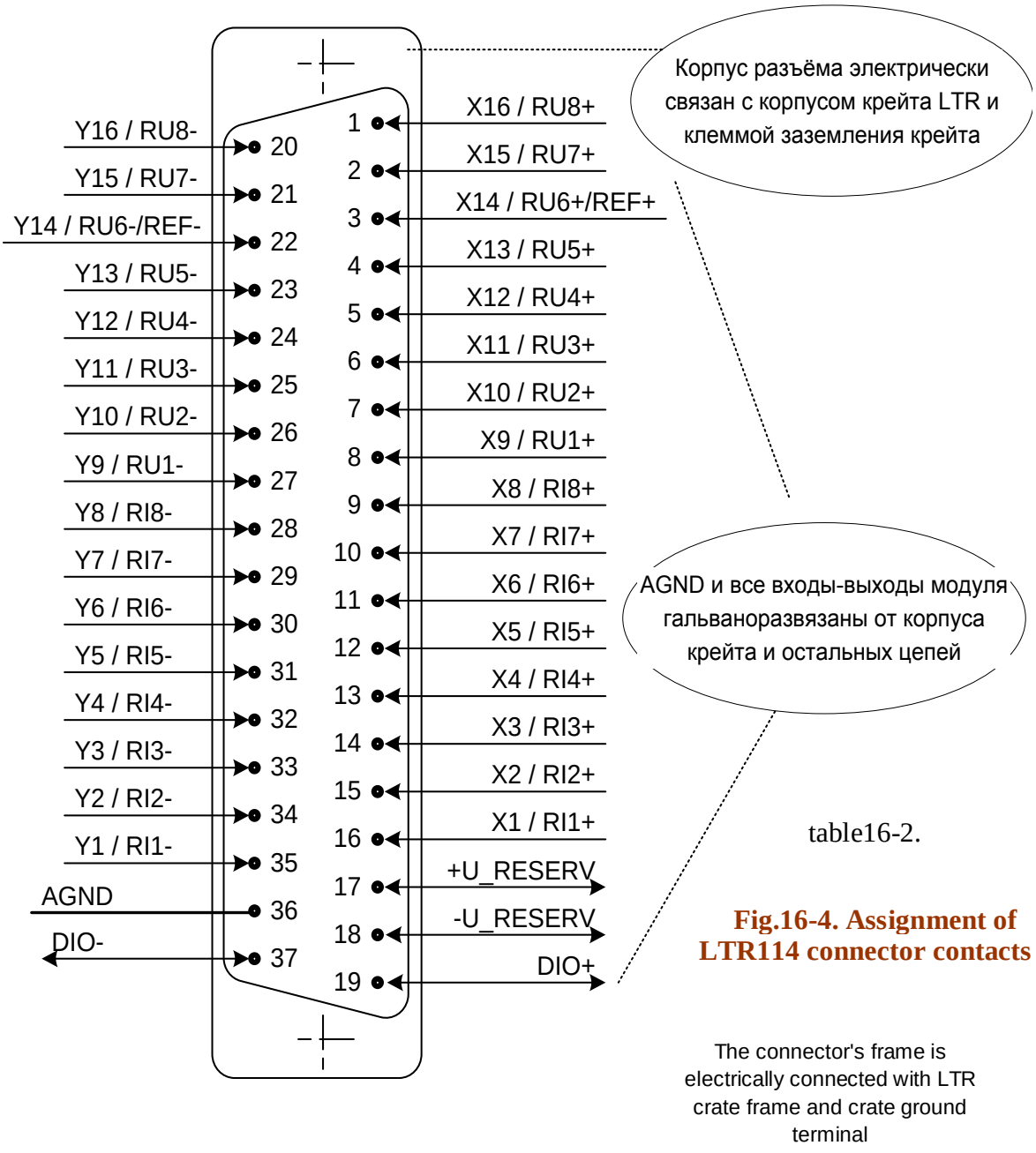


table16-2.

Fig.16-4. Assignment of LTR114 connector contacts

The connector's frame is electrically connected with LTR crate frame and crate ground terminal

Table16-2. Description of user LTR114 connector signals

Signal name	Common point	Direc-tion	Description
X1, X2,…,X16 Y1, Y2,…,Y16	AGND	Input	Pairs of circuits (X1, Y1), (X2, Y2)… (X16… Y16) form 16 differential inputs for voltage measurement mode. Accordingly, X1,…, X16 are non- inverting, and Y1,…, Y16 are inverting circuits of differential inputs. Number of input (from 1 to 16) corresponds to the actual number of LTR114 input. Operating range of signals on X_i and Y_i is ±10 V relative to AGND common wire circuit for 16 dif-ferential inputs. Moreover, the information component of the differential signal (voltage separation between Y_i and X_i) has an operating range of ±10 V.
RI1– RI2–,..., RI8– RI1+, RI2+,..., RI8+	absent	Output	Pairs of circuits (RI1–, RI1+), (RI2–, RI2+),…, (RI8–, RI8+) form the poles of 8 current circuits of 8 measured resistors. Each resistor (from 0 to 4 kOhm) must be connected to RI_i–, RI_i+, RU_i–, RU_i+ circuits in 4-wire diagram
RU1–, RU2–,..., RU8– RU1+, RU2+,..., RU8+	absent	Input	Pairs of circuits (RI1–, RI1+), (RI2–, RI2+),…, (RI8–, RI8+) form the poles of 8 voltage drop measurement circuits for 8 measured resistors. Each resistor (from 0 to 4 kOhm) must be connected to RI_i–, RI_i+, RU_i–, RU_i+ circuits in 4-wire diagram
DIO+	DIO-	Input-output	Electrically isolated "single-wire" interface which can be used for alternative types of connection of the following devices: -external temperature detector DS18S20; -other LTR114 modules in order to integrate them into a single synchronous diagram on a "one master- several slaves" basis; -external TTL output of signal from which ADC conversion frequency can be synchronized; -external TTL input of the device recording the moments of internal initiation of ADC conversion.
+U_RESERV -U_RESERV	AGND	Input-output	Circuits for implementation of a redundant diagram of connection of 2 LTR114 modules to the same signal sources, see fig.16-8.
REF+ REF–	AGND	Output	Control output of internal reference voltage sources of LTR114 (is used during LTR114 calibration and verification). This output is not used during the normal operation.

16.3.1 General connection case

An example of measuring circuits connection is given in fig.16-5. Here, four differential (2-phase) voltage sources U1-U4 are connected to channels 1-4; four measuring resistors (physical channels 13-16 are also engaged in the 4-wire diagram) are connected to channels 5-8; four single-phase (with common grounding) voltage sources U5-U8 are connected to channels 9-12. A 2-wire connection of digital DS18S20 temperature detector is also shown.

LTR114 provides an essential possibility to connect a group of non-isolated measuring resistors with a common wire circuit (connection point *C* on fig.16-5). It is significant to note that the *C* point must be isolated from other circuits (including AGND). Such type of connection is used only in a special case when measuring resistors for any reasons already have a common connection circuit and it can not be broken off.

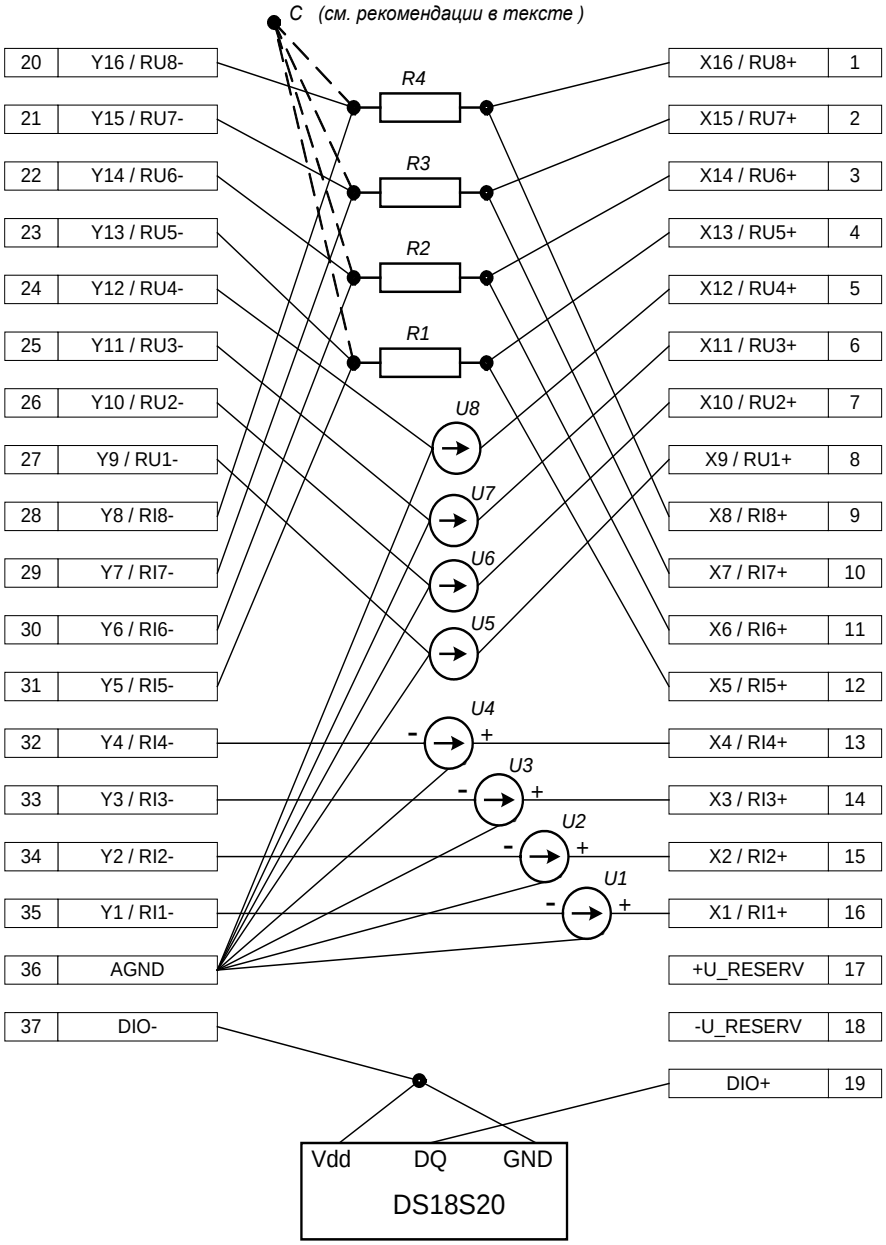


Fig.16-5. LTR114. An example of measuring circuits connection

For other cases, it is recommended to C (See recommendation in the text) connection diagram (there is no connection of resistors at the *C* point on fig.16-5) because this diagram ensures better symmetry of differential circuits and, therefore, better suppression of in-phase interfering signal and better signal/noise ratio in each measuring channel.

Let us consider in more detail connections for each type of signal source.

16.3.2 Connection options

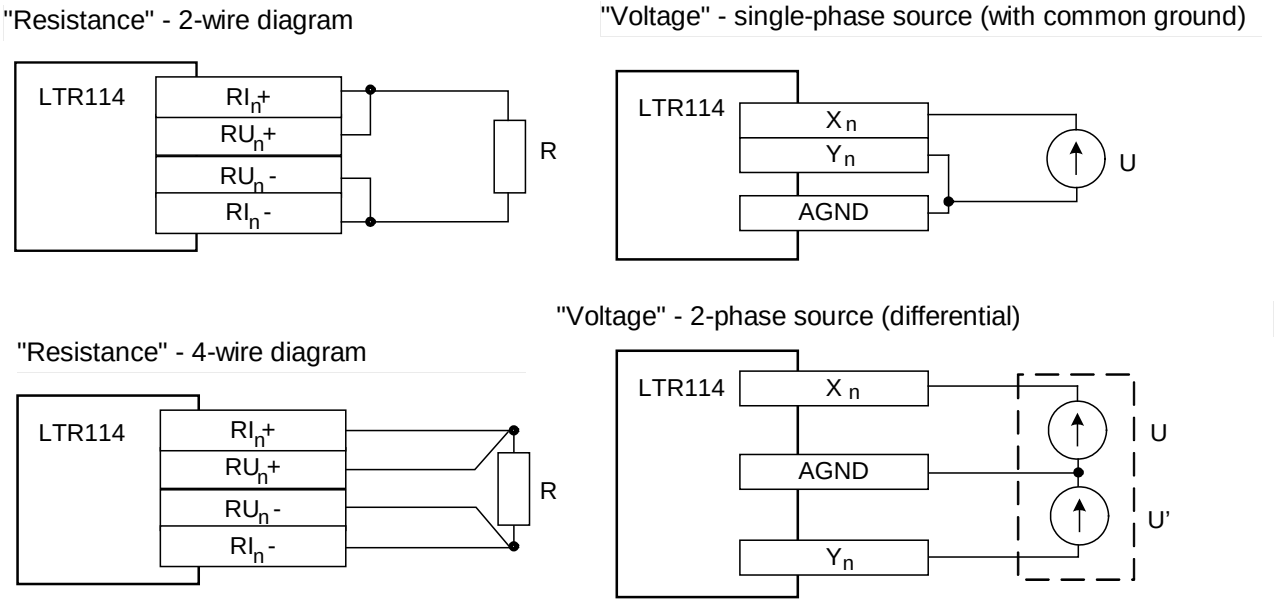


Fig.16-6. LTR114. Typical connection options

4 main options of signal source connection to the channel with number **n** are shown in fig.16-6. This options can be used in random combinations (up to 16 voltage sources and 8 sources of resistance), depending on application of circuits specified in table16-2.

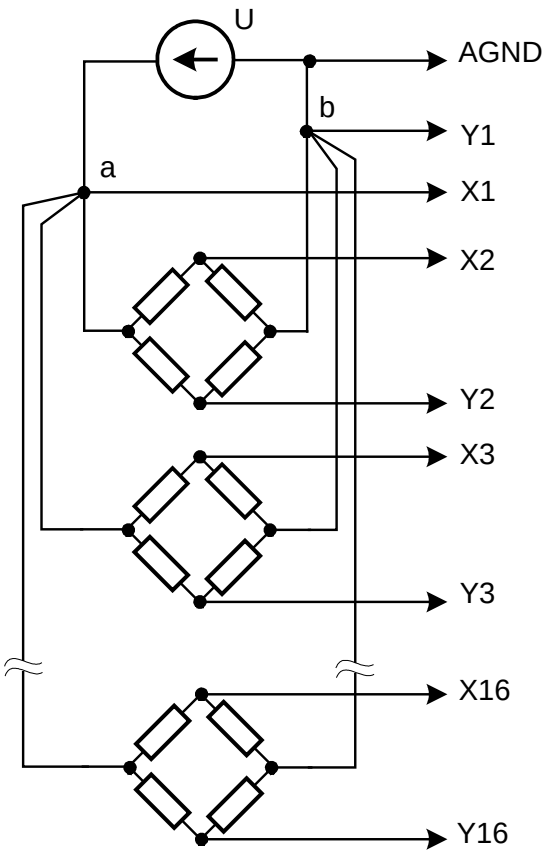
The difference between the 4-wire and 2-wire connection diagrams in case of *resistance measuring* is that there is no impact of internal resistance of wires on the measurement results. If internal resistance of wires can be neglected in your application and it is important to use as less wiring as possible, you can use the 2-wire diagram.

It is prohibited to connect inputs-outputs set for the resistance measuring mode to any external current and voltage sources except for special cases of duplicated connection of several LTR114 described below.

Any single-phase (with common ground) source must be connected to LTR114 with 2 wires but at *3 points* (!), as shown in fig.16-6.

In case of a screened cable, the screen shall be connected to the metal casing of the cable part of signal slot. Screen connection on the signal source side is not required.

Fully-reversed differential circuits are made with twisted-wire pairs (if applicable): RI-, RI+; RU-,RU+; X, Y from the same channel.



Connection of several bridge diagrams with external power supply is an interesting option. In this case, some of the channels can be used for voltage measurement at signal bridge diagonals and some for measurement of power supply voltage of each bridge.

fig.16-7 shows a model of connection of 15 bridges (channels 2-16) when channel 1 is used to measure power-supply voltage of the common supply circuit of the bridges. This option is cost-effective (cost calculated per measuring channel). The topology of bridges supply circuits shall be "radial" but not "serial traversal" in order to reduce their cross-interference: supply wires of all bridges shall converge at points **a** and **b**, and wires of channel for measurement of bridges (X1, Y1) supply voltage shall outgo from these points.

If it is impossible to apply the "radial" principle of bridges power wiring, more than one channel for bridges supply voltage measurement should be used.

This principle of bridges connection can be combined with other models of resistance and voltage measurement on other channels.

Fig.16-7. LTR114. An example of connection of 15-bridges with external power supply

While LTR212(M) module automatically considers bridge supply voltage in measured value of the bridge unbalance, in case of LTR114 the user must carry out such adjustment of measurement results himself at the upper software level.

16.3.3 Operating ranges of input signals.

Requirements set out below are essential for LTR114 correct operation. These requirements are necessary conditions for achieving the specified metrological characteristics of the device.

Requirement 1. If voltage is denoted by Ux and Uy relative to AGND on the corresponding poles X and Y of the differential input in the voltage measurement mode, the following voltage ratios should be maintained at Ux and Uy *inputs of the measured channel* in order to ensure the correct operation of LTR114:

$$\begin{cases} -5\hat{A} \le \dfrac{Ux+Uy}{2} \le +5\hat{A} \\ -10\hat{A} \le \mathrm{Ux} - \mathrm{Uy} \le +10\hat{A} \end{cases}$$

The specified ratios must be maintained for each differential input to which an external voltage source is connected. Here, the first inequation sets the limits of in-phase voltage at X and Y inputs relative to AGND for each measuring channel, and the second one sets the limits of counter-phase (informational) voltage. Both inequations shall be maintained simultaneously for each differential input set for voltage measurement.

Note: As compared to module LTR11, module LTR114 has more limited operating range of in-phase signal at X and Y inputs relative to AGND.

Requirement 2. When Ux and Uy voltages are present at X or Y input of the *channel which is not polled* (not included into the control table), these voltages shall fall within the following ranges (regardless of whether resistance or voltage is measured in adjacent channels and regardless of which measurement subranges are set) to ensure the correct operation of LTR114:

$$\begin{cases} -10\hat{A} \le Ux \le +10\hat{A} \\ -10\hat{A} \le \mathrm{Uy} \le +10\hat{A} \end{cases}$$

Requirement 3. External measured voltages and resistances must be within the specified measurement sub-range for the corresponding channel. Running-out of this sub-range (overflow) for any channel can increase the interchannel passage and other metrological characteristics in adjacent measuring channels.

Requirement 4. It is inappropriate to carry out the measurements if at least one of the measured channels is not connected or its connection is incomplete.

Note. As it is prohibited to connect inputs-outputs of LTR114 set for resistance measurement to any external sources of voltage or current, the voltage range of lines engaged in the resistance measurement does not depend on external factors.

16.3.4 Duplicated (redundant) connection

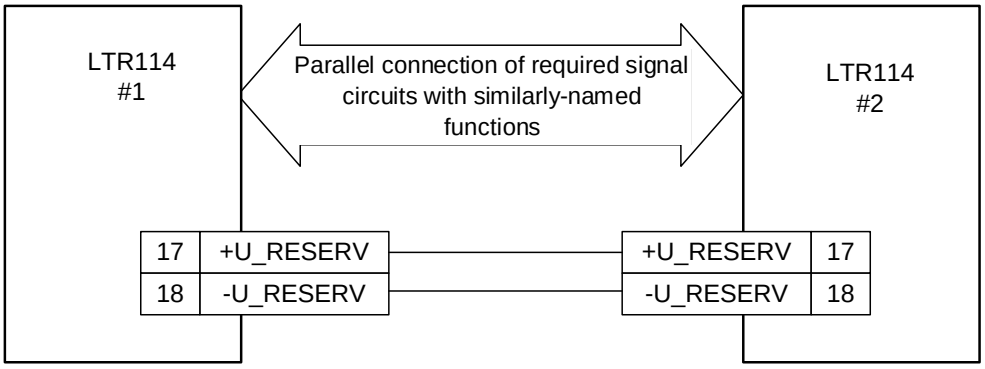


Fig.16-8. Duplicated connection of LTR114.

The purpose of the duplicated connection diagram is to ensure a high-resistance state of signal circuits even when one of LTR114 modules is de-energized. Usually the duplication is performed at the blocks level so it is assumed that LTR114 connected according to such diagram are located in different LTR crates. Duplication in LTR114 is implemented with some limitations. Let us consider them in more detail.

If the voltage measurement diagram is applied, metrological parameters deterioration is possible due to asynchronous switching processes in the input circuits if the duplicated connection diagram is used for simultaneous data acquisition in duplicated LTR114 modules. To avoid such deterioration, the data acquisition process must run in only one of the duplicated LTR114 modules.

If the resistance measurement diagram or a combined model (fig.16-5) is applied, one of the duplicated LTR114 modules must be unconditionally stopped (must be in the standby mode).

AGND circuits of the duplicated modules must be united if at least one LTR114 channel is used in the voltage measurement mode.

LTR114 does not support the duplication diagram involving synchronization of several LTR114 modules on a master-slave basis (fig.16-9) at least because the very "master-slave" principle is contradictory to the duplication idea. However, if any external synchronizing device performs the master function, a *special case* considered in paragraph 16.3.7 will occur.

Naturally, the concept of system duplication built on the basis of LTR114 shall specify that the duplication property is obtained only when LTR114 input switching circuits are operable. Moreover, the upper level software of the duplicated system should support automatic system restart if one of the system units fails.

16.3.5 Connection with synchronization: "master-slave"

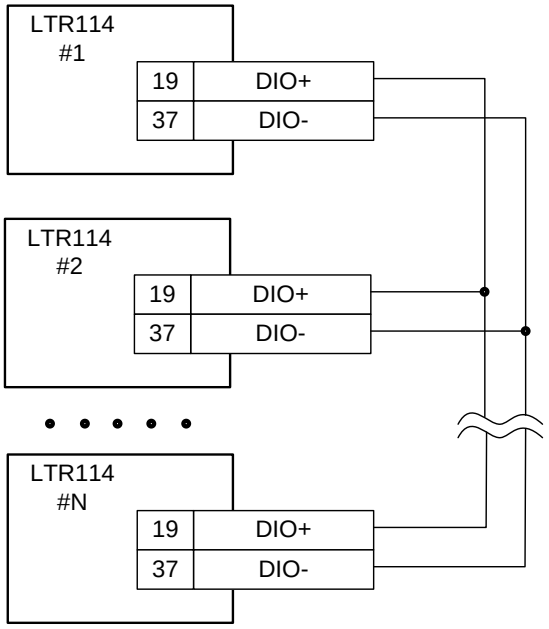


Fig.16-9. Synchronous connection of LTR114.

The synchronous diagram provides parallel data digitizing starting with the 1-st logical channel written in control tables of the modules and in accordance with the sequence of channels set in these tables.

Several LTR114 modules must be connected with a common synchronization line as shown in fig.16-9 to ensure their synchronous operation. In this diagram, one of the modules shall be configured for an "internal-master" synchronization mode and the others to an "external-slave" mode. When data acquisition is started on the slave modules they will not put out data unless ADC triggering pulses are received from the master module. An ADC triggering pulse is submitted for each data sample.

The correct sequence of actions during the start of the synchronous system comprised by several LTR114 modules is as follows:

- The synchronization line of slave LTR114 modules is configured for input ("slave")
- The synchronization line of master LTR114 module is set for output ("master")
- Data acquisition is started in LTR114 slave modules which will actually switch over to the mode of waiting for synchronization pulses from the master module.
- Data acquisition is started in LTR114 master module, and the slave modules will start to collect data synchronously with the master module.

It should be noted that the synchronization line DIO+, DIO- in each LTR114 is galvanically isolated from all other circuits. Thus, LTR114 connection according to the synchronous diagram does not break the galvanic isolation of each module circuits relative to the crate frame and its grounding circuit.

It is recommended to use a twisted-wire pair for the synchronization circuit and a screened pair of wires for better noise suppression. If the screen is used, it should be connected with the metal casing of the cable part of LTR114 connector.

The synchronous connection diagram eliminates the possibility of DS18S20 temperature detector connection to lines DIO+, DIO-.

The synchronous connection diagram (fig.16-9) can be applied together with the duplication diagram only in a special case considered in paragraph 16.3.7.

Synchronous operation is also possible when there is no master module LTR114 . The function of ADC triggering pulses initiator can be performed by an external source of TTL pulse signal with a period of min. 250 μs.

Operational characteristics of synchronization channels are given in Appendix A.14 on page 352.

16.3.6 External synchronization.

When ADC conversion frequency must be strictly set (up to 4 kHz) for your application, and the proposed frequency spectrum for internal synchronization does not satisfy the task requirements, external synchronization can be used in the form of a digital TTL-signal sent to line DIO+ relative to DIO-. DIO- line performs the function of a common wire. Presence of galvanic isolation at input DIO+, DIO- relative to the rest circuits makes the connection of external synchronization signal source isolated from the LTR114 measuring circuits, which is significant for a device of such accuracy class.

The required characteristics of synchronization signal in the "slave" mode are given in Appendix A.14 on page 352.

16.3.7 Special case of synchronous duplicated system

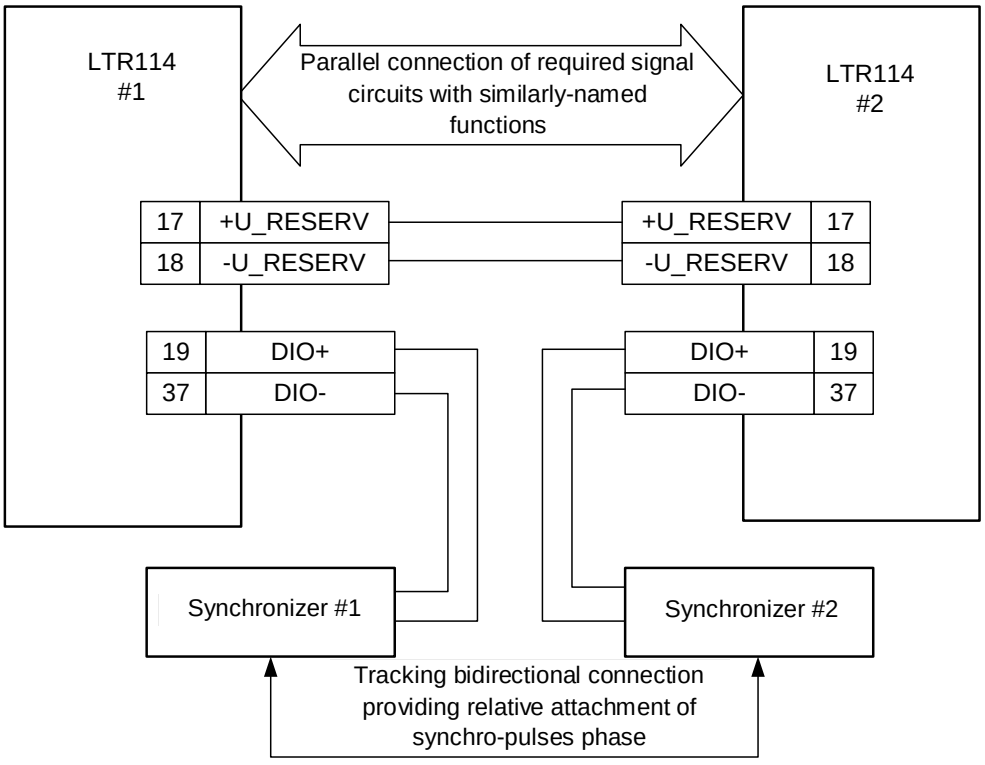
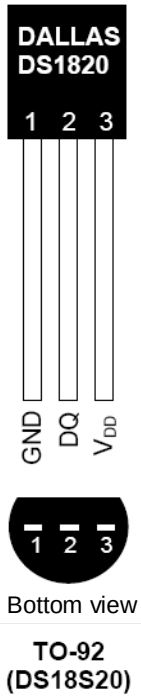


Fig.16-10. LTR114 synchronous duplicated system.

LTR114 does not support the duplication diagram involving synchronization of several LTR114 modules on a master-slave basis (fig.16-9) at least because the very "master-slave" principle is contradictory to the duplication idea. However, if any external synchronizing device performs the master function generating synchronization pulses of ADC triggering, and the lines sending synchronization pulses are duplicated (have separate sources of synchronization pulses synchronized with each other on the side of master device), the duplication feature can be obtained together with simultaneous synchronous operation of LTR114 (fig.16-10). In this case, the duplicated slave LTR114 modules operating in the *voltage measurement mode* can collect data simultaneously even at different channel polling sequences set in their control tables. However, *in the resistance measurement mode* (or in a combined mode) it should be ensured that the settings of their control tables and parameters of data acquisition frame do not allow for a situation of simultaneous measurement of resistance of the same external resistor by different LTR114 modules, otherwise the current will be supplied simultaneously from reference current sources of different LTR114 modules which will affect the normal operation (but will not cause a failure) of LTR114.

Operational characteristics of synchronization channels are given in Appendix A.14 on page 352.

16.3.8 Connection of DS18S20 temperature detector



If lines DIO+, DIO- of LTR114 are not supposed to be used for synchronous connection fig.16-9, fig.16-10, they can be used for connection of DS18S20 temperature detector as shown in fig.16-5. This detector can be used, in particular, for temperature measurement in areas of heterogeneous metal compounds to estimate the thermal electromotive force value.

Note: the function of measurement of LTR crate internal temperature is present in LTR-EU-8/16 crates.

Lines DIO+, DIO- in the mode of operation with a temperature detector fully implement the single-wire interface of DS18S20. Data acquisition from LTR114 temperature measurement channel will be performed against the background of the common process of data acquisition at intervals of approximately 1 sec.

Fig.16-11. Pin connection diagram of DS18S20.

16.3.9 Characteristics of signal line inputs and outputs

When connecting LTR114 module to your system, strictly observe the parameters specified in tables of this section.

! The manufacturer shall not be warranty liable for LTR114 failure caused by violation of maximum permissible operation conditions.

Note that impedance of input lines is greater in the *operating mode* than in the *switched-off* state of LTR114 module. For *further information on module switched-* off state see paragraph 4.8, page 93.

The characteristics of galvanic isolation in LTR are given in AppendixA.18, page362.

16.3.9.1 LTR114 operating mode

Module LTR114 installed in LTR crate has the following characteristics of input and output signal lines after LTR crate is powered on:

Table 16-3 Maximum permissible conditions, module LTR114 is switched-on.

Signal	**Type**	**Impedance**	**Maximum permissible conditions at input**
X1, X2,…,X16 Y1, Y2,…,Y16	Analog input	– Min. 100 Mohm for single-channel mode. – Variable resistive-capacitive for multi-channel mode	±20 V on inputs X <1...16>, Y <1...16> relative to AGND in the voltage measurement mode (see Notes 1, 2).
+U_RESERV	Input of reserved power supply to input circuits	—	-0.2.. +22 V relative to AGND circuit. **Short circuit is inadmissible on U_RESERV and AGND lines.**
-U_RESERV	Input of reserved power supply to input circuits	—	-22...+0.2 V relative to AGND circuit. **Short circuit is inadmissible on +U_RESERV and AGND lines.**
DIO+	Two-direction multi-purpose digital line	In the external synchronization mode: Over 50 kOhm when set for input. About 50 Ohm when set for output (see Note 3).	-0.3..+5.5 V relative to DIO- circuit. Maximum current ±20 mA. **Short circuit DIO+ to DIO- is admissible for maximum 5 sec.**

Notes:

1. It is prohibited to use external sources of current or voltage in the resistance measurement mode, and maximum permissible rates are not exceeded in resistance measurement circuit if an internal current source of LTR114 is used.

2. Numbers of channels having unconnected inputs should not be written to the control table. In other words, unconnected channels should not be polled. In case of breach of this condition, increase of noise and inter-channel transmission in the used channels is possible.

3. The state of input with pull-up resistor (1 kOhm) required for DS18S20 operation is used in the mode of external temperature sensor. Pull-up resistor is not used in the external synchronization mode.

16.3.9.2 Mode of power supply to input circuits from back-up LTR114 module

A switched-off LTR114 module with the input circuit energized from a back-up LTR114 module, see paragraph 16.3.4, has the following characteristics of input and output signal:

Table16-4 Maximum permissible conditions, LTR114 is switched-off and power is supplied via a redundancy circuit.

Signal	Type	Impedance	Maximum permissible conditions at input
X1, X2,…,X16 Y1, Y2,…,Y16	Analog input	Minimum 100 Mohm	±20 V at inputs X <1...16>, Y <1...16> relative to AGND circuit.
+U_RESERV	Input of reserved power supply to input circuits	—	-0.2..+22 V relative to AGND circuit
-U_RESERV	Input of reserved power supply to input circuits	—	-22...+0.2 V relative to AGND circuit
DIO+	Two-direction multi-purpose digital line	About 100 Ohm	-0.3..+5.5 V relative to DIO- circuit. Maximum current ±20 mA.

16.3.9.3 Module LTR114 is switched-off

Table 16-5 Maximum permissible conditions, module LTR114 is switched-off.

Signal	Type	Impedance	Maximum permissible conditions at input
X1, X2,…,X16 Y1, Y2,…,Y16	Analog input	About 5 MOhm	±20 V at inputs X <1...16>, Y <1...16> relative to AGND circuit
+U_RESERV	Input of reserved power supply to input circuits	—	-0.2..+22 V relative to AGND circuit
-U_RESERV	Input of reserved power supply to input circuits	—	-22...+0.2 V relative to AGND circuit
DIO+	Two-direction multi-purpose digital line	About 100 Ohm	-0.3..+5.5 V relative to DIO- circuit. Maximum current ±20 mA.

16.4 Special input lines testing mode

Checking input lines for breakage or short circuit of signal source is important for systems with a large number of channels. If your system does not provide for such option, the information given in this paragraph will not be useful for you.

This mode is treated as a *separate service task* which can be initiated before the main measurement session or after its completion. This means that LTR114 does not support simultaneous performance of this service task together with the main measuring task.

It should be noted at once that successful completion of testing of input lines from external signal sources (voltage and resistance) depends on the condition that the signal sources should not have a significant variable voltage component; otherwise, a non-deterministic variable will appear in the calculation procedure which will either complicate the testing task or make it unrealizable.

An internal test voltage source U_t and functionalities of internal LTR114 switch are used in the input lines testing mode. Equivalent diagrams of input circuits for two options connection of voltage and resistance circuits are shown in fig.16-12 and fig.16-13. Here, the *voltage signal source*is shown for the differential option where U_{SRC}^{X} and U_{SRC}^{Y} is EMF of the two phases of the voltage source relative to AGND common wire circuit[1], R_{SRC}^{X} and R_{SRC}^{Y} is internal (inherent) resistance of each phase of the signal source. It is obvious that for the case of single-phase (with common ground) source of signal you can take $U_{SRC}^{Y}=0$ and $R_{SRC}^{Y}=0$ for further calculations which are given below for this equivalent diagram. The circuits before the *resistance signal source* on fig.16-13 connected to LTR114 in a 4-wire diagram (fig.16-5) can be checked in the test mode pair-wise, separately for the circuit used for current supply and for the voltage drop measurement circuit (it does not matter in this equivalent diagram which of these pairs is for current and which one is for voltage measurement). The reference current source used for resistance measurement is switched-off in this mode.

In both cases (fig.16-12, fig.16-13), the same LTR114 internal diagram of input lines testing is used consisting of hardware key K1 actuating the line check test mode and keys K2, K3 setting the variations of the test mode. In this diagram, a test source of voltage U_t, resistors R1-R4 and transfer impedance R_{SW} of input channels of LTR114 electronic key are also engaged.

[1] this is the potential which can be measured on the voltage source at zero load current

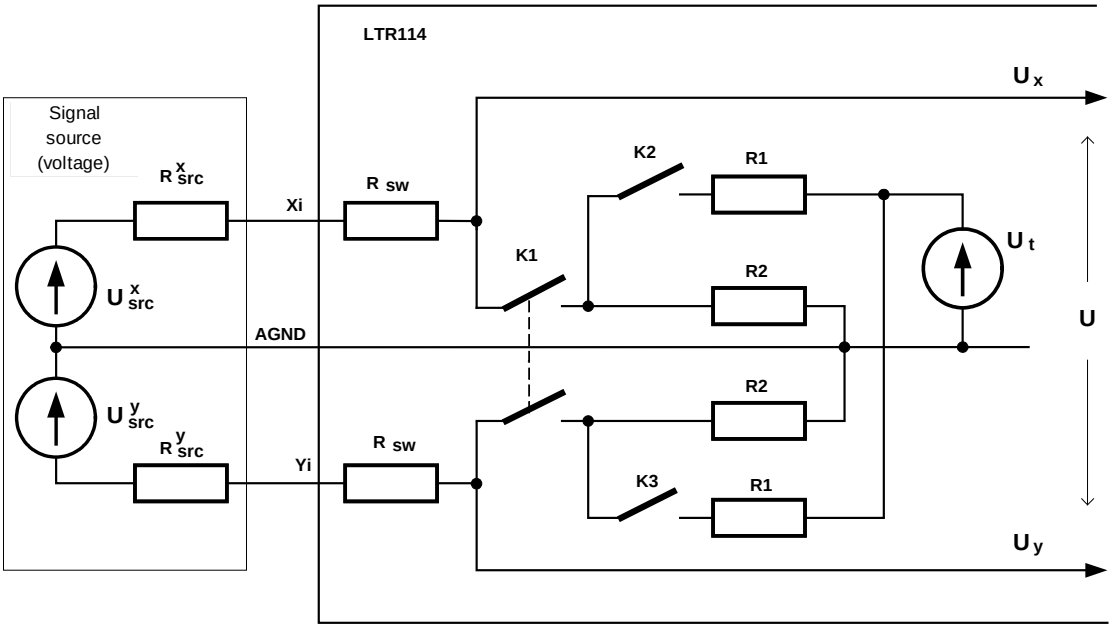


Fig.16-12. Input lines testing mode. Voltage signal source

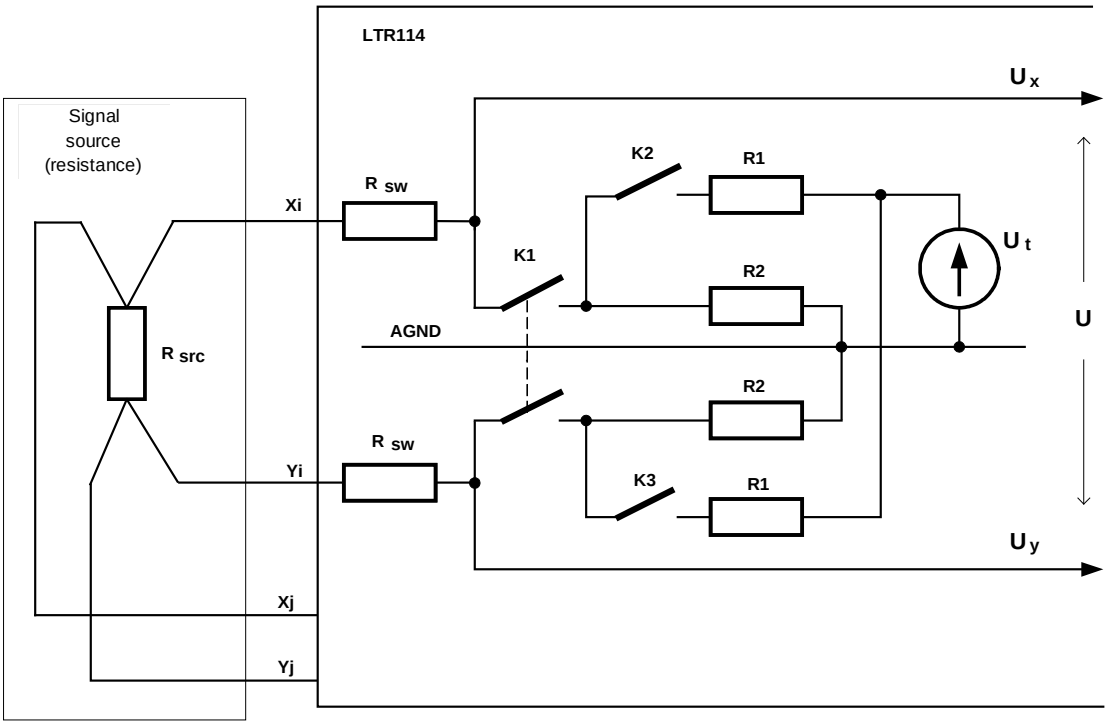


Fig.16-13. Input lines testing mode. Resistance signal source

-

Variations of input lines testing mode are listed in the table:

Test mode	K1	K2	K3
Off	Open	—	—
Pull-up X → "0", Y → "0"	Closed	Open	Open
Pull-up X → "+", Y → "0"	Closed	Closed	Open
Pull-up X → "0", Y → "+"	Closed	Open	Closed

-

Voltage U (fig.16-12, fig.16-13) measured by LTR114 is also engaged in the procedure for checking the input lines operability. Note that voltage U is applied to the internal point of LTR114.

Constant parameters of the equivalent diagram in question can be used for calculations and are presented in the table:

Parameter	Value
R_{SW}	120 Ohm
R1	20 kOhm
R2	100 kOhm
U_t	5.6 V

In the equivalent diagrams described above, only parameters which are external relative to LTR114 are unknown: resistance and EMF of the signal source. The rest of parameters of the circuits are known. The problem of identification of breakage and short circuit of signal source[1] becomes resolvable based on these initial data.

It should be noted that this principle of input lines control *explicitly does not support the identification of AGND circuit breakage* before the signal source in the voltage measurement mode. AGND circuit breakage will bring the device to conditions of uncertain (randomly changing under the influence of interferences) in-phase voltage at the differential input which can cause a distortion of measured signal and there is no possibility to elaborate a criterion for identification of a particular situation of AGND circuit breakage.

[1] General information on the "breakage" and "short circuit" criteria for undefined source of signal are not contained in this Manual but these criteria can be easily obtained for your specific case of signal source based on the provided data. To get an advice on this issue and other technical matters, send an email to support@lcard.ru .

Chapter 17. LTR210 ADC module

17.1 Intended purpose

LTR210 is intended for creation of multi-channel systems for recording of physical processes signals with a frequency of up to 5 MHz. LTR210 can be used for recording and measurement of transients against a set synchronization condition. LTR210 module has 2 channels of analog ADC input plus 1 multi-functional digital input/synchronization input-output. By installing up to 16 LTR210 modules into LTR crate, up to 32 analog channels for synchronous data acquisition with common synchronization can be obtained. A start-stop (oscillographic) mode with ADC conversion frequency of up to 10 MHz and a streaming mode of data acquisition with up to 500 thousands samples per second are supported.

17.2 General description of LTR210

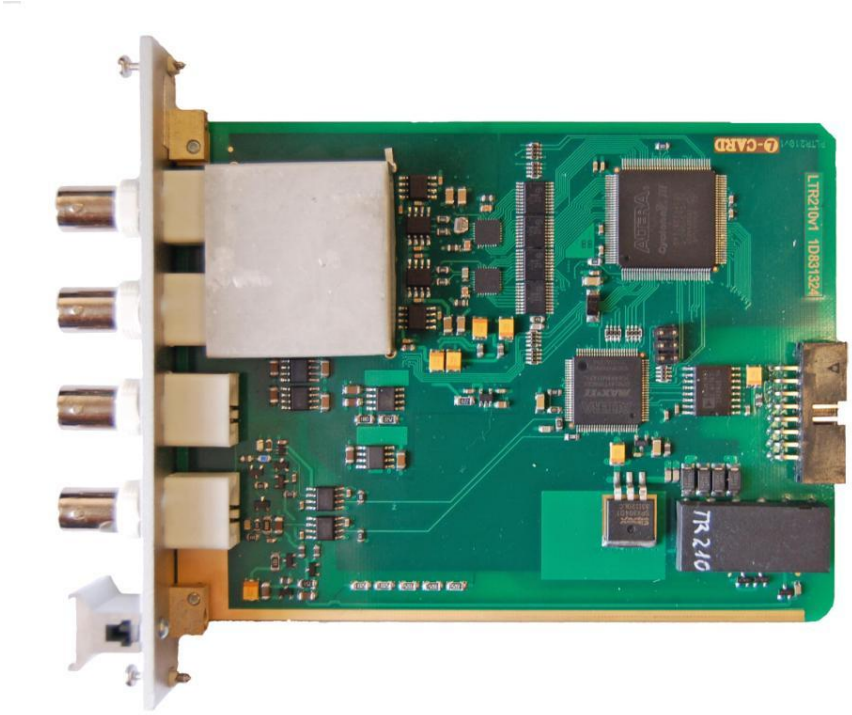


Fig.17-1. LTR210 view

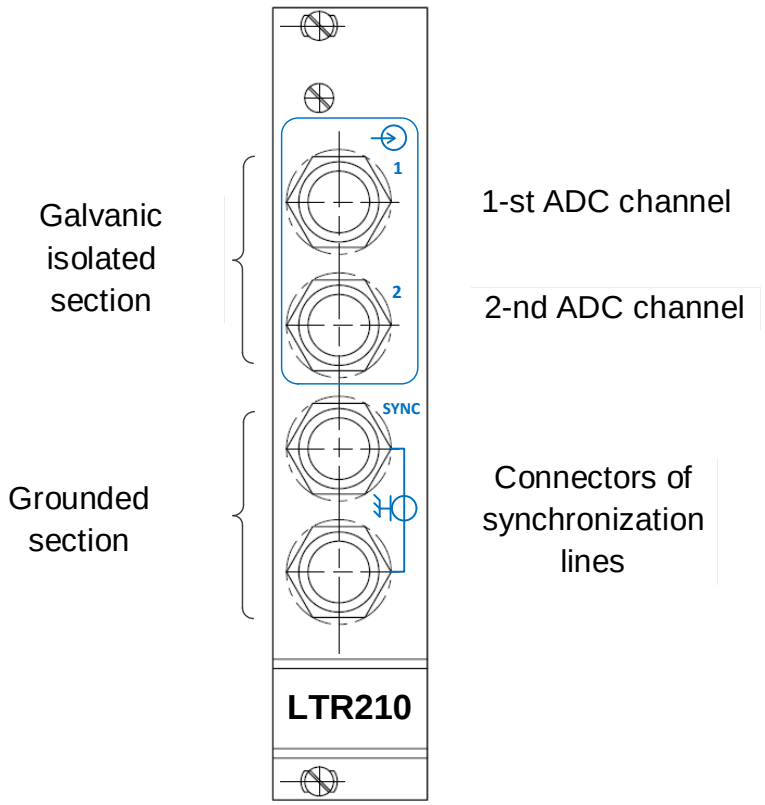


Fig.17-2. LTR210 panel

LTR210 panel (fig.17-2) has 4 BNC connectors (the upper pair are ADC inputs, the lower pair are multi-function digital input/synchronization input-output). Both connectors in the lower pair are connected in parallel inside LTR210. Therefore, different LTR210 can be connected consequently with wires into a common synchronization line.

LTR210 module is a 2-channel ADC designed for tasks of data acquisition with ADC conversion frequency of up to 10 MHz in the start-stop (oscillographic) mode. LTR210 has the following technical characteristics:

- LTR210 has two separate ADCs with bit depth of 14 bits and conversion frequency of up to 10 MHz.
- ADC frequency spectrum is defined by the ratio 10/n, where n=1,2,…,10. These frequencies are the result of division of LTR crate reference generator frequency (different LTR210 modules in the same LTR crate have coherent conversion frequencies). Both data acquisition channels can be configured for one conversion frequency
- Both ADC inputs have five independently programmable sub-ranges of input voltage: ”±10 V”, “±5 V”, “±2 V”, “±1 V”, ±0.5 V” and also programmable modes of "own zero" measurement and "closed input" mode (an AC mode with filtration of signal DC component). Presence of ±13.5 V DC component in ±0,5 V sub-range and ±4 V in ”±10 V” sub-range are operating conditions in the "AC" mode.
- Both ADC inputs have input resistance of 1 MOhm and 12 pF capacity, thus, the compatibility with a standard oscillographic probe is ensured.

- The upper passband frequency is 5 MHz, the lower passband frequency is 0 Hz (0.8 Hz in the "AC" mode)
- On LTR210 panel there are 4 BNC connectors (the upper pair are ADC inputs, and the lower pair is for connection of the synchronization line).
- There is a technical capability for connection of tens of LTR210 modules into a common synchronization line.

LTR210 supports the following configurations of multi-module synchronization:

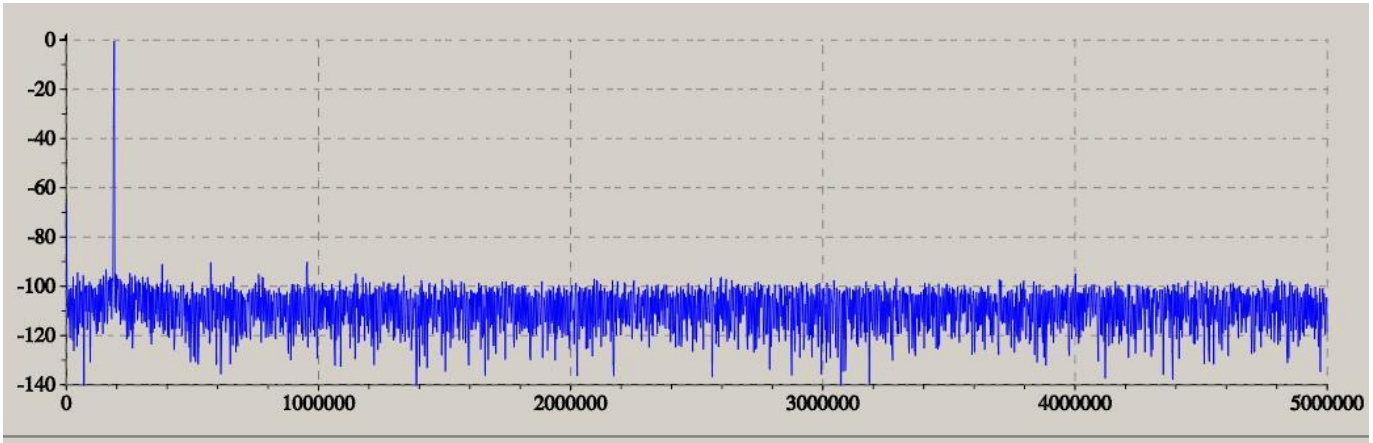
1. The pairs of BNC synchronization connectors of LTR210 adjacent modules can be connected sequentially into a 50 Ohm coaxial line with 50 Ohm terminal plugs. One of the LTR210 modules in this configuration (assigned as the master module) can be the source of recording synchronization pulse for the rest modules in the circuit. The synchronization event in the master module can be programmed as passing the set signal level in the selected channel.
2. An external synchronization signal with standard TTL voltage levels can be sent to the synchronization connector of LTR210 module.

- Module synchronization modes:
  1. On edge/on drop of analog signal at “IN1” or “IN2” inputs (upon the event of passing the set level within the specified sub-range of the corresponding input).
  2. On edge/on drop of digital signal at the synchronization input.
  3. Upon synchronization event occurred in another module assigned as the master in case that synchronization connectors of the modules are connected between themselves into a circuit.
  4. Upon asynchronous program event.
- ADC inputs are galvanically isolated from the ground and LTR crate frame, but the "common wire" circuits of both ADC channels inputs are not isolated from each other.
- LTR210 synchronization inputs are not isolated from the ground and LTR crate frame.
- Single-channel (on any of the channels) or bi-channel mode of recording are possible. In any case, one of the channels can be used for synchronization event generation.
- Module memory volume is 16 millions of ADC data samples (which corresponds to the recording time of 0.8 s at ADC conversion frequency of 10MHz in the bi-channel mode or 1.6 s in the single-channel mode).
- Multi-functional synchronization/digital input bit in the ADC data stream actually refers to the possibility to insert binary data from the selected source (independently for each ADC channel) in the ADC data stream without increase in the traffic: logic state of the SYNC line, result of level comparison in the selected ADC channel to the set *synchronization level*, pulse of asynchronous program or periodic synchronization. For example, in the bi-channel ADC data acquisition mode this makes possible to obtain the 3rd channel of digital input from the SYNC line and the 4th channel as the result of comparison of the selected ADC channel level to the synchronization threshold.
- The time delay caused by the signal propagation delay in inter-module synchronization circuit is max. ±T, where T is ADC conversion period.

17.3 LTR210 characteristics

The list of all LTR210 characteristics is given in Appendix A.15 on page 356. Important comments on some characteristics will be given here.

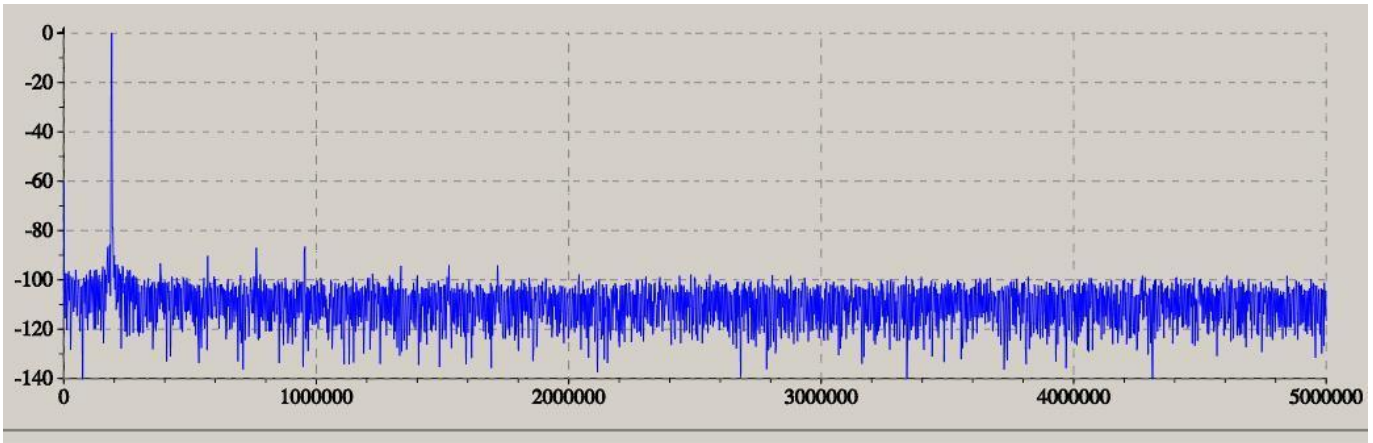
17.3.1 Spectral characteristics of LTR210.



channels

Channel	Color	Mean	RMS	Frequency	SNR	THD	SINAD	SFDR	ENOB
Channel 1		-0.000311	0.326528	191000	75.22	-81.35	74.28	88.93	12.05

Fig.17-3. Sinusoidal signal spectrum. Sub-range “±0.5 V”.



channels

Channel	Color	Mean	RMS	Frequency	SNR	THD	SINAD	SFDR	ENOB
Channel 1		-0.002390	1.382671	191000	75.84	-81.12	74.71	77.70	12.12

Fig.17-4. Sinusoidal signal spectrum. Sub-range “±2 V”.

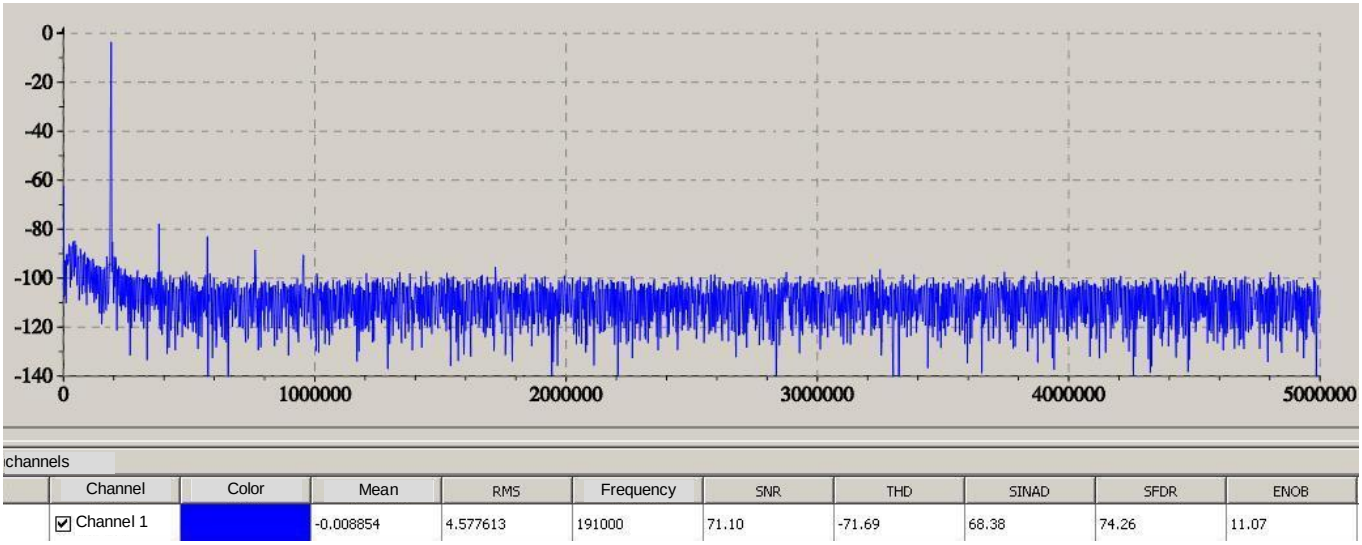


Fig.17-5. Sinusoidal signal spectrum. Sub-range "±10 V".

An important spectral characteristic of LTR210 is absence of visible determined leakages and interference in the spectrum. The above screen-shots of spectra are made at ADC conversion frequency of 10 MHz in the single-channel mode without data reduction. FFT dimension is 20,000 points. Blackman-Harris window. Sinusoidal signal frequency is 191 kHz. The rest calculated spectral characteristics for these conditions are shown on the screen-shots.

The increase of spectral noise density in the low frequency area in sub-ranges "±10 V" and "5 V" is explained by presence of thermal noise (Johnson's noise) generated by input high-resistance voltage divider, paragraph17.5.1, page 278. This objective physical effect deteriorates the signal/noise ratio at sub-ranges "±10 V" and "5 V" approximately by 3 dB as compared to sub-ranges "±2 V", "1 V" and "0.5 V".

Appearance of fold harmonics (at the level below -77 dB relative to the first harmonic with a frequency of 191 kHz) at the range "10 V) is explained by characteristics of GZ-118 generator applied when making these screen-shots.

The increase of spectral noise density in the frequency area when connecting to the input of a standard oscillograph probe 1:10 (in a multi-purpose oscillograph, as a rule, this effect is not observed due to its small dynamic range) is also associated with this physical effect. Thermal noise does not appear when working with probe in 1:1 mode at sub-ranges "±2 V", "1 V" and "0.5 V".

If in your mode of LTR210 application, low-frequency thermal noise appears and the useful part of the signal spectrum occupies more high-frequency spectrum part, it makes sense to apply additional program HFF to improve the signal/noise ratio.

17.3.2 LTR210: a multi-purpose oscillograph or a specialized data acquisition system?

LTR210 module is different from a multi-purpose oscillograph with the following set of properties which present the module as a specialized data acquisition system:

- 14-bit ADC and signal-noise ratio more than 74 dB.
- Main relative error of DC voltage measurement reduced to the measurement range ±0,2 %.
- Possibility to build a multi-module synchronous data acquisition system.
- Possibility of remote connection via Ethernet in the option with LTR-EU crate.

- Availability of an additional continuous data acquisition mode (up to 500 thousand samples per second) for checking measurement channels for serviceability prior to carrying out key measurements at high conversion frequencies.
- Availability of periodic acknowledgments of writing to buffer at long waiting for an external synchronization event of data reading (this is an important property when using LTR210 for conducting measurements in expensive physical experiments, for example, those related to destruction of structures).
- Digital input of synchronization signal is implemented in LTR210 as a separate input channel.
- Galvanic isolation of analog inputs of each module which is not lost when integrated to a multi-module synchronization system.
- Index data format containing module number, channel number, code of specified voltage sub-range, cycle counter of control over data continuity- all these possibilities of LTR data format increase the convenience and reliability of correct data interpretation at the upper program level when developing software for multi-channel systems.
- Possibility of hardware and software integration with other data collection modules within LTR system. Possibilities of system development in different LTR crates design options as well as in future LTR crate models which are planned to be released.
- Possibility of implementation to LTR210 of an additional logic functionality by means of updating FPGA firmware and software with account for customers' demands (for firmware, see paragraph 17.5.3, page 284).

17.3.3 LTR210 module configuration

The basic configuration of LTR210 module does not include accessories supplied in the package. The module can be supplied with the following components upon additional order:

Component	Note
50 Ohm plug (terminator), type BNC-7017.	Plug for LTR210 synchronization line. In most cases, 2 pieces per synchronization line are required, see paragraph 17.6.2, page 287
BNC-BNC-0.15 cable, 0.15 m length.	Cable configuration: BNC-7006 connectors on both ends of RG-174/U 50 Ohm cable. Total cable length (with connectors shells) is 15 cm. The cable is used for connection of the synchronization line of LTR210 modules located in adjacent slots of LTR crate, see paragraph 17.6.2, page 287.
BNC-BNC-1.0 cable, 1.0 m length.	Cable configuration: BNC-7006 connectors on both ends of RG-174/U 50 Ohm cable. Total cable length (with connectors shells) is 1 m. The cable is used for connection of the synchronization line of LTR210 modules located in different LTR crates and for sending signals to ADC inputs from signals sources with block BNC-connectors.

17.4 Installation and set-up

During LTR210 installation in crate, observe the module installation rules common for LTR system, see paragraph3.6.2.2, page 52.

Mounting screws on the module panel must be tightened.

The module does not require any settings before installation to LTR crate.

17.5 Overview of LTR210 hardware components and operation principles

17.5.1 Block diagram

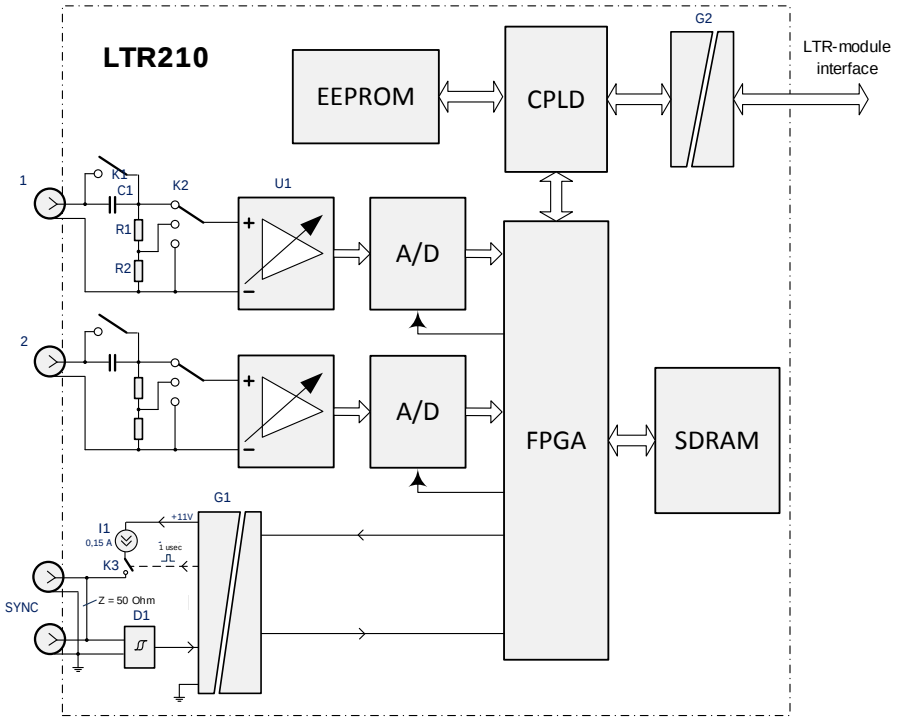


Fig.17-6. LTR210 block diagram

The block diagram of LTR210 (fig.17-6) is based on two identical ADC channels with corresponding coaxial inputs 1 and 2. The input circuit of each channel includes a capacitor (C1) with a capacity of 660 nanofarad, a resistance divider (R1, R2) with input resistance of 1 MOhm, and hardware keys K1, K2. Capacitor C1 at opened key K1 performs the function of *closed input* ("AC" mode when the constant component of the input signal is cut off). When key K1 is closed, the *open input* is implemented (“DC+AC” mode when the constant and the variable components of signal are passed). Electronic key K2 in its upper (as per diagram) position passes input signal 1:1 (used during setting LTR210 for sub-ranges “±2 V”, “±1 V”, ±0.5 V”), in the middle position the key passes signal at the ratio of 1:5 (used during setting LTR210 for sub-ranges “±10 V”, “±5 V”), in the lower position the key enables the *mode of own zero measurement.*

It is significant that 1 MOhm input resistance is ensured in the range of peak values ±14 V of input signal (when the power supply of LTR210 module is on). Beyond the limits of ±15 V range, input resistance falls down up to 750 Ohm due to the presence of a diode protective loop in the input circuit. Maximum permissible long-term input voltage is ±20 V.

The signal is coming from key K2 output to the capacitor input with controlled amplification factor U1 implementing (together with dividers R1-R2) the full line of sub-ranges of LTR210 input voltage measurement: ”±10 V”, “±5 V”, “±2 V”, “±1 V”, ±0.5 V”.

The signal is coming from amplifier U1 output to ADC (A/D) of LTC2245 type with internal pipelined architecture. ADC conversion frequency from 1 to 10 MHz is set from FPGA. It is

significant that LTR210 ADC conversion frequency is the result of division of frequency of the single reference generator of LTR crate (Appendix A.16, page 359). Lower conversion frequencies are obtained in FPGA by means of data reduction (decimation). It is technically possible to implement a filtration mechanism (LFF) in future FPGA firmware to improve the signal/noise ratio at low frequencies of data acquisition.

All intellectual logic of LTR210 is located in FPGA with updated software-loaded firmware. FPGA controls hardware keys and amplifiers independently for each channel depending on the selected program mode, performs ADC synchronization, receives and processes data from both ADCs, performs data buffering in SDRAM (32 MB), implements data synchronization functions via SYNC synchronization channel, sends processed data to CPLD for further output to LTR-module interface, and implements the interface of LTR210 modes control.

CPLD has a minimal sufficient non-volatile logic for processing low-level commands RESET, STOP and ROM_IO (for access to EEPROM) and logic of firmware loading to FPGA from the upper program level.

EEPROM keeps serial number of LTR210 module and its calibration factors.

External LTR210 synchronization channel has two SYNC connectors on the module panel which are connected in parallel. These connectors are connected inside LTR210 by the line with wave-making resistance of 50 Ohm in order to have a possibility to connect several LTR210 modules into the same coherent line. LTR210 module synchronization channel is capable to operate to input (slave mode) as well as to output (master mode).

In the slave mode, synchronization signal is received by Schmitt trigger (to improve the noise resistance) and is further sent to FPGA via a galvanic isolation element G1.

In the master mode, synchronization signal from FPGA, having passed through the galvanic isolation element G1, triggers a current pulse of about 150 mA with duration of 1 μs in current source circuit I1 and electronic key K3. *The synchronization event corresponds to increasing voltage edge and current in the SYNC line.* When SYNC connectors of one or several LTR210 modules connected into a 50 Ohm coaxial line with 50 Ohm plugs (at both ends of the line), voltage at the pulse moment will be 3.0-4.5V and in when there is no pulse it will be less than 0.1 V. **It should be considered** that if there are no 50 Ohm plugs in the synchronization line, the synchronization signal voltage pulse can reach the peak voltage value of up to 11 V! This happens because the source of impulse current power is supplied from an internal voltage source of 11 V and in case of no load the mode is close to "no-load run" mode of this voltage source. This excess voltage can not bring out of operation own SYNC input or connected SYNC input of other LTR210 module due to presence of corresponding protection of SYNC input in LTR210, but when connecting a standard TTL-input of an external device to this line necessary measures must be taken to protect this TTL-input.

Quite powerful synchronization signal from master LTR210 implemented in LTR210 spreading through well-coordinated electrical environment with wave-making resistance of 50 Ohm allows for connecting tens of LTR210 modules into a common synchronization circuit!

It is important that synchronization connectors SYNC of LTR210 are grounded to LTR crate frame and ADC inputs 1 and 2 are isolated from the frame and ground circuit of LTR crate. Particularly, in case of uniting several LTR210 modules in the synchronization line SYNC, galvanic isolation of inputs of each LTR210 is saved. Inputs 1 and 2 of the same LTR210 module are not galvanically isolated from each other.

17.5.2 Operation principles

- The entire digital part of LTR210 can be logically divided into two parts:

1) Non-loaded non-volatile logic (stored in CPLD and EEPROM).
2) Loaded non-volatile logic (in FPGA Cyclone III).

Program FPGA loading from the upper program level is performed by means of CPLD. CPLD stores the controlling logic of reset, module stop, access to EEPROM and FPGA loading. In FPGA, all the rest LTR210 logic is stored depending on the functional application of this module.

- LTR210 operation logic is based on a 32 MB circular buffer in SDRAM, and all possible data buffering capabilities correspond to the capabilities of this circular buffer.
- The maximum rate of writing to the circular buffer is 40 MB/s (the maximum traffic from 2 ADCs operating at a conversion frequency of 10 MHz).
- The maximum rate of reading from the circular buffer is determined by the possibilities of LTR-module interface: for LTR-U-1-4 crate, this rate is 200 kS/s, for other crates it is 500 kS/s; and since in LTR 4 bytes correspond to one sample, this will result in 800 and 2000 kB/s traffic, accordingly. When several LTR210 modules are used in LTR crates, the limitation of traffic capacity of this crate interface should be considered.
- Based on the above stated buffer capabilities, LTR210 can operate in the following modes:
  - A continuous data acquisition mode with the total frequency of data collection of 200 or 500 kS/s (depending on the crate configuration) in the single-channel mode or 100 or 250 kS/s in the bi-channel mode, provided that the rate is calculated for each channel.
  - A frame-by-frame mode of data acquisition according to synchronization conditions with data accumulation within the limits of the circular buffer of up to 16 million samples.
- In the frame-by-frame mode of data acquisition, when a *synchronization event* occurs, LTR210 module sends the accumulated data (with the total size of **SIZE** samples) to the interface starting with the sample written to the buffer **SIZE_HIST** samples prior to the synchronization event occurrence. Thus, with **SIZE_HIST** set by software (within the buffer size limits), *pre-history data* (prior to the synchronization event) will be sent to the interface with the size of **SIZE_HIST** and subsequent data (after the synchronization event) with the size of **SIZE – SIZE_HIST**.
- Since in the frame-by-frame mode of data acquisition *with continuous writing to the circular buffer* the speed of writing to the buffer can exceed the speed of reading, in this mode the maximum size of continuous data frame received from LTR210 depends on the reading to writing rate ratio and **SIZE_HIST** value.

Examples of correlation between these parameters are presented in the table below:

Table17-1. LTR210. Examples of maximum frame size for set ADC sampling frequency and set portion of pre-history in the frame-by-frame mode of data acquisition with continuous writing.

Rate of transmission to the interface (Kwords/s)	500	500	500	500	200	200	200	200
Number of channels	2	1	2	1	2	1	2	1
Pre-history (% of the frame size)	0	0	50	50	0	0	50	50
ADC conversion frequency (MHz)	10	10	10	10	10	10	10	10
Maximum frame size (per channel)	215086	882984	212363	860344	84731	342382	84305	338923

For the common case, see the evaluation formula connecting the implemented ratios of LTR210 data acquisition parameters in the Programmer's Manual.

- LTR210 also supports the frame-by-frame mode of data acquisition *with automatic suspending of writing to the circular buffer*. In this mode, even if the set speed of writing to the buffer exceeds the reading rate, you can receive a frame with the size of 16 million of continuous data samples (up to the maximum amount of data in the circular buffer) from LTR210. In this mode, writing to the circular buffer is automatically paused until LTR210 sends the full size **SIZE** of requested data to LTR interface.
- The mode of *continuous acquisition-output without data loss* up to 50 kHz is implemented in LTR210. The mode is limited in speed by ratio Fs*N ≤ 50000 Hz, where Fs is specified frequency of recording (writing) of ADC channel (with account for reduction factor), N is number of ADC channels engaged in writing (1 or 2).
- LTR210 supports response to the following synchronization events:
  - Program asynchronous synchronization with output of a data frame of the set size on the asynchronous program command.
  - Analog synchronization with output of a data frame of the set size upon the signal passing of the *set synchronization levels* (paragraph 17.5.2.2) in the set ADC channel; the direction of signal transition is programmed. Despite that data of one ADC channel can be not written in the buffer (if the single-channel mode is used), *analog synchronization will nevertheless operate, particularly, for the channel from which data are not coming*.
  - digital synchronization with output of a data frame of the set size upon the signal transition from one logic state to another in the external synchronization line SYNC; the direction of signal transition is programmed;
  - periodic synchronization with periodic start of output of data frames of the set size and interval (up to 1 hour with the period setting unit of 1 μs, the mode is equal to periodic oscillograph scanning).
- LTR210 can send to line SYNC the a response (in the form of a pulse 0->1->0 with duration of 1 μs) to an internal synchronization event (in the modes of program asynchronous, analog or periodic synchronization).
- LTR210 supports the following modes of grouping with adjacent LTR210 modules:
  - **INDIVIDUAL** mode when different LTR210 modules do not send a synchronization event to each other via the external SYNC line. Nevertheless, data reading from several LTR210 can be synchronized relative to an external synchronization source connected to the SYNC line.

- **MASTER or SLAVE** modes when MASTER -LTR210 serves as a source of synchronization event for itself and other SLAVE LTR210 modules. Synchronization event is transmitted by edge of pulse to SYNC line.

- Insertion of special logic signal to ADC data stream is implemented in LTR210 (for both ADC channels logic signals are different and independent). This logic signal can have following functions assigned by software:
  - Value of the SYNC line (i.e. a digital input of SYNC signal is actually implemented).
  - Dedicated data synchronization signal of ADC1 channel according to the specified thresholds (paragraph17.5.2.2, i.e. a digital input from the comparator on a signal from 1st ADC channel is actually implemented).
  - Dedicated data synchronization signal of ADC2 channel according to the specified thresholds (paragraph 17.5.2.2, i.e. a digital input from the comparator on a signal from 2nd channel of ADC is actually implemented).
  - Value is "1" at the moment of triggering of one-time program or periodic synchronization (if such modes have been installed), for other cases, the value is "0".

The logic signal mode is set independently of whether this logic signal is used for ADC synchronization or not used.

- When data frame transfer is finished LTR210 sends a status word containing the following:
  - an attribute of history data invalidity (appears when SIZE_HYST≠0 and reading synchronization is occurred with a too short delay relative to the record (writing) enable).
  - an attribute of missing repeated synchroevent (appears if during the transfer of data related to the current synchronization event the next synchronization event occurrs which can not be processed).
  - an OVERLAP attribute indicating that the transfered data frame can have incorrect values of samples because the process of writing into the circular buffer was in advance of the reading process (the attribute is relevant only for the frame-by-frame data acquisition mode *with continuous writing to the circular buffer*).
- For experimental user tasks related to long waiting for a synchronization event, a mode of periodic confirmation of writing to the circular buffer can be enabled: when a synchronization event has not occurred, a status word with an attribute of writing process running is sent at intervalы of 0.5 s.
- Index part of the data word sent from LTR210 contains ADC data field, ADC channel number, code of the set voltage range, cycle counter of control over ADC data continuity and multifunctional bit of synchronization/digital input (table17-5, page 291).
- Multifunctional synchronization/digital input bit in the ADC data stream actually means a possibility to insert binary data from the selected source (independently for each ADC channel) to ADC data stream:
  - Logic status of SYNC line
  - The result of comparison of level for the selected ADC channel with *the set synchronization level* (for example, in the single-channel data collection mode from the 1st ADC channel, the results of data comparison from the 2nd ADC channel can be inserted to this stream).

- Pulse of asynchronous program or periodic synchronization if such synchronization has been used (this possibility allows for seeing the synchronization pulse in the data stream regardless of whether this synchronization condition has been used as a condition for data acquisition).

- LTR210 performs data correction in accordance with calibration factors "on-the-fly" prior to writing them to buffer. Operations of data comparison to the set thresholds is executed in respect of calibrated ADC data.
- The main logic of LTR210 operation is implemented in FPGA Cyclone III. FPGA firmware is updatable and loaded before the start of the operation (not kept inside LTR210).

17.5.2.1 Rate of data transmission to LTR210 interface.

Rate of data output of LTR210 is set by software from the following possible values: **500**, **200**, **100**, **50**, **25**, **10** kS/s. We remind that a sample in LTR is equal to 4 bytes, see paragraph 4.6, page 15. Correspondingly, the data transmission traffic will be equal to **2,000**, **800**, **400**, **200**, **100**, **40** KB/s.

Technically possible traffic from LTR210 is determined by the maximum speed of interface of this LTR crate and the number of installed LTR210 (or other modules).

For reference:

- In LTR-U-8/16 crates, the maximum possible total traffic from LTR-modules is 20 MB/s.
- In LTR-EU crates, the maximum possible total traffic from LTR-modules via USB 2.0 interface is 16 MB/s.
- In LTR-EU crates, the maximum possible total traffic from LTR-modules via Ethernet interface is 10 MB/s.
- In LTR-U-1-4 crates, the maximum possible traffic from the LTR-module is 400 KB/s.

! Based on the above mentioned data, it is strongly not recommended to exceed even for a short period the maximum permissible total traffic from LTR-modules in any LTR module configuration of the crate. In particular, in case of multi-module LTR210 configuration during synchronous data acquisition from several LTR210 modules it is required to set the data transmission rate for each LTR210 so as to avoid exceeding the maximum possible total traffic for this LTR-crate.

17.5.2.2 Levels of analog synchronization (detailed).

The known hysteresis principle shown in fig.17-7 is used in LTR210 to avoid "bounce" during separation of logic synchronization signal from the analog one.

The upper and the lower synchronization thresholds are set for both ADC channels independently.

It is important to note that the mechanism of analog synchronization operates with calibrated data and calibrated synchronization thresholds, which ensures precision setting of synchronization thresholds.

Extracted logic synchronization signal for the set ADC channel can be inserted into the data stream from LTR210. Thus, a separate **channel of data acquisition from the bi-threshold comparator via the set ADC** channel is actually implemented (irrespectively of whether this signal is used for ADC synchronization or not used.).

It is significant that the separation of synchronization signal is performed in the digital stream of samples from ADC collected with the set interval of data acquisition for ADC channel (considering the specified ADC convertion frequency and data reduction factor). Thus, the duration of pulse of this synchronization signal shall not be less than the period of data acquisition to ensure reliable synchronization triggering.

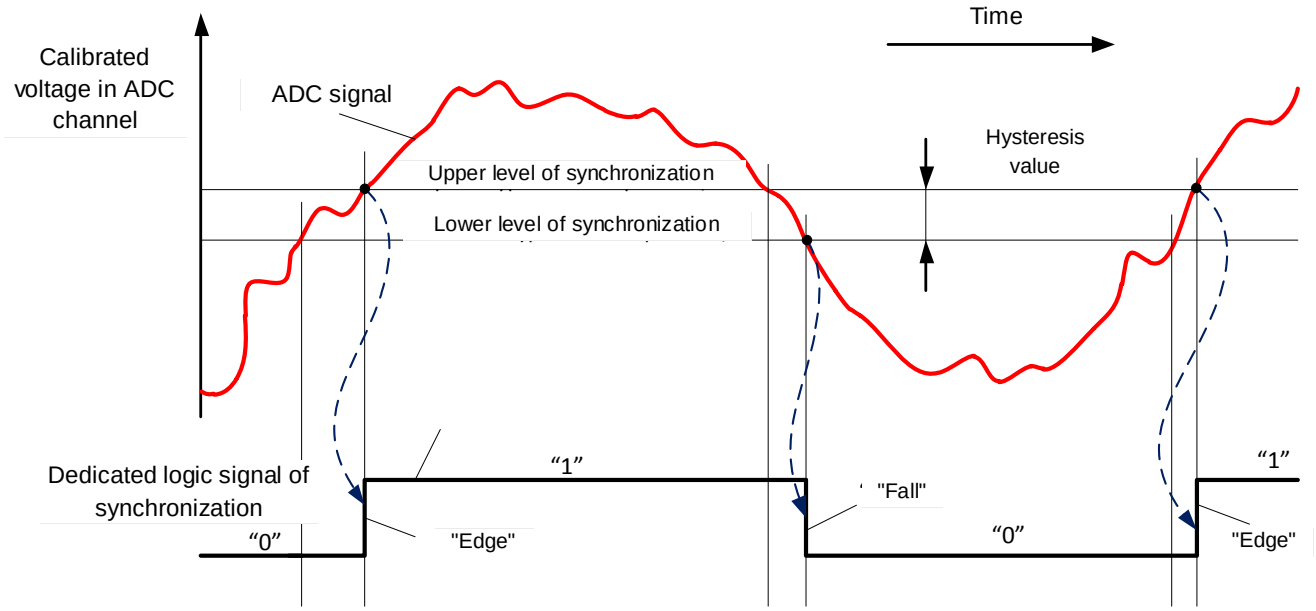


Fig.17-7. Hysteresis principle at separation of logic signal during analog synchronization

17.5.2.3 External synchronization via SYNC line.

In version 1 FPGA firmware (paragraph17.5.3, page 284), the synchronization signal from SYNC line is sampled with a period of data acquisition in ADC channel (considering the set ADC conversion frequency and data reduction factor). Thus, the duration of pulse of this synchronization signal shall not be less than period of data acquisition to ensure reliable external synchronization triggering on edge or on drop of digital synchronization signal. Generally, this limitation is overcomable and can be eliminated during the development of the next firmware version.

17.5.3 Versions of LTR210 firware.

In the table below, the hystory of FPGA LTR210 firmware versions is presented. This information will be updated in this Manual as new firmware versions are released. *The current FPGA firmware version is software-accessible.*

Information on engaged FPGA capacity is provided in the table for reference only. Quite a low percentage of engaged FPGA capacity is indicative of potentially great logic possibilities of

LTR210 which can be added in the next firmware versions to increase LTR210 capabilities. Let us remin that loaded FPGA firmware can be updated remotely.

Table17-2. LTR210. FPGA firmware versions

Firmware version FPGA	Date	FPGA engaged capacity Cyclone III	Note on implementation
1	May 2013	31 % logic elements 11 % memory volume	First official firmware.
2	August 2013	32 % logic elements 11 % memory volume	1. An error in module synchronization mechanism in the SLAVE mode is corrected 2. Digital delays in synchronization between the MASTER and SLAVE modules as well as between the ADC input and synchronization input are adjusted.
3	January 2014	32 % logic elements 11 % memory volume	An error related to ADC channels confusing in the DC component cut-off mode is corrected.
4	March 2014	32 % logic elements 11 % memory volume	A rarely occurring error of no LTR210 response to the program triggering of data acquisition is corrected.

17.5.4 Future development of logic capabilities of LTR210.

As the feedback from users is received and generalized, LTR210 FPGA firmware (paragraph 17.5.3) can be modified by L-Card. Quite a big amount of free logic resources in FPGA provides an opportunity to implement new services, synchronization modes and data processing methods inside FPGA LTR210.

You can send your feedback to e-mail address en@lcard.ru or write directly to the conference http://en.lcard.ru/forums/1?forum=1.

17.6 Connection of signals

The four connectors on LTR210 module panel *are* of BNC plug in socket type with corresponding cable connector of BNC cable plug type.

Actually, in case of accurate handling of LTR210 it is not prohibited (*but not recommended*!) to use domestic connector CP-50 instead of foreign-made BNC as a cable connector, but in this case *possible difficulties*[1] can arise when connecting or disconnecting this connector with the plug in connector BNC on LTR210 module.

[1] Historical roots of this problem belong to the non-conformity of "meter" standards of the former USSR to the western "inch" standards.

Attention! Due to the non-conformity of domestic (made in Russia) connectors to the BNC standard, use of CP-50 connectors (cable parts or adapters) in some cases can cause a damage of plug in connectors BNC in LTR210.

In case that LTR crate is supplied with several LTR210 modules more than two BNC connectors are implemented in LTR210 modules installed in adjacent slots of the crate, **it should be considered** that access to some BNC connectors will be difficult due to their tight integration. This fact restricts the possible sequence of assembly-disassembly of such field of plug connection. In all fairness it has to be added that the engaging force of the "original" BNC cable is much lower as compared to the "not original" CP-50 and in case of tight integration this fact will be of a high importance.

LTR210 board has one process 6-pin connector. **It is prohibited to put jumpers on process connectors of LTR modules and make any external connections!**

Table17-3. Description of LTR210 user connectors signals

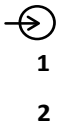
Signal name	Common point	Direc-tion	Description
	AGND	Input	Inputs of ADC channels 1 and 2 galvanically isolated from (grounding circuit) the LTR crate frame. AGND circuit (isolated BNC frame) is a common circuit for both inputs "with common ground". Input resistance is 1 MOhm. Inputs are compatibile with a standard oscillographic probe. Maximum permissible voltage values at the input: ±20 V.
	LTR crate frame and groundi ng circuit.	Input-output	A pair of BNC connectors (with common designation SYNC) cases of which are connected to LTR crate frame (and its grounding circuit). Both connectors inside LTR210 are connected in parallel (included in one LTR210 synchronization line with wave-making resistance of 50 Ohm). LTR210 module can serve both as a receiver and transmitter of synchronization signal from this line. Input characteristics: • Switching threshold +1.5…+2.4 V • Hysteresis voltage value 0.4…1.3 V • Input resistance 50 kOhm (within voltage range from 0 to 4.3 V) • Maximum permissible input voltage: ■ Long-term: -6.0 …+11 V ■ Short-term for 1 ms: -12 V …+15 V. Output characteristics: • Rated load resistance 25 Ohm (50 Ohm loads at both line ends). • Active pulse output current 150 mA (pulse duration is 1 μs). • Passive output current less than 2 μA • Output voltage of "no-load run" (up to 11 V peak voltage of 1 μs pulse). • Output peak voltage at the rated load +3.0…+4.5 V. For specific issues of connection, refer to paragraph 17.6.2

17.6.1 Behavior of LTR210 inputs in the switched-off state of the module.

In case that a multi-module system is created on the basis of more than one LTR crate, the behavior of circuits at the module connector in the switched-off state should be considered.

LTR Crate System

Table17-4. Circuits of user LTR210 connectors – switched-off state

Signal name	Common point	Description
	AGND	Maximum permissible voltage values at the input: ±20 V. "High level of resistance" of circuits inputs is not maintained. Impedance has a complex non-linear nature.
	LTR crate frame and grounding circuit.	Maximum permissible input voltage: ■ Long-term: -6.0 …+11 V ■ Short-term for 1 ms: -12 V …+15 V. *SYNC circuit resistance at a voltage from 0 to 4.3 V is maintained on the level of 15 kOhm when LTR210 is switched off.*

17.6.2 Specific issues of SYNC line connection

In the figures below, generalized connection diagrams of synchronization line are shown. For any module, connections to the top or bottom synchronization connectors SYNC can be changed in position if required.

In case of connection of any external devices to synchronization line SYNC you should consider that when there is no load the master module of LTR210 SYNC can send a pulse with peak voltage of up to 11 V to SYNC line.

It is acceptable to connect SYNC line to ADC channel input (for control of synchronization pulse) but it does not make sense because:

- synchronization line status can be inserted in an ADC data stream by internal means of LTR210 as well;
- a valuable characteristic of galvanic isolation of each LTR210 module inputs is lost;

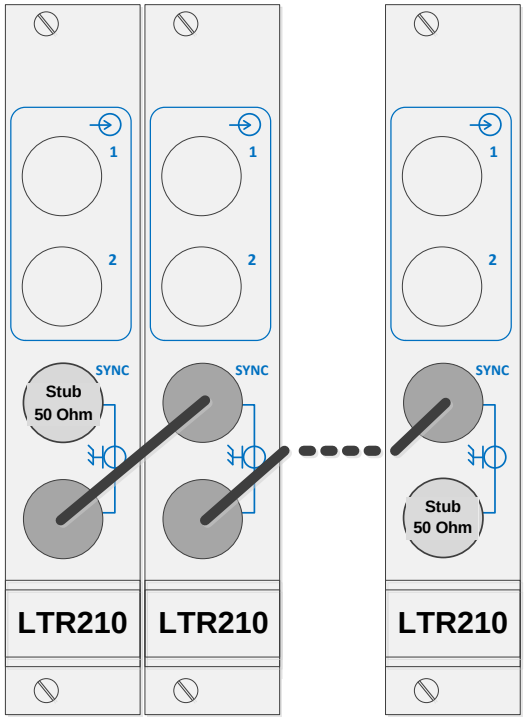


Fig.17-8. "Master-slave" synchronization diagram of LTR210 with full line matching by 50 Ohm plugs at both line ends.

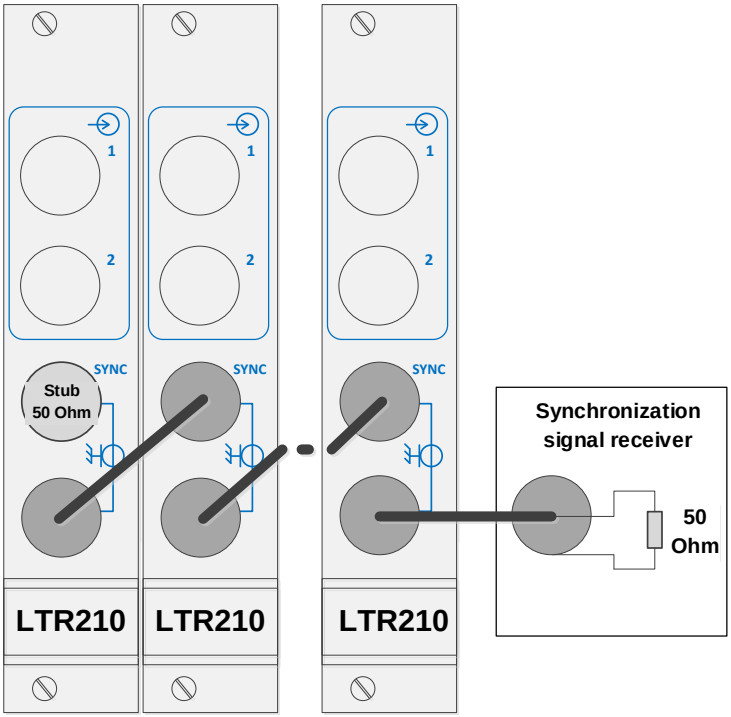


Fig.17-9. "Master-slave" synchronization diagram of LTR210 with an external receiver of synchronization signal with full line matching by 50 Ohm plugs at both line ends.

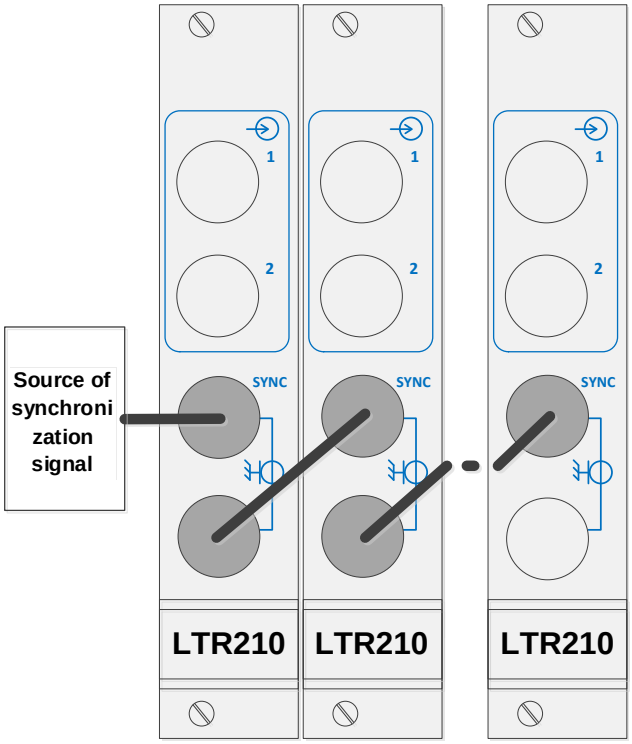


Fig.17-10. Synchronization diagram for "slave" LTR210 modules with partial line matching on the signal source side. Signal source with an output resistance of 50 Ohm us required.

Number of connectable LTR210 modules is limited in this diagram and heavily depends on the matching quality. To improve the matching quality on the side of the line opposite to the synchronization signal source, a load (from 50 to 400 Ohm) can be connected into the line depending on the load characteristic of the synchronization signal source.

17.6.3 Multi-module configurations based on different LTR crates.

SYNC circuit feature of maintaining high level of resistance makes it possible to use synchronization circuits in a multimodule system even when part of LTR210 modules are de-energized.

Regardless of the fact that different LTR crates have different generators of reference ADC conversion frequency (see Appendix A.16, page 359), in the frame-by-frame mode of data acquisition according to the synchronization conditions the difference between signal conversion frequency phases will not be acceptable for a number of tasks.

If the frequency difference of generators in different LTR crates is critical, it can be algorithmically measured and considered by sending the same periodic signal to two ADC channels belonging to different LTR modules and different crates. Using the obtained control samples of these signals, it is possible to define the frequency difference Δf of these signals and make a relative correction Δf/f of data from the "other" LTR crate in further calculations.

17.7 Low-level description of LTR210

In this chapter, a low-level description of LTR210 system of commands is presented. *These data are meant mainly for "advanced" users* who intend to work with LTR210 at the low level (for example, with the use of LTR crate controller when creating autonomous systems).

The protocol of LTR- modules is described in paragraph 4.6.3, page 83. This protocol is specified in detail in the context of LTR210 in the tables below. For program description of LTR210 commands, see the document *"LTR Crate System. Programmer's Manual"* [1].

Note: in the tables below, where bit fields are described, the used letter always refers only to the description of the current data/command format (repetition of letters in different formats does not mean their logical inter-relation).

17.7.1 LTR210 command system

Table17-5. LTR210. Formats of input commands and data.

Command/data to LTR210 (command code, hex)	**Format: bit C, byte 1, byte 2, byte 3**	**Response**	**Description**
LTR210 commads related to CPLD			
STOP (00)	1 00xxxxxx xxxxxxxx xxxxxxxx	No	**Module stop.** The command stops the stream of information from the module and switches it over to the *STANDBY mode and En*_FPGA = 0 *after the completion of the current transmission from the module (if any).* Command without response.
RESET (80)	1 10xxxxxx xxxxxxxx xxxxxxxx	RESET_ RESP	**Module reset.** The command immediately returns all module hardware to the initial state (and the module sends back a module identifier, see .table17-6. The STOP command must always be issued prior to the RESET command.
ROM_IO *[only in the standby mode]* (60)	1 0110000S DDDDDDDD 00000000	Yes	**Low-level access to EEPROM.** **One ROM_IO command implements a 8-bit diagram of the Data protocol of** AT25DF041A **Flash memory.** **The response package contains values at the output of** AT25DF041A for 8 diagram cycles. The command can be executed only at *En*_FPGA = 0. At *En*_FPGA = 1 this command is ignored by the module. Access to EEPROM in the form of a sequence of ROM_IO commands should always end with one STOP command. L-Card provides a ready API-function for reading from EEPROM. The function of recording in EEPROM is not provided to user. S is CS AT25DF041A signal (active level **is** high). Bit-by-bit diagram with 1 byte length is sent to input AT25DF041A: dddddddd **is** data (high-order bit first). SCK signal (8 pulses) is generated automatically by CPLD hardware.
PS_CNTRL (E0)	1 11100000 XXXXXXXX XXXXXXXC	Yes (table below) Response to each command PS_DATA	**Interface Passive Serial(PS) for loading FPGA Cyclone III:** **Control signals:** C – nCONFIG. L-Card provides a ready API-function for FPGA firmware writing.

Command/data to LTR210 (command code, hex)	**Format: bit C, byte 1, byte 2, byte 3**	**Response**	**Description**
PS_DATA (E1)	1 11100001 XXXXXXXX DDDDDDDD	Yes (table below) Response to each command PS_DATA	**Interface Passive Serial(PS) for loading FPGA Cyclone III: Data transfer DATA<7..0> with high-order bit first.** *Byte 1* *DATA<7..0>* *Byte 2:* *DATA<7..0>* *Note: CLK signal for FPGA Cyclone III is generated automatically by hardware.* *L-Card provides a ready API-function for FPGA firmware writing.*
EN_ FPGA (E2)	1 11100010 00000000 0000000e	EN_FPGA_ RESP	**Permission of FPGA logic.** e is En_FPGA bit En_FPGA = 1 means that execution of the commands *listed below in this table* is permitted. En_FPGA = 0 means that execution of the commands *listed below in this table* is not permitted (by default) The permission should be sent after the successful firmware loading to FPGA. On STOP and RESET commands the hardware resets En_FPGA to zero automatically. EN_FPGA has EN_FPGA_RESP response (physically coming from FPGA) only in case of permission of FPGA (e=1). In case of FPGA inhibit there is no response.
LTR210 commads related to FPGA			
SIZE_L (E4)	1 11100100 ssssssss ssssssss		**Setting of size of output data at occurrence of synchronization event** Size <23:0> Size up to 16M-512 samples. ***For bi-channel mode, only even Size should be set***
SIZE_H (E5)	1 11100101 00000000 ssssssss		
SIZE_HIST_L (E6)	1 11100110 ssssssss ssssssss		**Time offset of the start of data output to the history relative to the moment of the synchronization event occurrence.** Size_Hist <23:0> Size of history up to 16M-512 samples ***For bi-channel mode, only even Size_His should be set***
SIZE_HIST_H (E7)	1 11100111 00000000 ssssssss		

Command/data to LTR210 (command code, hex)	**Format: bit C, byte 1, byte 2, byte 3**	**Response**	**Description**
RD_MODE (E8)	1 11101000 **TTT**00GGG E000SSSS		**Register defining the mode of data recept from LTR210 (process of reading from the circular buffer).** **TTT** – rd_traffic: 0 – reading from the buffer at a rate of 500 kS/s; 1 – reading from the buffer at a rate of 200 kS/s; 2 – reading from the buffer at a rate of 100 kS/s; 3 – reading from the buffer at a rate 50 kS/s; 4 – reading from the buffer at a rate of 25 kS/s; 5,6,7 – reading with a physical rate of 10 kS/s. All modes of data reception are operable only when writing to the buffer is enabled (ADC_N_CH_FOR_WR ≠ 0). SSSS – **sync_src**: synchronization event source: **0** – program start of output of SIZE words accumulated in the write buffer at the receipt of PROGRAM_SYNC command. **1** – start of output of SIZE words accumulated in the write buffer **when the signal passes the set level (**SYNC_LEVEL) **in the first ADC channel**. The direction of signal passage is defined by the **edge_mode** field. **2**— start of output of SIZE words accumulated in the write buffer **when the signal passes the set level (**SYNC_LEVEL) **in the second ADC channel**. The direction of signal passage is defined by the field **edge_mode.** **3** – start of output of SIZE words accumulated in the write buffer **on front (drop) to the external synchronization line SYNC.** The edge-drop settings are defined by **edge_mode field. This is digital synchronization from an external source but not from another LTR210 module!** **4 – periodic** start of output of SIZE words accumulated in the write buffer (this mode is equal to periodic oscillograph scanning). The period is defined by registor value **Fps.** **5** – start of output of a continuous data stream as data are written to the buffer. The mode operates correctly only if the following ratio is maintained: Fs*N ≤ 50000 Hz, where Fs is set frequency of ADC channel writing with account for reduction factor, and N is the number of ADC channels defined by WR_CONROL field. **6 -15** are reserved (for future capabilities) E **is edge_mode**: 0 – on signal edge (increasing step); 1 – on signal drop;

Command/data to LTR210 (command code, hex)	Format: bit C, byte 1, byte 2, byte 3	Response	Description
			G— GROUPING (grouping): **0 – INDIVIDUAL** mode at which different LTR210 modules do not send synchronization events to each other. Nevertheless, data reading from several LTR210 modules can be synchronized relative to an external source of synchronization connected to SYNC line. **1 – MASTER, 2 – SLAVE are** modes when the MASTER-LTR210 serves as a source of synchronization event for itself and other SLAVE LTR210 modules. Synchronization event is transmitted by edge of pulse to SYNC line. The MASTER module operates for any **sync_mode,** except **sync_mode = 5.** Value of **sync_src** field makes no effect on the SLAVE-module.
SYNC_LEVEL (E9)	1 11101001 **AA**LLLLLL LLLLLLLL		**Level of synchronization (for the mode when sync_src = 1 or 2) according to the calibrated value of ADC codes**. **AA** “0” LLLLLLLLLLLLL is the lower level of synchronization the of 1-st channel. (To obtain the range of **±16,000 ADC codes**, multiply the level value by 2). “1” LLLLLLLLLLLLL is the upper level of synchronization of the 1-st channel. (To obtain the range of **±16,000 ADC codes**, multiply the level value by 2). “2” LLLLLLLLLLLLL is the lower level of synchronization of the 2-nd channel. (To obtain the range of **±16,000 ADC codes**, multiply the level value by 2). “3” LLLLLLLLLLLLL is the upper level of synchronization of the 2-nd channel. (To obtain the range of **±16,000 ADC codes**, multiply the level value by 2). Note: The "upper" and the "lower" level mean the levels of hysteresis of analog synchronization triggering (paragraph . 17.5.2.2).

Command/data to LTR210 (command code, hex)	**Format: bit C, byte 1, byte 2, byte 3**	**Response**	**Description**
WR_CONROL (EA)	1 11101010 PPPPPPPP 00000**A**WW	**END_ DATA_ STATUS_ RESP** (is sent only when writing is canceled)	**Control of the input pipeline of data recording to the circular buffer.** **WW - ADC_N_CH_FOR_WR<2:0>:** 0 – forbidden (reserved); 1 – writing signal of the 1st channel; 2 – writing signal of the 2nd channel; 3 – writing signal of the 1st and 2nd channel. If WW=0 writing is canceled, a confirmation is sent. **END_DATA_STATUS_RESP** with a writing end attribute: The only correct transition from the state WW≠0 is to the state WW = 0 which is performed only through the writing stop! In case of program reset ,ADC_N_CH_FOR_WR during reading, the reading process is aborted (with sending of a status command). PPPPPPPP is ADC_DCM ADC data reduction factor. In case of pre-set mode of continuous data output **sync_src = 5** , the transition of ADC_N_CH_FOR_WR from zero to non-zero state means enabling the continuous data output of LTR210 to the interface. **A** is **WRITE_AUTO_PAUSE** 1 – sets the mode of automatic pause of writing unless data are not read and further automatic recommencement of writing (this mode makes it possible to obtain the maximum amount of read continuous data of up to 16 million samples) 0 – sets the mode of continuous writing when the maximum possible amount of read data depends on the writing rate (on set ADC frequency) and the number of written channels (the mode makes it possible to react to synchronization events coming at a minimum interval defined by current data reading time)
ADC_MODE (EB)	1 11101011 00000000 T000ffff		**ADC mode control.** **ffff** is ADC_FREQ DIV divider of ADC conversion frequency (the field is accessible for writing only when GO = 0). Frequency of samples from one ADC channel (Hz) will be equal to: $Fs = \frac{10^7}{(ADC\_FREQ+1)*(ADC\_DCM+1)}$ *[Hz]* *For the bi-channel mode, the total frequency of samples written to the buffer will be 2*Fs* **T** is the test mode control (data from the counter for module 63949 (prime number) substitute the ADC data; the data bit depth is conditionally considered as 16-bit, values of calibration factors are taken "by default"). The test mode is generally used for testing of SDRAM, FPGA and LTR-module interface: 0 – test mode is OFF; 1 – test mode is ON. Notes: factors ADC_FREQ and ADC_DCM, correspondingly, make an effect on ADC data and work in the same way as if they were real ADC data.

<table>
<tr><th>Command/data to LTR210 (command code, hex)</th><th>Format: bit C, byte 1, byte 2, byte 3</th><th>Response</th><th>Description</th></tr>
<tr><td>ANALOG_
CONTROL
(EC)</td><td>1
11101100
0BBB0bbb
00MM00mm</td><td></td><td>Control of input analog path.

BBBBBB
bbb – Sub-range of the 1st channel (band1) :
0 –“±10 V”;
1 –“ ±5 V”;
2 –“ ±2 V”;
3 –“ ±1 V”;
4 –“ ±0.5 V”;
5-7 – Installation is forbidden (reserved).

BBB – Sub-range of the 2nd channel (band2):
0 –“ ±10 V”;
1 –“ ±5 V”;
2 –“ ±2 V”;
3 –“ ±1 V”;
4 –“ ±0.5 V”;
5-7 – Installation is forbidden (reserved).

mm – input mode of the 1st channel (inp1_mode):
0 – “measurement of own zero”;
1 – “open input”;
2 – “closed input”.
MM – input mode of the 2nd channel (inp2_mode):
0 – “measurement of own zero”;
1 – “open input”;
2 – “closed input”.</td></tr>
<tr><td>CALIBR_
MEMORY
(ED)</td><td>1
11101101
dddddddd
dddddddd</td><td>W/R</td><td>Calibration factors in FPGA.
Writing of 32 16-bit factors to the factors memory. 32 words of memory reading are sent based on the writing results. It is not allowed to send any packages to LTR210 before receiving the responses, otherwise, the response (32 words) will be aborted. See below the K and B factor formats.
<table>
<tr><th>Address</th><th>Channel</th><th>Factor</th><th>Sub-range</th></tr>
<tr><td>00</td><td>1</td><td>B</td><td rowspan="2">“±10 V”</td></tr>
<tr><td>01</td><td>1</td><td>K</td></tr>
<tr><td>02</td><td>1</td><td>B</td><td rowspan="2">“±5 V”</td></tr>
<tr><td>03</td><td>1</td><td>K</td></tr>
<tr><td>04</td><td>1</td><td>B</td><td rowspan="2">“±2 V”</td></tr>
<tr><td>05</td><td>1</td><td>K</td></tr>
<tr><td>06</td><td>1</td><td>B</td><td rowspan="2">“±1 V”</td></tr>
<tr><td>07</td><td>1</td><td>K</td></tr>
<tr><td>08</td><td>1</td><td>B</td><td rowspan="2">“±0.5 V”</td></tr>
<tr><td>09</td><td>1</td><td>K</td></tr>
<tr><td>0A…0F</td><td colspan="3">Reserved</td></tr>
<tr><td>10</td><td>2</td><td>B</td><td rowspan="2">“±10 V”</td></tr>
<tr><td>11</td><td>2</td><td>K</td></tr>
<tr><td>12</td><td>2</td><td>B</td><td rowspan="2">“±5 V”</td></tr>
<tr><td>13</td><td>2</td><td>K</td></tr>
<tr><td>14</td><td>2</td><td>B</td><td>“±2 V”</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Command/data to LTR210 (command code, hex)</th><th>Format: bit C, byte 1, byte 2, byte 3</th><th>Response</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td>15</td><td>2</td><td>K</td><td></td></tr>
<tr><td>16</td><td>2</td><td>B</td><td rowspan="2">“±1 V”</td></tr>
<tr><td>17</td><td>2</td><td>K</td></tr>
<tr><td>18</td><td>2</td><td>B</td><td rowspan="2">“±0.5 V”</td></tr>
<tr><td>19</td><td>2</td><td>K</td></tr>
<tr><td>1A…1F</td><td colspan="3">Reserved</td></tr>
</table>
</td></tr>
<tr><td>PROGRAM_ SYNC (EF)</td><td>1
11101111
00000000
00000000</td><td></td><td>Program single-shot synchronization.
On arrival of this command to LTR210, an event of the program synchronization occurs.</td></tr>
<tr><td>Fps (F0)</td><td>1
11110000
ffffffff
ffffffff</td><td></td><td rowspan="2">Periodic start frequency control.
ff…ff Fps_code<31:0> defines the frequency of periodic start Fps.
F0 is the lower-order part of 32-bit frequency code
F1 is the upper-order part of 32-bit frequency code
$F_{FPS} = \frac{10^6}{Fps\_code + 1}$ [Hz]
A register can be changed "on the run".
Register F0 should always be written first, register F1 is written next. The written value becomes valid after writing of register F1.</td></tr>
<tr><td>(F1)</td><td>1
11110001
ffffffff
ffffffff</td><td></td></tr>
<tr><td>FPGA_VER (F2)</td><td>1
11110010
00000000
00000000</td><td>FPGA_ VER_ RESP</td><td>FPGA status.
The command returns FPGA firmware version and PLL state flags.</td></tr>
<tr><td>GET_STATUS_ MODE (F3)</td><td>1
11110011
00000000
0000000E</td><td>PERIOD_ STATUS_ RESP</td><td>The command enables in LTR210 periodic (with a 10 ms period) sending of the status word when there is no data transmission, if E=1. If E=0 and "by default", periodic status sending is forbidden.
On commands STOP, RESET and during FPGA loading/reloading, bit E is reset to “0”.</td></tr>
</table>

Command/data to LTR210 (command code, hex)	Format: bit C, byte 1, byte 2, byte 3	Response	Description
DATA0_MODE (F4)	1 11110100 0000SSSS 0000FFFF		**Control of synchronization/digital input logic of ADC1 data format.** FFFF **0** is “0” value. **1** is value of SYNC line (digital input from SYNC line). **2** is function of ADC1 channel data comparator: The value is "1" when in ADC1 channel the signal is above the SYNC_LEVEL threshold, and "0" when it is below the threshold. **3** is function of ADC2 channel data comparator: The value is "1" when in ADC 2 channel the signal is above the SYNC_LEVEL threshold, and "0" when it is below the threshold. **4** – The value is “1” at the moment of triggering of single-shot program or periodic synchronization (if such mode is installed); for other cases the value is “0”. **5-15** – “0” value (reserved for future capabilities) **Control of synchronization/digital input logic of ADC2 data format** SSSS **0** is “0” value. **1** is value of SYNC line (digital input from SYNC line). **2** is function of ADC1 channel data comparator: The value is "1" when in ADC1 channel the signal is above the SYNC_LEVEL threshold, and "0" when it is below the threshold. **3** is function of ADC2 channel data comparator: The value is "1" when in ADC 2 channel the signal is above the SYNC_LEVEL threshold, and "0" when it is below the threshold. **4** – The value is “1” at the moment of triggering of single-shot program or periodic synchronization (if such mode is installed); for other cases the value is “0”. **5-15** is “0” value (reserved for future capabilities).
C0-CF **D0-DF** **F5-FF**			**Reserved commands for further development of FPGA firmware**

Table17-6. LTR210. Formats of outgoing (response) commands.

Command/data from LTR210	Format	Description
RESET_RESP	1 10gggggg 00100010 00100010	**Response to RESET.** Contains a module identifier: in the second and third byte – decimal "210". In the gggggg field, the numberof **CPLD** firmware version of this module is written. **The true number of CPLD firmware will be returned by LTR210 only when EN_FPGA = 0.** **At EN_FPGA =** 1, value of the gggggg field does not make any sense and shall be ignored.

Command/data from LTR210	Format	Description
EN_FPGA_ RESP	1 11100010 00000000 00000001	**Response to EN_FPGA.** **Returns response to the EN_FPGA command** of FPGA permission
FPGA_VER_ RESP	1 11110010 vvvvvvvv 000000FL	**Response to FPGA_VER.** **Returns the number of FPGA version** vvvvvvvv vvvvvvvv FPGA firmware version. "1" is the first version. L is the current status of PLL in FPGA (*pll_lock*): "0" means no PLL capture (FPGA non-operating state); "1" means PLL capture (FPGA operating state). F is the flag indicator of PLL capture hold (*pll_lock_hold*): "0" means that PLL capture disappeared before accessing this register; "1" means that PLL capture has been kept before accessing this register.
ROM_RESP	1 01100000 dddddddd 00000000	**Response to EEPROM reading.** Sent by the module in response to the ROM_IO command. dddddddd **has 8 bit of values of the reading time diagram** AT25DF041A.
PS_RESP	1 11100011 00000000 00000dSC	**Response to FPGA programming.** C is nConfig signal from Cyclone III. S is nSTATUS signal from Cyclone III. d is CONF_DONE signal from Cyclone III.
DATA	In the operating mode: 0 nnnbBBBC sddddddd dddddddY In the test mode (see the register ADC_MODE): 0 nnnbBBB0 sddddddd dddddddd	**Data with additional information.** C is channel number: 0 is data from the 1st channel; 1 is data from the 2nd channel. BBB is range. 0 –"±10 V"; 2 –" ±5 V"; 3 –" ±2 V"; 4 –" ±1 V"; 5 –" ±0.5 V"; 6-7 – (reserved). nnn is the data counter for module 7. *The counter is set for zero by commands STOP or RESET as well as after FPGA (re)loading.* b is an attribute of the start of a continuous data block Range value: the range value is inserted at the moment of synchronization. sddddddddddddddY is ADC data in an additional code from -16384 to +16383. Y is the multifunctional bit of synchronization/digital input. Weights in the format of calibrated data are given in table17-9, page 302.

Command/data from LTR210	Format	Description
PERIOD_ STATUS_ RESP	1 11110011 00000000 **Ww0HMOFL**	**Periodic status word.** **H** is an attribute of history data invalidity (appears when SIZE_HYST≠0 and reading synchronization is occurred with a too short delay relative to the record enable). **Ww** is an attribute of writing for the 2nd channel (W) and the 1st channel (w) “00” – no writing “01” – writing for channel 1 “10” – writing for channel 2 “11” – writing for channels 1 and 2 **M** is an attribute of missing repeated synchronization event “0” means no missing synchronization events “1” means one or more repeated synchronization events are missing **O** is OVERLAP attribute when data are written to SRDAM: “0” means no OVERLAP (normal case) “1” means OVERLAP (read data can be invalid), because the process of writing to SDRAM was in advance of the reading process. **L** is the current status of PLL in FPGA (*pll_lock*) “0” means no PLL capture (FPGA non-operating state) “1” means PLL capture (FPGA operating state) **F** is a flag indicator of PLL capture hold (*pll_lock_hold*) “0” means that PLL capture disappeared before accessing this register “1” means that PLL capture has been kept before accessing this register

Command/data from LTR210	Format	Description
END_DATA_ STATUS_ RESP	1 00000000 **E**0000000 **Ww0HMOFL**	**A status word sent at the end of a data block of the requested size.** **E** is a flag of data writing stop. Package **END_DATA_STATUS_RESP** is always sent with **E=1** at the end of data writing (due to reset ADC_N_CH_FOR_WR). A package with**E=1** flag serves as an attribute of interruption of the current transferring data array and an attribute of its end (perhaps, pre-scheduled end if the amount of transmitted data is less than the Size). **H** is an attribute of history data invalidity (appears when SIZE_HYST≠0 and reading synchronization has occurred with a too short delay relative to the record enable). **Ww** is an attribute of writing for the 2nd channel (W) and the 1st channel (w): “00” – no writing; “01” – writing for channel 1; “01” – writing for channel 2; “01” – writing for channels 1 and 2. **M** is an attribute of missing repeated synchronization event: “0” means no missing synchronization events; “1” means one or more repeated synchronization events are missing. **O** is OVERLAP attribute when data are written to SRDAM: “0” means no OVERLAP (normal case); “1” means OVERLAP (read data can be invalid), because the process of writing to SDRAM was in advance of the reading process. **L** is the current status of PLL in FPGA (*pll_lock*): “0” means no PLL capture (FPGA non-operating state); “1” means PLL capture (FPGA operating state). **F** is a flag indicator of PLL capture hold (*pll_lock_hold*): “0” means that PLL capture disappeared before accessing this register; “1” means that PLL capture has been kept before accessing this register.

Table17-7. LTR210. K calibration coefficient format

Category	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
Weight	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}

Table17-8. LTR210. B calibration coefficient format

Category	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
Weight	S	S	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}
S is extended sign bit of additional code																

Table17-9. LTR210. Format of output calibrated data D_K and internal calibration operation

Category	<15>	<14>	<13>	<12>	<11>	<10>	<9>	<8>	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
Weight	S	2^{14}	2^{13}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	Y

S is sign bit of additional code.

Y is synchronization signal value (see theDATA data format).

In LTR210, internal calibration (in FPGA) is performed according to the formula:

$$Dk = (D + B)*K$$

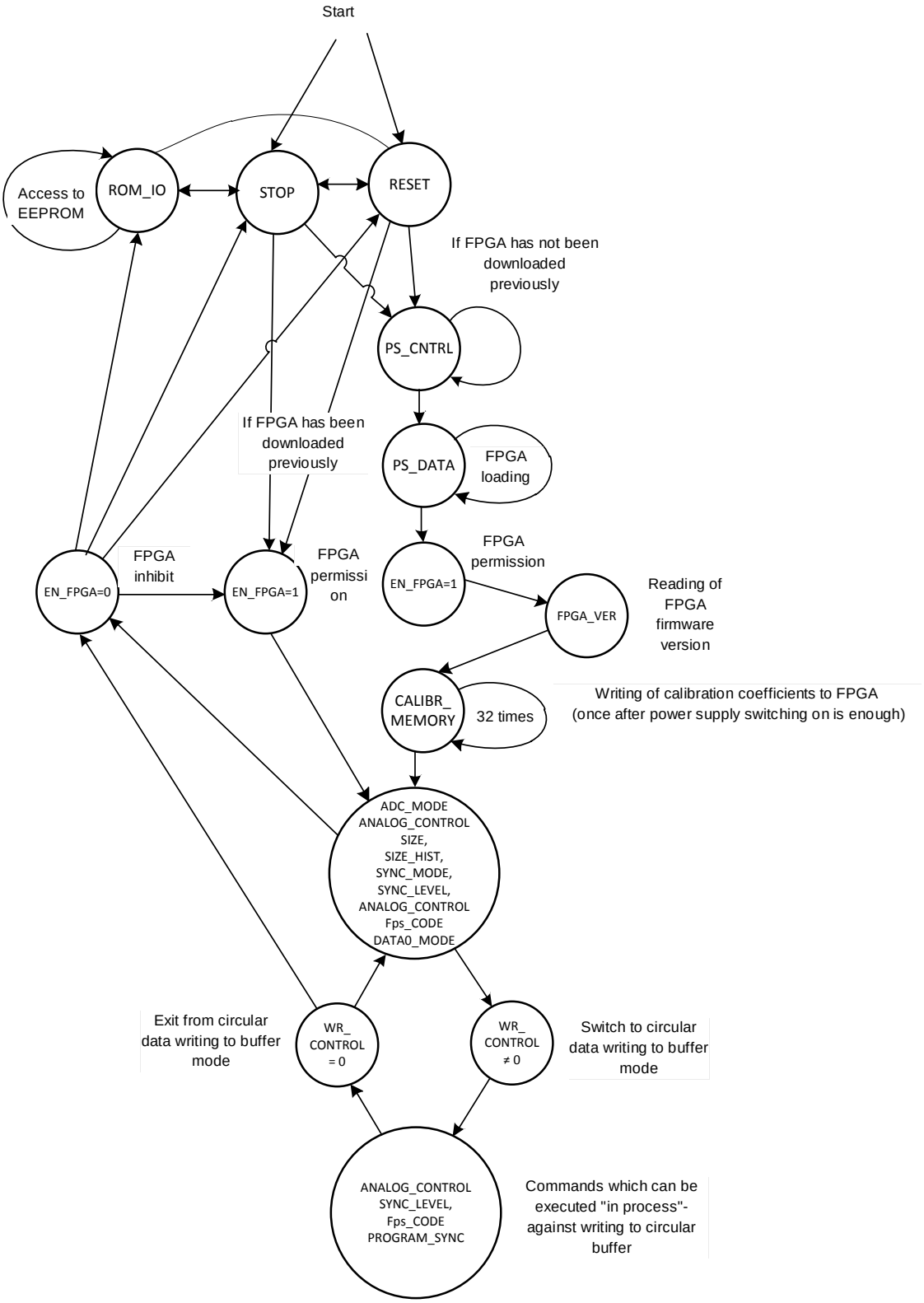
where D is "pure" data of analog-digital converter;

K, B are calibration factors (table17-7, table17-8).

Dk range of output calibrated data representation: from -16384 to +16383.

17.7.2 Permissible sequence of LTR210 commands

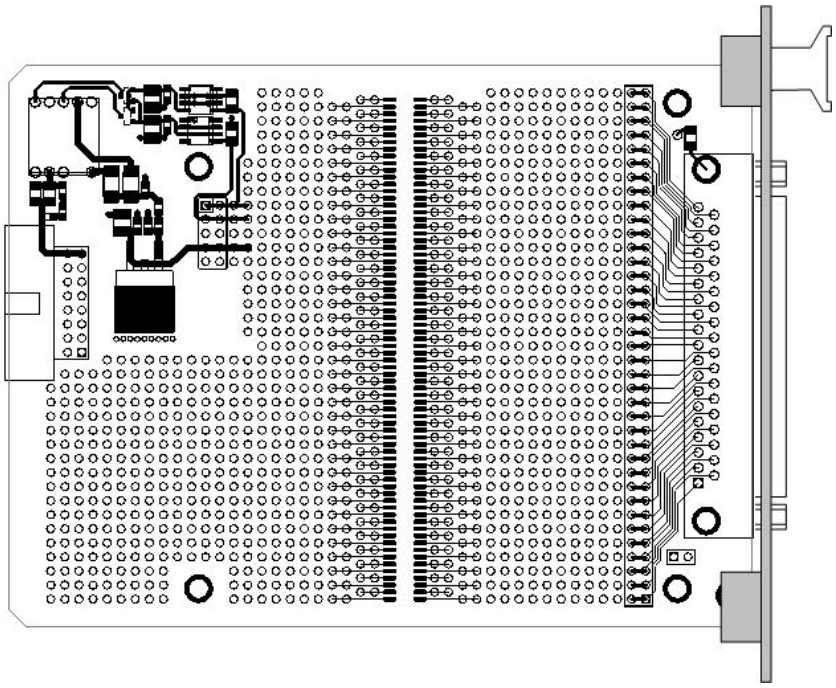
Application of LTR210 command system describe above is subject to some limitations related to the sequence of commands use. The permissible sequence of commands (fig.17-11) defined by LTR210 hardware architecture described in paragraph 17.5 as well as by logic of commands and waiting for response to them as follows from the commands description in paragraph 17.7.1.



Note: The graph does not show the fact that commands STOP and RESET can come in any status and bring LTR210 to its initial state.

Fig.17-11. LTR210. Permissible sequence of commands (graph)

Chapter 18. Prototype module LTR00



LTR00 module is intended for mounting of user nodes (option is available to user). LTR00 board has:

1) Node of stabilized supply source +5 V (0,2 A), +-15 V (2x0,04A) (both having separate galvanic isolation) which can be applied for different demands.

2) Available for order of LTR00 modification:

- Panel of LTR00-01 module has spare DRB-37M connector for user connections.
- Panel of LTR00-02 module is blind and does not have connector.

3) LTR00 has constructive option of mounting the printed-circuit board as per user design (drawings will be provided) as the second level; this board will have PLD/PBD plug connections with carrier board having the possibility of connection to supply circuits, signal circuits from the DRB-37M connector. *This design will give the user opportunity to apply its own printed-circuit board keeping marketable condition of module in whole.*

4) Over the entire free area of LTR00 board there are spare slots for output elements with spacing 2,54 mm and scale of slots SMD with spacing 1,27 mm for narrow SOIC (frame width is 150 mil), there are 4 mounting holes for supports of user board.

See all details on application and limitations of LTR00 module in a separate manual, see L. [6], page 367.

Chapter 19. Special configurations of LTR-modules

This section contains information on specific connections of modules for typical tasks.

19.1 Configuration with LE-41 charge amplifier

Systems of data collection from piezotransducers using a charge amplifier are usually applied in different vibrometry applications. In such applications, the sensor charge is directly proportional to the acceleration, and **charge amplifier function is to ensure proper conversion of physical values of** *charge* **to** *voltage* within the as wide frequency band as possible and then digitize the voltage function by means of ADC. Where necessary, functions of speed and vibration detector coordinates at the defined time interval and with set initial conditions are determined using integration methods during data processing.

It is proposed to use 4-channel external modules of amplifiers LE-41 together with LTR crate. Detailed technical information on LE-41 can be found in the document LE-41. Specification and Operating Manual [9].

If it is intended to control LE-41 input charge sub-ranges, passband and enable specific modes of fault check of sensor's[1] cable and not to use pre-settings of LE-41 (this is also possible), then all LE-41 amplifiers in the system are connected to the common interface RS-485. LTR43 module can serve as a setter for RS-485 and LE-41 modules can serve as executing devices. Individual logic addresses can be written preliminarily in LE-41 in such a way that one executing device will respond to a request from the setter.

It is recommended to use for calculations *calibration factors*LE-41 which can be read from LE-41 via RS-485. If you want to use default calibration factors LE-41 but do not intend to read them from RS-485, then L-Card will provide you with a certificate for particular serial number of the product LE-41, in which precise values of calibration factors will be indicated.

Let us consider two typical examples of LE-41 connection to LTR crate system.

19.1.1 LE-41 – LTR11 – LTR43 configurations

Here, a 16-channel system of data collection from charge sources (piezotransducer) is considered through an example of connection of *4 charge amplifiers LE-41 to one ADC of LTR11 module and to one LTR43* module where amplifiers are powered and controlled via RS-485 interface. The cable diagram for this configuration is shown in Fig.19-1.

[1] it is known to specialists that in multi-channel vibrometry, availability of an automated procedure of cables checking from sensors is important

LTR11 setting for this configuration: 16-channel differential mode, all channels set for sub-ranges ±10 V. In case that ADC frequency is set to 400 kHz for 16-channel mode, we obtain capture frequency of 25 kHz per channel.

The proposed system of charge amplifiers connection is *much more cost-effective per channel* as compared to the alternative option of LTR22 application (paragraph 11.3.1.2, page 306), but in this case the following requirements are raised to the **connection cable:**

- Length of wires (circuits X, Y) from LTR11 to LE-41 shall be maximum 1 m (0.5 m recommended) in order to minimize the impact of *switching interference* (paragraph 5.4.4, page 104).
- Due to the broadbandness of the analog path in LTR11 (lack of any filtering of frequencies which are higher then half of sampling frequency in LTR 11), the differential connections of LTR11 inputs shall be made with great care: pairs of wires X and Y of one channel should be laid as a screened pair (the screen shall be connected with AGND) or unscreened twisted-wire pair.
- To minimize the impact of digital interference from RS-485 on LTR11 inputs, it is recommended to lay the circuits A-B as a twisted pair or a screened pair of wires (it is recommended to connect the screen with AGND).

For laying differential circuits, it is recommended to use screenedwire МГТФЭ 2х0.07. Since the screens must be connected to AGND circuit, the creens of adjacent wires can contact each other inside the cable.

It is obvious that such connections of several LE-41 to the same LTR11 implementing less than 16- channels at a maximum possible frequency of sampling over 25 kHz per channel are possible.

If required to use more than 4- LE-41 modules, the problem of their power supply should be solved. Possible options: an external power supply source, two or more LTR43 (LTR41, LTR42) modules in one LTR crate, additional dummy module LTRN00 (see Table 2.5, page 11). In all cases, power supply circuits will be different for different groups of LE-41.

It is not recommended to connect more than 16 LE-41 amplifiers to one RS-485 interface (for the proposed connection diagram) - (64-channel system).

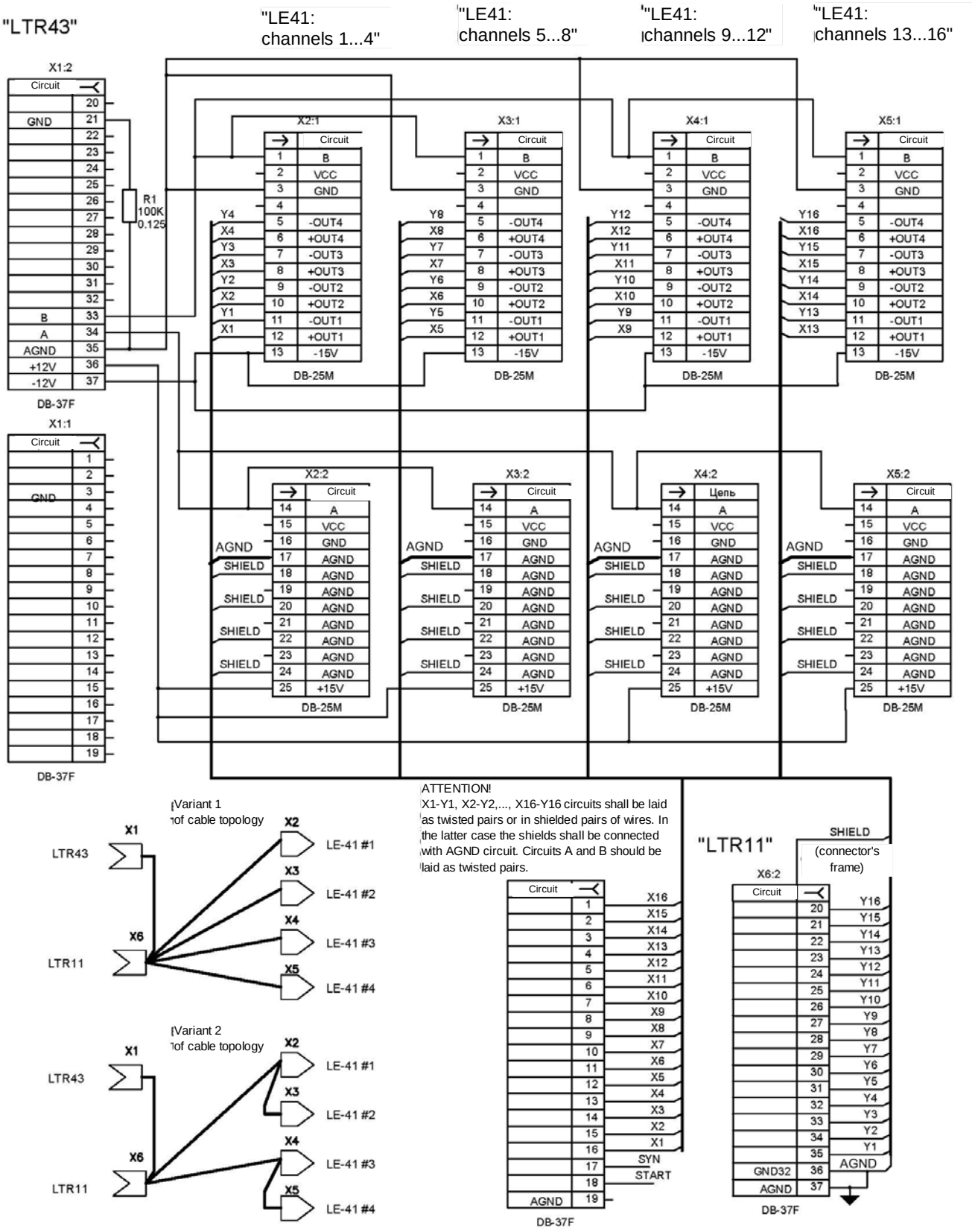


Fig. 19-1
Diagram of cable LE-41 – LTR11 - LTR43

19.1.2 LE-41 – LTR22 – LTR43 configurations

*4*m* - channel connection system will be considered here providing for connection of *m charge amplifiers LE-41 of m ADC modules of LTR22 and one LTR43 module*. Here, the amplifiers LE-41 are controlled via RS-485 interface from LTR43, and each amplifier LE-41 is powered from *its* LTR22. Cable diagram for configuration with *m* amplifiers LE-41 is shown in Fig.19-2.

The proposed diagram potentially is of higher quality in terms of the following characteristics as compared to the previous diagram based on LTR11(paragraph 19.1.2, page 308):

- Better signal/noise ratio mainly due to the proper filtration of input signal inside LTR22 with frequencies higher than half sampling frequency and due to the absence of dynamic switching at LTR22 input and, finally, due to 16-bit ADC as compared to 14-bit ADC in LTR11.
- Better spectral precision of data capture because a sigma-delta ADC is used in LTR22.
- Less time of interchannel passage due to the absence of dynamic switching in LTR22.
- Absence of any phase offset between the processes of data capture in different channels of one LTR22 module due to the strictly parallel data collection in comparison with sequential polling used in LTR11 (there is a possibility of LTR22 modules synchronization for operation without a phase offset).
- Longer connections between LE-41 and LTR crate are potentially possible provided that - the principles of symmetrical differential connection are complied with.

LTR22 setting for this configuration: all channels are set to ±10 V sub-ranges. ADC frequency shall be set for a minimum to provide the smallest passband width sufficient for solution of the assigned task.

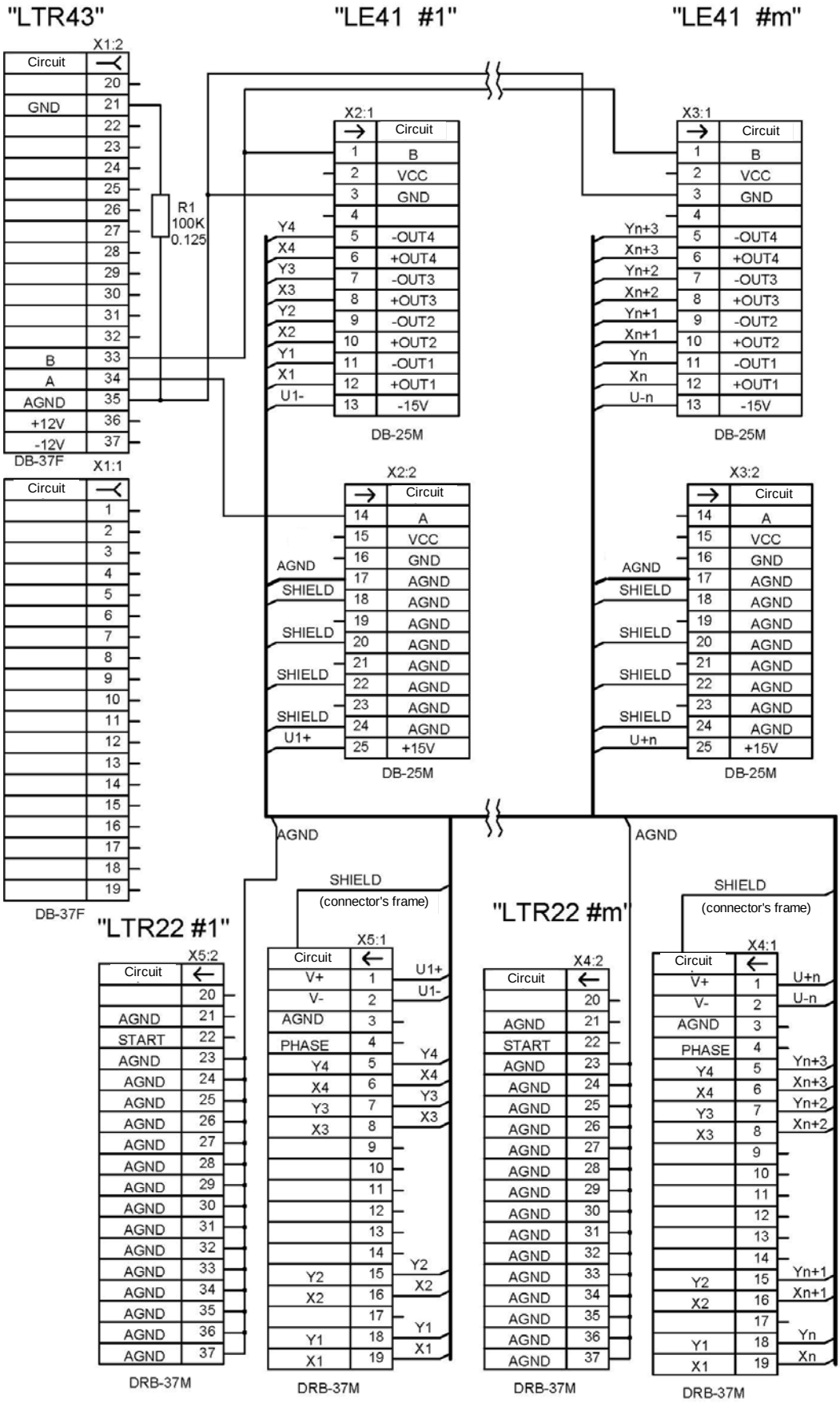


Fig.19-2. LE-41 – LTR22 –LTR43 cable diagram

Chapter 20. Low-level programming of LTR-EU crate

! This chapter is addressed only to highly-qualified users who are set for programming LTR-EU crate at the level of Blackfin processor.

For any further questions related to signal processor ADSP-BF537, refer to the corresponding official documentation of Analog Devices company on website www.analog.com .

20.1 Introduction.

20.1.1 Low-level options provided to the user.

This low-level description of LTR-EU crate controller architecture is meant for users who need to modify L-Card firmware for the following specific purposes:

- Implementation of additional logic of processing of commands and data from LTR modules and sending of control information and data to LTR modules including formation of real-time intercommunications between LTR modules.
- Implementation of additional logic of data transmission between LTR-EU controller and the computer (selection, data transformations, etc.).
- Implementation of additional logic of writing and reading of optional 2GB flash-memory for user data storage.
- Implementation of additional logic of formation and processing of crate external synchronization signals (DIGINx, DIGOUTx).

Correspondingly, the extent of this low-level description architecture does not exceed the limits of the above mentioned purposes.

Actually, this means that the user is allowed to solve the above stated problems within the limits of LTR-EU controller architecture.

- LTR-EU crates have a possibility of JTAG connection for convenient debugging (paragraph 20.3).

20.1.2 What is forbidden for the user?

The user is forbidden to make any changes in the original electrical circuits of LTR-EU controller and perform any actions changing LTR-EU controller architecture. The last-mentioned limitation is also applicable to program peripheral settings of Blackfin processor interfaces (ports) with hardware peripherals used in standard L-Card software and to the method of intercommunication of Blackfin processor with hardware peripherals via interfaces (ports).

! If requirements stated below are violated by the user, L-Card reserves the right to refuse to provide technical support to such user and disclaim the warranty obligations:

From the program point of view, the above-mentioned requirements mean that in the course of L-Card software modification the user shall change the program code in such a way that these

changes do not affect the interfaces of interconnection of peripheral hardware of Blackfin processor within the standard archtecture of the crate controller.

The description of ADSP-BF537 capability assignment for external devices connected to the processor is given below. Use of this information along with commented source L-Card firmware texts (in case that the programmer has necessary qualification) will make it possible to fulfill the listed requirements and to modify LTR-EU crate software correctly.

20.2 Low-level description of LTR-EU crate controller architecture.

Table20-1. Main system parameters of LTR-EU crate controller

Parameter, characteristic	Value, description
Processor	
Processor type	ADSP-BF537KBCZ-6BV
Blackfin processor core frequency	up to 600 MHz
Dynamic power supply of ADSP Blackfin core	implemented
Frequency of processor synchronization input signal (at CLKIN input)	20 MHz (1/3 of crate reference generator frequency)
External (relative to Blackfin) hardware watchdog with the triggering time of about 9 sec	Not present in LTR-EU Board Version = 0 crates Implemented in LTR-EU Board Version ≠ 0 crates (paragraph 4.4.1)
Real-time clock with battery	Not present in LTR-EU Board Version = 0 crates M41T81M6-type clock is present in LTR-EU Board Version ≠ 0 crates
External processor memory	
RAM type	32 MB SDRAM PC133 with 16 MB x 16 bit arrangement
Registers of USB-controller ISP1583	128 controller registers with ISP1583 arrangement (only 16-bit access upon a signal from AMS0 processor).
Data of ISP1583 controller for writing and reading	One 16-bit register (only 16-bit access upon a signal from AMS1 processor).
Type of load FLASH-memory	2 MB DataFlash memory AT45DB161D (connected via SPI, selected by SPISSEL1).
Type of additional (optional) FLASH-memory	2 GB MicroSD (connected via SPI, selected by SPISSEL4).

Table20-2. Peripheral functions of interfaces (ports)

Blackfin PORT	**Initial state**	**Function**
Interface with ISP1583 USB-controller		
PF0 (Board Version = 0) PF1 (Board Version = 1)	input	Engaged in the data transfer logic of ISP1583
PF8, AMS1	input	Engaged in the data transfer logic of ISP1583
PF2	input	Applied as interruption from ISP1583
PG10	output	Applied as reset of ISP1583
PG14, PG15, AMS0	input	Applied in the logic of access to registers ISP1583
External synchronization interface		
PF1, PG13 (Board Version = 0) PF0, PG13 (Board Version = 1)	input	Applied as multipurpose programmable digital inputs-outputs or interruption inputs. PF0 (in Board Version = 1) can be applied as UART0 TX acting as an external channel of communication via DIGOUTx lines of the crate
Interface with load flash-memory (using SPI)		
PF3	input	BOOT SELECT (input is performed in Blackfin software for selection of loading type) In LTR-EU Board Version = 1, this input has an alternative function UART1 RX for implementation of a receiving channel UART via DIGINx lines of the crate
PF10	output	Applied as SPISSEL1 for selection of load flash-memory on SPI interface
Interface of data transfer from Blackfin to LTR modules (using SSC)		
PG11	input	Signal from FPGA about readiness to receive up to 128 (including) 32-bit words from SSC port.
PJ5,PJ11,	outputs	Applied as DT0SEC and DT0PRI of SSC interface.
PJ9,PJ1-	outputs	Applied as DSCLK0 and TFS0 of SSC interface.
Interface of data transfer from LTR modules to Blackfin (using PPI)		
PF9	input	Applied as PPIFS1 (frame pf PPI interface)
PF15	input	Applied as PPICLK (PPI interface synchronization)
PG0,PG1,…,PG7	input	PPI interface data
Control interface between Blackfin and FPGA (using SPI)		
PG12	input	Interruption input (when LTR modules configuration is changed).
PF7	input	Input for a timer for measuring fan rotation frequency
PF5	output	Applied as SPISSEL5 for selection of FPGA register in SPI interface
Interface with a thermometer (using SPI)		
PF4	output	Applied as SPISSEL6 for selection of a temperature sensor in SPI interface
Interface with optional 2 GB Flash-memory		
PF6	output	Applied as SPISSEL4 for selection of 2 GB Flash-memory on SPI interface

Blackfin PORT	Initial state	Function
Common lines of SPI interface		
PF11,	output	Applied as SPI MOSI
PF12,	input	Applied as MISO
PF13	output	Applied as SPI SCK
FPGA loading interface		
PF14	input	Applied for FPGA loading control
PG8	output	Applied for FPGA loading control
PG9	input	Applied for FPGA loading control
MII interface with Ethernet PHY controller		
PH0, PH1, PH15, PJ0, PJ1	In the context of MII interface functions	MII interface with Ethernet PHY controller
Processing of critical events		
NMI	input	An interruption signal (with edge 0->1) is sent to NMI input to prevent de-energizing of the crate controller and to ensure proper shutdown of critical activities (particularly, with flash-memory)
Real-time clock (Board Version ≠ 0)		
PJ2, PJ3, PJ4	input	Lines SCL, SDA of interface I^2C are used for comminication with the real time clock. Line PJ4 can be used as a timer input to which an output interruption line from the clock is connected. Line PJ4 is not used in the regular software
Watchdog (Board Version ≠ 0)		
AMS2	output	Blackfin access to addressing space associated with AMS2 will cause a reset of the watchdog timer. If the watchdog timer reset is not performed within approximately 9 sec, RESET Blackfin is activated from hardware.

Table20-3. Configuration of Blackfin initial loading type.

Signal	State
BMODE0	1
BMODE1	1
BMODE2	0

20.2.1 Registers FPGA on SPI.

Channel 5 of SPI interface is used for access to FPGA registers. Blackfin acts as a setter in this interface (SPI Master). Phases of transmission of address and data of the protocol for access to registers are divided into separate transmission transactions via SPI, but from the point of view of low-level function arguments **AlteraWriteCommand()** and **AlteraReadCommand()** of access to FPGA registers via SPI, 12-bit **address** and 8 bits of **data** are provided for writing (W) and reading (R) of FPGA registers.

Table20-4. FPGA registers

<table>
<tr><th>Address (hex)</th><th>Access</th><th colspan="2">Description of registers fields</th></tr>
<tr><td rowspan="2">000</td><td>W</td><td colspan="2"><0>RESET
“0” is active reset (by default)
“1” is no reset
RESET resets all FPGA logic to the initial state.
While RESET=0, FPGA will be in the reset state.
Starting with Board_Version = 1, FPGA reset is performed not only by means of external button RESET but using a watchdog timer as well.
<7…1> field is reserved</td></tr>
<tr><td>R</td><td colspan="2">Reading of 512 byte of identification string of FPGA firmware from FPGA memory.
Upon the RESET signal, the counter of string read address (inside FPGA) is set to zero. After each reading (in case of passive RESET) the address counter is incremented). The operation of reading of FPGA firmware identification string is executed once after each FPGA firmware loading to the crate.</td></tr>
<tr><td>001</td><td>W</td><td colspan="2"><0> RING_MODE
"0" is normal operating mode
"1" is "ring" test mode: all packages of data and commands sent by Blackfin- via SSC are sent back via PPI, and during this, the channel of information transmission from LTR-modules is closed. The test mode is used for fault check of SSC and PPI interfaces.
<1> AVR_fuse
"0" is normal (user) mode
"1" is process mode with super-slow speed rate (see paragraphs 4.6.3.7, 4.6.3.8, page 87).
<6…2> field is reserved
<7> for Board Version > 0 boards:
“0” – Micro SD card is not inserted (depends on MSD_ON condition)
“1”- Micro SD card is inserted
For boards Board Version = 0 this bit is reserved</td></tr>
<tr><td>002</td><td>W</td><td>SPEED
<7 … 0></td><td rowspan="2">Each bit ofSPEED<15..0> vector with value "0" sets the mode of slow data transmission to LTR modules, and with value "1" the mode of fast transmission is set (see paragraphs 4.6.3.7, 4.6.3.8, page 87). The low-order bit of <0> vector sets the interface speed for the first crate slot (paragraph 3.1, page 33), and thereafter, the bits order from SPEED<1> to SPEED <15> corresponds to the slot number from 2 to 16.
In LTR-EU-2-5 and LTR-EU-8-1 crates, the corresponding high-order bits ofSPEED vector are not used.</td></tr>
<tr><td>003</td><td>W</td><td>SPEED
<15…8></td></tr>
<tr><td>004</td><td>R</td><td>PRESENCE
<7 … 0></td><td rowspan="2">Each bit of vector presence <15..0> with value "0" indicates the absence of[1] LTR-module in a crate slot, and with value "1" it indicates the presence of LTR-module in the slot. The low-order bit of vector PRESENCE<0> relates to the first crate slot (paragraph 3.1, page 33), and further, the bit order from PRESENCE <1> to PRESENCE <15> corresponds to slot numbers from 2 to 16. In LTR-EU-2-5 and LTR-EU-8-1 crates, the corresponding high-order bits of vector PRESENCE are not used.</td></tr>
<tr><td>005</td><td>R</td><td>PRESENCE
<15 … 8></td></tr>
</table>

[1] or a major failure of interface or power supply system of LTR-module

Address (hex)	Access	Description of registers fields
007	W/R	**RG_TEST** <7..0> This is a test register available for reading and writing which is used for FPGA diagnostics after its loading and for diagnostics of SPI channel for communication with FPGA. This register makes no effect on the rest logic of FPGA operation. At first reading of this register upon the RESET signal the read value will contain **Board Version**: "0" is **Board Version = 0** "1" is **Board Version = 1** values "2"..."255" are reserved
008	W	**LED1**<1..0> - direct control of LED "U" on the crate panel: "0" or "3" – no light; "1" – red; "2" – green. **LED2**<3..2> - direct control of LED "E" on the crate panel: "0" or "3" – no light; "1" – red; "2" – green. After sending the **RESET** command, fields LED1 and LED2 are reset.
009	W	Register of outputs permissions: <0> **DIGOUT_OE** "0" – inhibit (Z-state) of signals DIGOUT1 and DIGOUT2 output "1" - permission of signals DIGOUT1 and DIGOUT2 output. <1> **PF1_OE (PF0_OE)** "0" – inhibit (Z-state) of FPGA output to the line PF1 of Blackfin (Board Version = 0), and to the line PF0 of Blackfin (Board Version = 1) "1" - permission of FPGA output to the line PF1 of Blackfin (Board Version = 0), and to the line PF0 of Blackfin (Board Version = 1) <2> **PG13_OE** "0" – inhibit (Z-state) of FPGA output to the line PG13 of Blackfin "1" - permission of FPGA output to the line PG13 of Blackfin <7..3> field is reserved
00A	W	**DIGOUT1_SRC** <7..0> - Setting signal source DIGOUT1 "0" – constant "0" "1" – constant "1" "2" – PF1 (Board Version = 0), PF0 or UART0 TX (Board Version = 1) "3" – PG13 "4" – DIGIN1 (translates the status) "5" – DIGIN2 (translates the status) "6" – START tag "7" – 1s tag "8",…,"255" values are reserved

Address (hex)	Access	Description of registers fields
00B	W	**DIGOUT2_SRC**<7..0> - Setting signal source DIGOUT2 "0" – constant "0" "1" – constant "1" "2" – PF1 (Board Version = 0), PF0 or UART0 TX (Board Version = 1) "3" – PG13 "4" – DIGIN1 (translates the status) "5" – DIGIN2 (translates the status) "6" – START tag "7" – 1s tag "8",…,"255" values are reserved
00C	W	<0>**PF1_SRC (PF0_SRC)** - Setting signal source FPGA on the line PF1 of Blackfin (Board Version = 0), PF0 of Blackfin (Board Version =1) (permission of FPGA output is controlled by bit **PF1_OE (PF0_OE)**) "0" – FPGA translates line DIGIN1 status to PF1 "1" – FPGA translates line DIGIN2 status to PF1 **<4> PF3_SRC -** Setting FPGA signal source on the line PF3 (UART1 RX) of Blackfin (supported for Board Version >0) 0 - DIGIN1 1 – DIGIN2 <7..1> field is reserved, except for **<4> in** Board Version >0
00D	W	<0>**PG13_SRC** Setting FPGA signal source on the line PG13 of Blackfin (permission of FPGA output to the line PG13 is controlled by bit **PG13_OE**) "0" – FPGA translates line DIGIN1 status to PG13 "1" – FPGA translates line DIGIN2 status to PG13 <7..1> field is reserved
00E	W	Control of insertion of synchronization tag START at the level of modules interface (imitation of LTR43 module) but a package is sent in the format of service command between the crate controller and the computer (paragraph 4.6.5, page 90). **START_SRC**<7..0> 0 – inhibit of START tag 1 – START tag is sent from DIGIN1 signal edge 2 – START tag is sent from DIGIN1 signal drop 3 – START tag is sent from DIGIN2 signal edge 4 – START tag is sent from DIGIN2 signal drop 5 – START tag is sent when this value is written to the register 6…255 – reserved

Address (hex)	Access	Description of registers fields
00F	W	Control over insertion of synchronization tag m1s (second synchronization tag) at the level of modules interface (imitation of LTR43 module) but a package is sent in the format of service command between the crate controller and the computer (paragraph 4.6.5, page 90). **M1S_SRC**<7..0> 0 – inhibit of m1s tag 1 – m1s tag is sent from DIGIN1 signal edge 2 – m1s tag is sent from DIGIN1 signal drop 3 – m1s tag is sent from DIGIN2 signal edge 4 – m1s tag is sent from DIGIN2 signal drop 5 – m1s tag is sent when this value is written to this register 6 – The tag is sent at 1 second interval until another value of this register is set. The initial phase of the first second tag is referenced directly to the moment of writing this value to this register. 7…255 – reserved
010… FFF		Adresses reserved. Access is prohibited.

Notes to the table:

- It is recommended to write zero values to the bit fields of registers which are reserved *for writing* in order to have a definite possibility to assign these fields with new context after FPGA firmware update.
- Value of a reserved bit of the register field *for reading* can be uncertain and is prohibited for use.
- When reading a register with "W" type access, the value of a read byte is not defined.
- Writing to a register with "R" type access makes no effect on FPGA operation logic.

20.2.2 Typical examples of settings of digital LTR-EU crate interface

20.2.2.1 Modes of synchronization and input-output

Here are some examples of settings of registers fields (table 2-1) for cases when digital lines DIGINx, DIGOUTx are used for synchronization according to "second tag", "start tag" or for digital input-output.

Table20-5. START TAG synchronization modes

Bit fields of FPGA registers, table20-4	Values of bit fields for START TAG synchronization modes							
	"Inhibit of START tag"	"Internal" (see the note)			"External"			
		without trans-lation	with trans-lation to DIGOUT1 output	with trans-lation to DIGOUT2 output	from DIGIN1 signal edge	from DIGIN1 signal drop	from DIGIN2 signal edge	from DIGIN2 signal drop
DIGOUT1_SRC	X	X	"6"	X	X	X	X	X
DIGOUT2_SRC	X	X	X	"6"	X	X	X	X
START_SRC	"0"	"5"	"5"	"5"	"1"	"2"	"3"	"4"
DIGOUT_OE	X	X	"1"	"1"	X	X	X	X

Note: "Internal synchronization" – from the moment of writing to the register START_SRC of value “6”..

Table 20-6. SECOND TAG synchronization modes

Bit fields of FPGA registers, table20-4	Values of bit fields for SECOND TAG synchronization modes							
	"Inhibit of START tag"	"Internal" (see the note)			"External"			
		without trans-lation	**with transla-tion to DIGOUT1 output**	**with transla-tion to DIGOUT2 output**	**from DIGIN1 signal edge**	**from DIGIN1 signal drop**	**from DIGIN2 signal edge**	**from DIGIN2 signal drop**
DIGOUT1_SRC	X	X	"7"	X	X	X	X	X
DIGOUT2_SRC	X	X	X	"7"	X	X	X	X
M1S_SRC	"0"	"6"	"6"	"6"	"1"	"2"	"3"	"4"
DIGOUT_OE	X	X	"1"	"1"	X	X	X	X

Note: "Internal synchronization" – from the moment of writing to the register M1_SRC of value “6”.

Table 20-7. Modes of DIGOUT1 output

Bit fields of FPGA registers, table20-4	Values of bit fields for control of DIGOUT1 output modes								
	Inhibit of output (Z-state)	**level "0"**	**level "1"**	**PF1 (PF0, see the note)**	**PG 13**	**DIGIN1**	**DIGIN2**	**START TAG**	**SECOND TAG**
DIGOUT1_SRC	X	"0"	"1"	"2"	"3"	"4"	"5"	"6"	"7"
DIGOUT_OE	"0"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"
PF1_OE (PF0_OE, see the note)	see paragraph 20.2.3			"0"		see paragraph 20.2.3			
PG13_OE	see paragraph 20.2.3				"0"	see paragraph 20.2.3			

Note: The indication in brackets is for Board Version > 0

Table20-8. Modes of DIGOUT2 output

Bit fields of FPGA registers, table20-4	Values of bit fields for control of DIGOUT2 output modes								
	Inhibit of output (Z-state)	**level "0"**	**level "1"**	**PF1 (PF0, see the note)**	**PG 13**	**DIGIN1**	**DIGIN2**	**START TAG**	**SECOND TAG**
DIGOUT2_SRC	X	"0"	"1"	"2"	"3"	"4"	"5"	"6"	"7"
DIGOUT_OE	"0"	"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"
PF1_OE (PF0_OE, see the note)	see paragraph 20.2.3			"0"		see paragraph 20.2.3			
PG13_OE	see paragraph 20.2.3				"0"	see paragraph 20.2.3			

Note: The indication in brackets is for Board Version > 0

Table20-9. Use of PF1 (PF0) Blackfin port

Bit fields of FPGA registers, table20-4	PF1 (PF0) Blackfin port configuration			
	"For input"			"For output" for control of DIGOUT1, DIGOUT2, see table 20-7, table20-8.
	initial state (by default)	PF1(PF0) <= DIGIN1 (digital input or at interruption)	PF1(PF0) <= DIGIN2 (digital input or at interruption)	
PF1_OE (PF0_OE)	X	"1"	"1"	"0"
PF1_SRC (PF0_ SRC)	X	"0"	"1"	X

Note: The indication in brackets is for Board Version > 0

Table20-10. Use of PG13 Blackfin port

Bit fields of FPGA registers, table20-4	PG13 Blackfin port configuartion			
	"For input"			"For output" for control of DIGOUT1, DIGOUT2, see table 20-7, table20-8.
	initial state (by default)	PG13 <= DIGIN1 (digital input or at interruption)	PG13 <= DIGIN2 (digital input or at interruption)	
PG13_OE	X	"1"	"1"	"0"
PG13_SRC	X	"0"	"1"	X

20.2.2.2 Setting for operation with transmitter-receiver RS-485/422↔UART

Here is an example of setting of registers fields values (table 2-1) for the case pf connection of transmitter-receiver RS-485/422↔UART. Supported for Board Version >0

Address (hex)	**Access**	**Value of registers fields** (table 2-1)	**Note**
009	W	<0> **DIGOUT_OE = 1** <1> **PF0_OE = 0** <2> **PG13_OE = 0**	Permission for DIGOUT1, DIGOUT2 output. Inhibit for FPGA to set active levels on PF0 and PG13.
00A	W	**<7..0> DIGOUT1_SRC = 2**	UART0 TX Blackfin → DIGOUT1 (UARTO transmission channel to the line RS-485 or RS-422)
00B	W	**<7..0> DIGOUT2_SRC =3**	PG13 Blackfin → DIGOUT2 PG13 = 1 – permission of RS-485 transmitter output. PG13 = 0 – inhibit of RS-485 transmitter output. For RS-422 should be PG13=1 constant.
00C	W	<0> **PF0_SRC = X** **<4> PF3_SRC = 0**	UART1 RX Blackfin ← DIGIN1 (UART1 receiving channel from the line RS-485 or RS-422)
00D	W	<0> **PG13_SRC = X**	
00E	W	**<7..0> START_SRC = 0**	Inhibit of "start tag"
00F	W	**<7..0> M1S_SRC = 0**	Inhibit of "second tag"

20.2.3 "Output to output" collisions.

The following combinations of settings represent inadmissible states:

- PF1_OE (PF0_OE) = 1 simultaneous with setting for PF1 Blackfin port output
- PG13_OE = 1 simultaneous with setting for PG13 Blackfin port output
- DIGOUT_OE = 1 simultaneous with another active output connected to DIGOUT1 or DIGOUT2 output.

Change of program peripheral setting of interfaces (ports) of Blackfin processor used in regular L-Card software as well as change of the mode of interaction between Blackfin processor and peripheral devices via the interfaces (ports) (paragraph 20.1.2) can also result in occurrence of inadmissible "output to output" collisions.

20.3 JTAG application.

For debugging Blackfin software of LTR-EU crates, L-Card proposes to use one of JTAG-emulators: ADZS-USB-ICE, ADZS-HPUSB-ICE or ADZS-ICE-100B with USB interface (table 2-6, page 32). They differ significantly with USB transfer rate and price. You can get information on these devices on the manufacturer's website www.analog.com .

Controllers boards of LTR-EU crates have a JTAG connector fig.20-1compatible with the above mentioned JTAG-emulators.

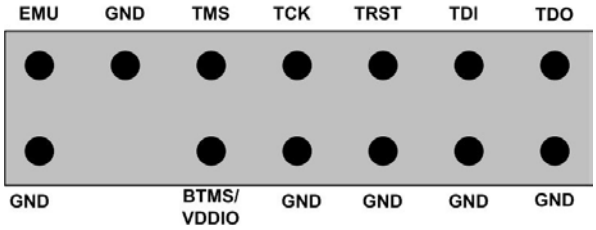


Fig.20-1. JTAG

It should be highlighted that in crates LTR-EU-8(16) Board Version = 0 (paragraph 4.4.1) (and also in LTR-EU-2-5), connection of a JTAG emulator is **a complicated operation from the technical point of view** because to access the JTAG connector in LTR-EU-2-5 crate, one has to remove the top frame cover (in LTR-EU-8-1, LTR-EU-16-1 crates - bottom cover); that is why debugging of crate software requires specific non-operating (in terms of operation) crate condition.

In crates LTR-EU-8(16) Board Version = 1, there is an access hole with "JTAG" marking in the bottom cover, under the removable cover of which there is a connector for connection of JTAG emulator.

! Connection or disconnection of JTAG-emulator connector to LTR-EU crate should be performed when both devices are de-energized and with previously connected grounding circuits of the computer (to which JTAG-emulator is connected) and LTR crate (for grounding, see paragraph 3.6.4). Non-observance of these rules can cause an equipment failure!

! In case of any defects and malfunctions related to incorrect and inappropriate product disassembly/assembly, the warranty liability of L-Card for this product will be terminated.

! When using JTAG-emulator in controllers of crates LTR-EU Board Version ≠ 0 (paragraph 4.4.1), an *alternative type of processor loading* (by holding the RESET button for at least 10 sec, sub-paragraphs 3.2.3, 3.2.5) should be used at which the watchdog timer is prohibited as it interferes with normal running of JTAG session.

In crates LTR-EU Board Version = 0 without a hardware watchdog (external one relative to Blackfin), alternative loading mode does not have any hardware peculiarities, so in these crates JTAG session will run properly for any loading option.

! Use of relatively cheap frameless JTAG-emulator ADZS-ICE-100B with LTR-EU requires using a special extension -cable LTR -JTAG (fig.20-2, table 2-5). Proceed *with extreme caution when handling this JTAG -emulator*: a short circuit of open parts of JTAG-emulator on LTR-EU crate frame is inadmissible as well as on any internal circuits of the crate. Note that from both sides of LTR-JTAG cable there is structural element (pulled out plug contact and plugged hole of socket) showing the orientation of connectors during connection.

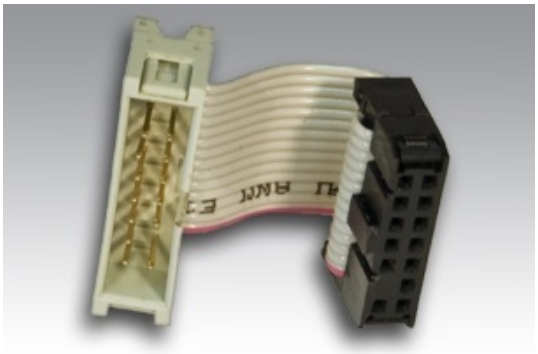


Fig.20-2. LTR-JTAG cable

General comments:

1. It should be admitted at once that use of **JTAG in LTR** is not absolutely but **conditionally possible** for the user under condition of compliance with the above mentioned requirements. Like all other issues set out in the present chapter, this issue requires a quite competent approach from the user.

2. This low-level description will be updated in the next revisions of the manual with data required for solution of user tasks of low-level programming of LTR crate controller. You can send your comments on updating the low-level description with necessary information to support@lcard.ru .

Appendix A. Specifications

This Appendix contains a list of LTR crate system specifications under normal operating conditions (Appendix A.19, page 324).

If LTR crate or separate LTR modules were kept under maximum permissible weather conditions, they should be kept under normal conditions for minimum 3 hours prior to switching on.

To provide the claimed accuracy characteristics the measuring system shall be warmed-up for 15 min.

All below mentioned crate characteristics correspond to connection to standard USB 2.0 full-speed port via optional USB- cable included in the scope of supply.

General instructions on operation with electrical appliances shall be observed when working with LTR crate system.

A.1. Module LTR11.

! Performance limits and additional characteristics of signal lines are presented in paragraph 5.4.1, page 324.

A.1.1. LTR11 specification

Parameter	Value
Number of channels	6 differential or 32 with common ground (single-phase)
Sub-ranges of input signal measurements	±10 V, ±2.5 V, ±0.6 V, ±0.15 V
Maximum ADC conversion frequency	400.0 kHz
In-phase signal voltage	±10 V (does not depend on the sub-range)
ADC bit depth	14 bits
The bit depth calculated according to the signal/noise ratio at the grounded input at ADC frequency of 100 kHz	in the sub-range: – ±10 V 12.8 bits – ±2.5 V: 12.8 bits – ±0.6 V 12.5 bits – ±0.15 V 12.0 bits
The bit depth calculated according to the signal/(noise+harmonics) ratio obtained during digitizing of sinusoidal signal with a frequency of 1 kHz and 2.5 V amplitude at ADC frequency of 100 kHz	sub-range 2.5 V: 12.2 bits
The limits of the permissible systematic component of main reduced (to final value of sub-range) error of DC voltage measurement:	– +0.05% in sub-ranges 2.5 V and 10 V; – ±0.1% in sub-range 0.6 V; – ±0.5% in sub-range 0.15 V.

Parameter	Value
The limit of permissible mean-square deviation of the random component of main reduced (to final value of sub-range) error of DC voltage measurement:	– 0.05% in sub-ranges 2.5 V and 10 V; – 0.1% in sub-range 0.6 V; – 0.5% in sub-range 0.15 V.
Common-mode rejection factor[1] 50 Hz in the differential mode, min.	70dB
Common interference suppression factor[2]at 50 Hz in the differential mode, min.	100 dB
Input resistance in case of single-channel input	min. 10 MOhm in the operating mode in the range of input voltage ±10 V
Integral non-linearity of conversion	Max. ±1.5 power reactivity margin
Differential non-linearity of conversion	Max. –1 to +1.5 power reactivity margin
Inter-channel transmission of 1 kHz sinusoidal signal of in the range ±10 V at ADC actuation frequency of 400,0 kHz and internal resistance of signals sources equal to 50 Ohm, see also Table A.1.2.	-92 dB
Galvanic isolation characteristics	Appendix A.18, page. 362
Characteristics of START and SYNC synchronization inputs: – logic zero level, max. – logic one level, min. – pull-up resistor – offset duration – pulse duration, minimum	 0.5 V 2.4 V 20 kOhm relative to GND unlimited 250 ns

A.1.2. Inter-channel passage

Typical values of inter-channel passage of 1 kHz sinusoidal signal depending on the range, ADC run frequency and internal resistance of signal sources are given below.

ADC conversion frequency (kHz)	Channel polling time, µs	Signal source resistance	Inter-channel passage (typical value), sinusoidal signal 1 kHz
50	20	50 Ohm	in the sub-range: – ±10 V:< -100 dB – ±2.5 V:< -100 dB – ±0.6 V: -93 dB – ±0.15 V: -90 dB
100	8.38	50 Ohm	in the sub-range: – ±10 V:< -92 dB – ±2.5 V:< -92 dB – ±0.6 V: -90 dB – ±0.15 V: -60 dB
50	20	5 kOhm	in the sub-range: – ±10 V:< -88 dB – ±2.5 V:< -88 dB – ±0.6 V: -88 dB – ±0.15 V: -87 dB

[1] for interference applied to the input relative to AGND circuit at unbalance of resistances of external input circuits equal to 1 kOhm

[2] for interference applied to the input relative to LTR grounding terminal at unbalance of resistances of external input circuits equal to 1 kOhm

ADC conversion frequency (kHz)	Channel polling time, µs	Signal source resistance	Inter-channel passage (typical value), sinusoidal signal 1 kHz
100	8.38	5 kOhm	in the sub-range: – ±10 V:< -77 dB – ±2.5 V:< -77 dB – ±0.6 V: -76 dB – ±0.15 V: -53 dB
50	20	20 kOhm	in the sub-range: – ±10 V:< -60 dB – ±2.5 V:< -60 dB – ±0.6 V: -60 dB – ±0.15 V: -58 dB
100	8.38	20 kOhm	in the sub-range: – ±10 V:< -25 dB – ±2.5 V:< -25 dB – ±0.6 V: -23 dB – ±0.15 V: -22 dB

A.2. Module LTR212(M)

Performance limits and additional characteristics of signal lines are presented in paragraph 6.4.2, page 327.

A.2.1. LTR212(M) specification

Parameter	Value
Value of RVS input voltage (at contacts -EXC, +EXC) on the load with a resistance of min. 12.5 Ohm (equivalent to supply of up to 8 measuring bridges, 100 Ohm each)	(2.5 ± 0.1) V, (5.0 ± 0.2) V
Range of bridge unbalance voltage measurements	from 0.001 to 80 mV
The range of input in-phase voltage relative to the bridge supply point with the minimum potential:	
– for set voltage of reference voltage source of 2.5 V	$(0{,}5\ldots1)*(U_{EXC}^{max}-U_{EXC}^{min})$ [1]
– for set voltage of reference voltage source of 5.0 V	$(0{,}25\ldots0{,}75)*(U_{EXC}^{max}-U_{EXC}^{min})$
Measurements sub-ranges	±80 mV, ±40 mV, ±20 mV, ±10 mV, 0...80 mV, 0...40 mV, 0...20 mV, 0...10 mV
The limits of permissible main relative error (not involving zero calibration operation)	
– for sub-ranges ±40 mV, ±80 mV, 0…80 mV	$\pm\left[0{,}05+0{,}015\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$ %
– for sub-ranges 0…40 mV, ±20 mV	$\pm\left[0{,}07+0{,}02\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$ %
– for sub-ranges 0…20 mV, ±10 mV, 0…10 mV	$\pm\left[0{,}1+0{,}05\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$ %
	Symbols: X_K – final value of the set measurement sub-range, V; X – reading of LTR212, V
The range of bridge initial unbalance compensation	Minimum 1.5% of the rated value of bridge supply voltage
Common-mode rejection factor in case of unbalance of external input circuits resistances equal to 1 kOhm: – for DC voltage relative to LTR frame – for AC voltage of 50 Hz frequency realative to LTR frame	 minimum 100 dB minimum 100 dB
Conversion frequency stability[1]	±50 ppm in operating conditions

[1] U_{EXC}^{max}, U_{EXC}^{min} is, accordingly, the maximum and the minimum voltage value in the pair of voltages of bridge supply +EXC and -EXC. An option of reversed voltage of bridge supply is considered here as well.

Parameter	Value
Input bias current	Maximum 50 nA
Input resistance	Minimum 10 MOhm
Resistance to short circuit of the reference voltage source	Minimum 1 min
Power consumption when 8 bridges of 100 Ohm resistance each and reference voltage source voltage of 5 V are connected, max.	5.5 W
Galvanic isolation characteristics	Appendix A.18, page. 362

A.2.2. Amplitude-frequency characteristics of LTR212(M)

A.2.2.1. Mean accuracy mode

Base sampling rate in this mode is 7,680 Hz.

Amplitude-frequency characteristic (*AFC*) of the channel when filtration in DSP is disabled at a sampling rate of 7680 Hz is shown in Fig.A. 20-13. Algorithms of two filters operating sequentially are implemented in DSP for further signal filtration:

Second-order infinite-impulse response -filter- balancing the initial AFC within the set frequency band to the accuracy of ≈ 0.02 dB;

Finite-impulse response- filter of at least 215-th order limiting channel passband at the set level. Finite-impulse response- algorithm includes operation of decimation (i.e. "reduction" of data stream) resulting in (7600/K) Hz of data output frequency at the filter output, where K- is decimation factor. Passband of the finite-impulse response- filter can be selected from the range of 25 Hz, 70 Hz, 258 Hz, 456 Hz, 675 Hz or both filters can be disabled.

Resulting AFC with additional filters enabled for each of the specified cutoff frequencies are shown in the corresponding figures below. Characteristics of the module depending on the filtration mode are presented in TableA.20-11:

Table A.20-11
Characteristics of filters

Filter	disabled	25 Hz	70 Hz	258 Hz	456 Hz	675 Hz
Order of the finite-impulse response -filter		229	225	217	221	229
File name		d212_85	d212_160	d212_345	d212_545	d212_760
Decimation factor		40	24	11	7	5
Data output frequency, Hz	7600.0	190.0	316.67	690.91	1085.71	1520.0
Passband by level – 3 dB, Hz	2,000	25	72	259	460	680
Beginning of attenuation band, Hz		85	160	345	545	760

[1] LTR212 is the only LTR module having its own generator which sets the conversion frequency. A reduced parameter should be used to estimate the maximum offset of conversion frequencies phases of different LTR212 modules. However, new LTR212M modifications are already synchronized relative to the single LTR crate generator.

Filter	disabled	25 Hz	70 Hz	258 Hz	456 Hz	675 Hz
Signal suppression in the attenuation band, dB		55	65	58	59	55

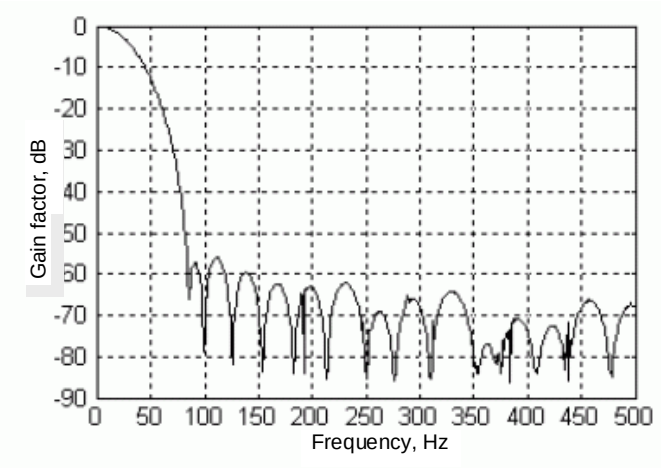


Fig. A. 20-3
LTR212(M). AFC with 25 Hz finite-impulse response -filter

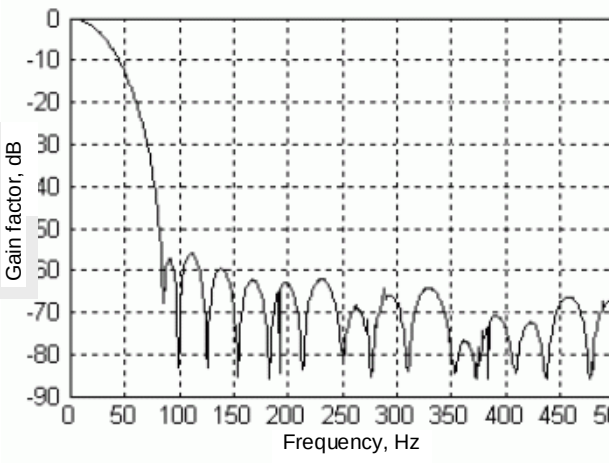


Fig. A .20-4
LTR212(M). AFC with infinite-impulse response- filter and 25 Hz finite-impulse response -filter

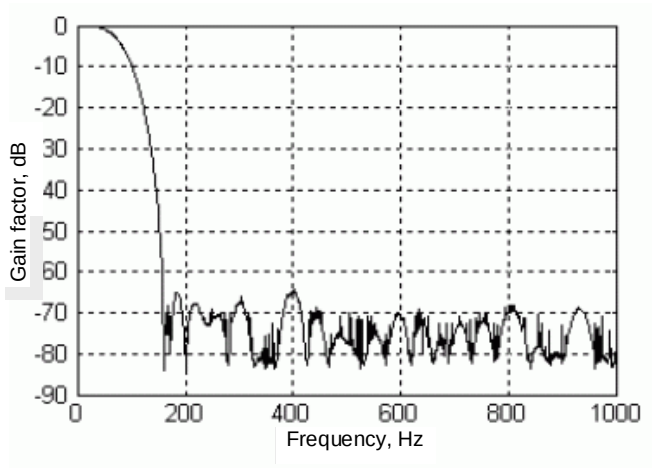


Fig. A. 20-5
LTR212(M). AFC with 70 Hz finite-impulse response- filter

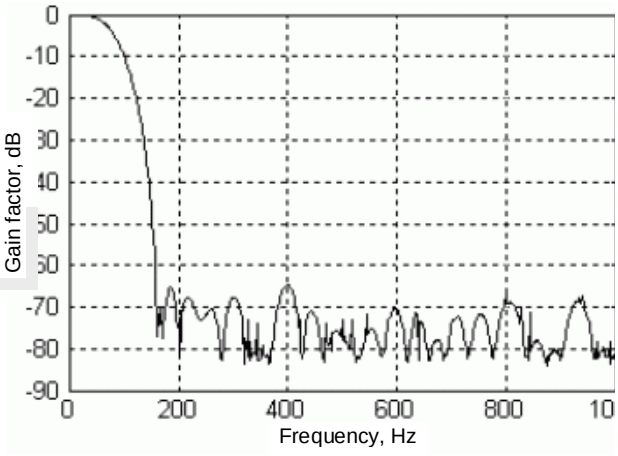


Fig. A. 20-6
LTR212(M). AFC with infinite-impulse response- filter and 70 Hz finite-impulse response -filter

AFC at disabled filters is shown in Fig.A. 20-13.

A.2.2.2. Four-channel high-accuracy mode

Program filters are not applied in this mode.

AFC in the high-accuracy mode is shown in Fig.A. 20-14.

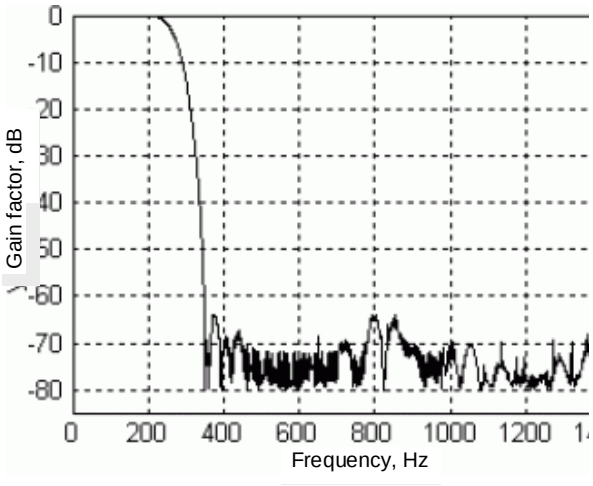


Fig. A. 20-7
LTR212(M). AFC with 258 Hz finite-impulse response- filter

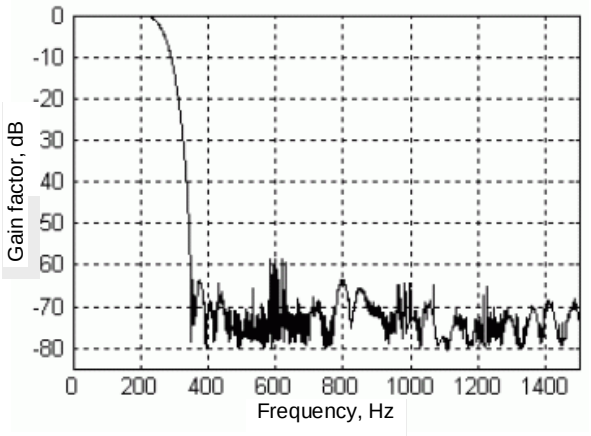


Fig. A. 20-8
LTR212(M). AFC with infinite-impulse response- filter and 258 Hz finite-impulse response -filter

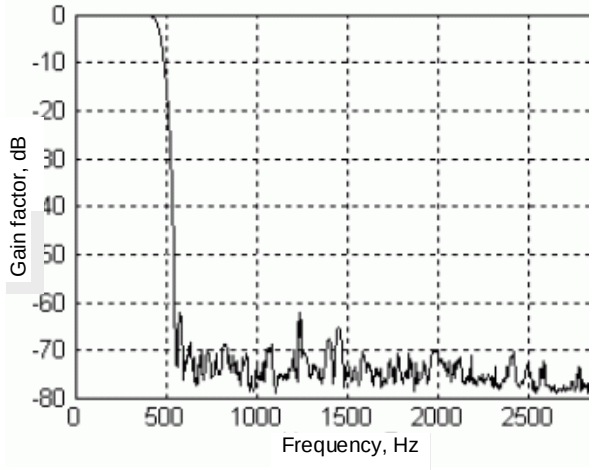


Fig. A. 20-9
LTR212(M). AFC with 456 Hz finite-impulse response- filter

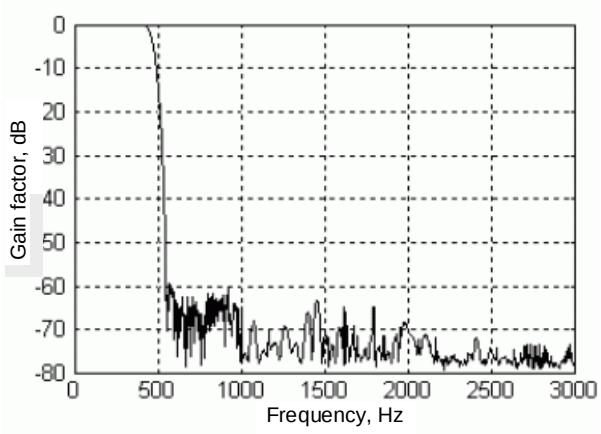


Fig. A. 20-10
LTR212(M). AFC with infinite-impulse response- filter and 456 Hz finite-impulse-response -filter

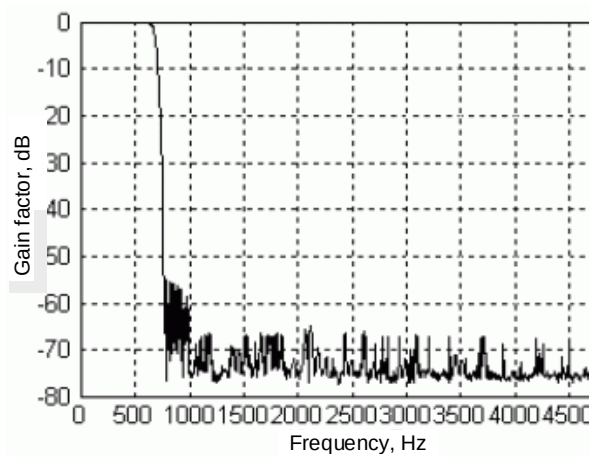


Fig. A. 20-11
LTR212. AFC with 675 Hz finite-impulse response- filter

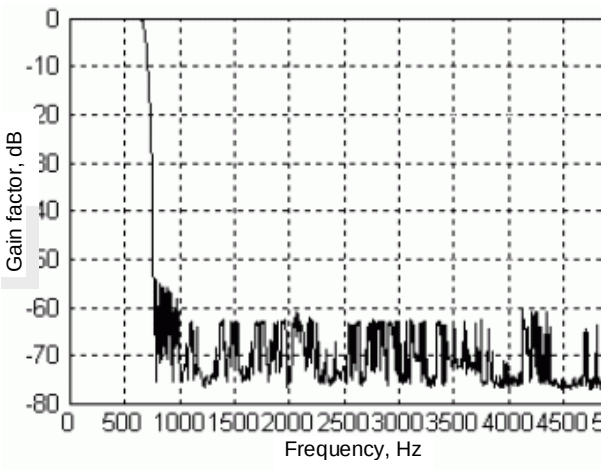


Fig. A. 20-12
LTR212. AFC with infinite-impulse response-filter and 675 Hz finite-impulse response -filter

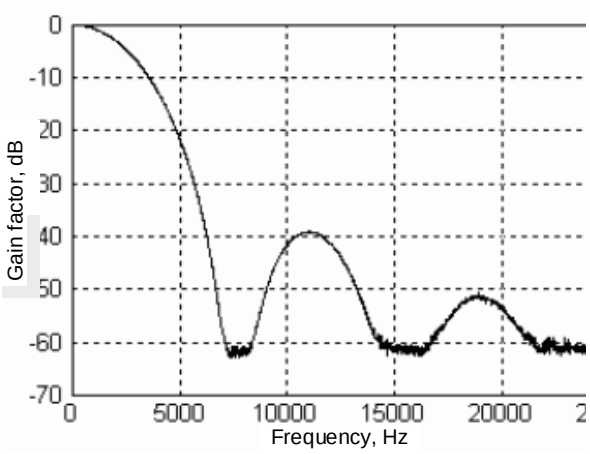


Fig. A. 20-13
LTR212. AFC at disabled filters

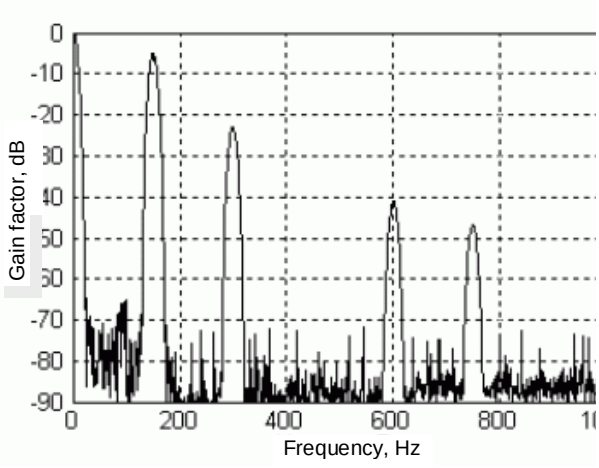


Fig. A. 20-14
LTR212. AFC in high-accuracy mode

A.3. LTR27 module

Specifications of LTR27 module as a carrier of measuring sub-modules are presented here. Characteristics of sub-modules H-27x are given inAppendix A.4, page 331

Parameter	Value
Number of installed sub-modules H-27x, max.	8
Number of measurment channels, max.	16
Galvanic isolation characteristics	See A.18, page 362
Power consumption in case of eight H-27x sub-modules installed, max.	5 W

A.4. Sub-modules H27x

Specifications of H27x sub-modules which can be installed in LTR27 carrier in any number (from 1 to 8) and in any combination are given here.

The below mentioned measurement errors correspond to data acquisition frequency of 5 Hz from each measurement channel H-27x.

Parameter	**Value**
Number of measuring channels in sub-modules:	
H-27U01, H-27U10, H-27U20, H-27T, H-27I5, H-27I10, H-27I20	2
H-27R100, H-27R250	1
Sub-module measurement range:	
H-27U01	±1 V
H-27U10	±10 V
H-27U20	0…+20 V
H-27T	-25…+75 mV
H-27I5	0…+5 mA
H-27I10	-10…+10 mA
H-27I20	0…+20 mA
H-27R100	0…100 Ohm
H-27R250	0…250 Ohm
The limits of permissible main relative error of **DC voltage measurement** for LTR 27 measuring module with sub-modules H-27U01, H-27U10, H-27U20, H-27T	±0.05%
The limits of permissible main relative error of **DC rate** measurement for LTR27 measuring module with sub-modules H-27I5, H-27I10, H-27I20	±0.05%
The limits of permissible main relative error of reduced error of measurements of DC resistance for LTR27 measuring module with sub-module H-27R100, H-27R250	±0.05%
Input DC resistance of sub-modules:	
H-27U01	Minimum 10 MOhm
H-27U10	1.02 ± 0.02 MOhm
H-27U20	1.02 ± 0.02 MOhm
H-27T	min. 10 MOhm
H-27I5	392 ± 4 Ohm
H-27I10	100 ± 1 Ohm
H-27I20	100 ± 1 Ohm

A.5. LTR43 module

Performance limits and additional characteristics of signal lines are presented in paragraph 8.4.1, page 333.

Parameter	Value
Configuration of digital input-output ports	4 ports (8 bit each) with each port set for input or for output
Number of bi-directional synchronization signals	2
Number of RS-485 ports	1 (alternative configuration of definite input-output signals, Table 8-1, page 149)
Levels of ports signals configured for input and synchronization inputs: – logic zero level, max. – Logic one level, min.	 0.4 V 2.4 V
Levels of ports signals configured for output and synchronization outputs: – Logic zero level: – Logic one level	 0.1..0.2 V (at unconnected output)[1] 4.8..5.2 V (at unconnected output)
Pull-up resistor on digital lines of ports	4.7 kOhm relative to +5 V[2]
Pull-up resistor on digital synchronization lines	absent (if an unconnected synchronization line is set for input, its state is not defined)
Maximum output current of input-output and synchronization lines configured for output	up to ±10 mA
Input current of logic zero of input-output signals	about 1 mA (due to pull-up resistors)
Input current of logic one of input-output signals	max. 0.3 mA
Input current of logic synchronization signal	max. 10 µA
Characteristics of external devices supply outputs: – output supply voltage – output load current, max. – maximum power output to load – maximum capacitive load	(alternative configuration of definite input-output signals, Table 8-1, page 149) ±12 V 120 mA if the maximum power output to load is not exceeded 2.8 W 1000 µF

[1] 0…0.1 V with 4.7 kOhm pull-up resistors relative to GND

[2] Optional configuration of LTR43 with 4.7 kOhm pull-up resistors on ports lines relative to GND is possible if it is specified at the time of ordering.

Parameter	Value
Time from the moment of sending an external or internal synchronization signal till the end of data output of a synchronization packet to the interface	1.5…1.8 µs (under condition that no data input is performed during the synchronization process), 1.5…4 µs (if the synchronization operation is combined with data input)
Time of transmission of internal synchronization signal to the output	20 ns
Requirements to dynamic parameters of input synchronization signal: – Maximum duration of signal transition – Minimum pulse duration	 unlimited min. 150 ns
Requirements to dynamic parameters of input signal of ports: – Maximum duration of signal transition	 500 ns
Operating transition of synchronization signal configured for input	edge (0-1)
Galvanic isolation characteristics: – galvanically isolated section of signals A485, B485, AGND, +12 V, -12 V relative to any of signals IO1,..., IO32, constant or mean-square AC value	maximum permissible voltage is 150 V
– other characteristics of galvanic isolation	See Appendix A.18, page 362

A.6. LTR41 module

Performance limits and additional characteristics of signal lines are presented in paragraph 9.4.1, page 335.

Parameter	Value
Number of asynchronous input channels	16
Number of bi-directional synchronization signals	2
Levels of synchronization signals:	compatible with TTL, 5 V-logic
Maximum output current of synchronization lines configured for output	up to ±10 mA
Input current of logic zero of input signals	max. 1 mA
Input current of logic one of input signals	min. 3 mA
Typical voltage/current value of input signals at the point of switching of logic levels[1]	2.2 V / 2.1 mA
Input current of logic synchronization signal	max. 10 µA
Characteristics of external devices supply outputs:	
–output power supply voltage	+4.9 V...+5.1 V stabilized
– output load current, max.	300 mA
– maximum capacitive load	1000 µF
Time from the moment of sending an external or internal synchronization signal till the end of data output of a synchronization packet to the interface	1.5…1.8 µs (under condition that no data input is performed during the synchronization process), 1.5…4 µs (if the synchronization operation is combined with data input)
Time of transmission of internal synchronization signal to the output	20 ns
Duration of pulse (positive or negative) of synchronization signals configured for input	min. 150 ns
Operating transition of synchronization signal configured for input	edge (0-1)
Galvanic isolation characteristics	See Appendix A.18, page 362

[1] typical current-voltage characteristic of input circuit is given in Fig. 9-3, page 120

A.7. LTR42 module

Preliminary data on LTR42 are given here. Complete data can be found in the next revisions of this document.

Performance limits and additional characteristics of signal lines are presented in paragraph 9.4.1, page 336.

Parameter	Value
Number of asynchronous output signals	16
Type of asynchronous output signals	optorelay output
Number of bi-directional synchronization signals	2
Type of synchronization signals	compatible with TTL, 5 V-logic
Maximum output current of synchronization lines configured for output	up to ±10 mA
Maximum current of closed optorelay output	max. ±70 mA
Maximum current of open optorelay output	max. ±1 µA at voltage ±250 V
Maximum permissible voltage of open optorelay output	max. ±250 V
Resistance of closed optorelay output	max. 30 Ohm
Typical time of optorelay output switching-on[1]	0.5 ms
Input current of logic synchronization signal	max. 10 µA
Characteristics of external devices supply outputs:	
output power supply voltage	+4.9 V…+5.1 V stabilized
output load current, maximum	300 mA
maximum capacitive load	1000 µF
Time from the moment of sending an external or internal synchronization signal till the end of data output of a synchronization packet to the interface	1.5…1.8 µs (under condition that no data input is performed during the synchronization process), 1.5…4 µs (if the synchronization operation is combined with data input)
Time of transmission of internal synchronization signal to the output	20 ns
Duration of pulse (positive or negative) of synchronization signals configured for input	min. 150 ns
Operating transition of synchronization signal configured for input	edge (0-1)
Galvanic isolation characteristics	See Appendix A.18, page 362

A.8. LTR51 module

Performance limits are presented in Table 10-6, page 176.

[1] duration of a transition switching-on process inside the optorelay at current in the executive circuit of up to 70 mA

Parameter	Value
Number of channels	2…16 independent with parallel polling, defined by the number of sub-modules (up to 8-two-channel sub-modules H-51x)
Type of inputs	single-phase
Form of measured signals	undefined compound form
Converter type	digital, calculating type with input diagram of selection by voltage level
Parameters of reference frequency generator	defined by the stability of the reference generator of LTR crate, see Appendix A.16, page 359
Signal input range	±10.0 V
Passband of input analog path at output resistance of signal source of max. 100 Ohm:	
– by level –1 dB	H-51FL: 0 - 5.9 kHz H-51FH: 0 - 29 kHz
– by level –3 dB	H-51FL: 0 - 36 kHz H-51FH: 0 - 178 kHz
Maximum possible measurement frequency	up to 250 kHz (equal to half sampling frequency)
Sampling frequency	programmed up to 500 kHz
Input resistance:	
– by DC	min. 100 KOhm
– by AC	complicated resistive-capacitive nature
Selection (calibration) diagram of input signal	bi-threshold with hysteresis
Ranges of calibration thresholds (set by means of jumpers installation)	–10.2…+10.1 V or –1.22…+1.21V (see Table 10-1, page 167)
Accuracy of calibration threshold setting	1.5% of the range
Calibration threshold setting increment	256 levels set in software within the range of calibration thresholds
Possibility of calibration diagram adjustment (appli-cation of calibration factors)	no
Temperature drift[1] of calibration threshold zero reduced to input	25 µV/ºC
Temperature dependence1 of calibration thresholds setting range	100 ppm/ºC
Galvanic isolation characteristics	See Appendix A.18, page 362

A.9. LTR22 module

Parameter	Value
Number of channels	4 with differential input
ADC conversion frequency:	
– maximum	78.125 kHz
– minimum	3.472 kHz
frequency spectrum	acording to the formula 11-1, page 180

[1] defined by characteristics of manufacturers' fitting elements and circuitry of the device. The parameter is not controlled intentionally

Parameter	Value
Sub-ranges of input signal measurements	±10 V, ±3 V, ±1 V, ±300 mV, ±100 mV, ±30 mV (set independently for each channel)
In-phase signal voltage	±10 V (does not depend on the sub-range)
Signal operating range relative to AGND – at input X – at input Y	 ±12 V ±12 V
ADC bit depth	16 bits
The limits of permissible main relative error of voltage measurement of mean-square value of AC (without AFC normalizing) at ADC frequency of 78.125 kHz at a signal frequency of: – 0.02...5 kHz – 5...15 kHz – 15...25 kHz	 ±0.15% within the sub-ranges ±10 V, ±3 V, ±1 V; ±0.3% within the sub-ranges ±300 mV, ±100 mV, ±30 mV ±0.5% within the sub-ranges ±10 V, ±3 V, ±1 V; ±1,0% within the sub-ranges ±300 mV, ±100 mV, ±30 mV ±2.0% within the sub-ranges ±10 V, ±3 V, ±1 V; ±4.0% within the sub-ranges ±300 mV, ±100 mV, ±30 mV
Common-mode rejection factor [1] of 50 Hz in the differential mode, min.	80 dB
Common interference suppression factor [2] at 50 Hz in the differential mode, min.	90 dB
Input resistance of the differential input (for any line X1…X4, Y1…Y4 relative to AGND circuit) when the module is switched-on	min. 10 MOhm in the operating mode in the range of input voltage ±10 V
Inter-channel passage of 1 kHz sinusoidal signal in all sub-ranges	max. -80 dB
Special modes: – measurement of own voltage of zero shift – AC mode "with constant component compensation" or normal DC+AC mode	programmed simultaneously for all channels programmed simultaneously for all channels
AFC parameters: – Lower AFC limit in the DC+AC mode – Lower AFC limit in the AC mode – Upper AFC limit	 Direct current (0 Hz) 0.7 Hz by level –3 dB 0.48 of the set conversion frequency by level –3 dB

[1] for interference applied to the input relative to AGND circuit at unbalance of resistances of external input circuits equal to 1 kOhm

[2] for interference applied to the input relative to LTR crate grounding terminal at unbalance of resistances of external input circuits equal to 1 kOhm

Parameter	Value
Typical values of noise level reduced to the input at shorted-out ADC inputs at a conversion frequency of 78.125 kHz – In 30 mV sub-range – In 100 mV sub-range – In 300 mV sub-range – In 1 V sub-range – In 3 V sub-range – In 10 V sub-range	 0.009 mV (eff.) 0.01 mV (eff.) 0.013 mV (eff.) 0.03 mV (eff.) 0.1 mV (eff.) 0.3 mV (eff.)
Typical values of noise level reduced to the input upon shorted-out ADC inputs at a conversion frequency of 3.4722 kHz – In 30 mV sub-range – In 100 mV sub-range – In 300 mV sub-range – In 1 V sub-range – In 3 V sub-range – In 10 V sub-range	 0.003 mV (eff.) 0.004 mV (eff.) 0.012 mV (eff.) 0.03 mV (eff.) 0.1 mV (eff.) 0.3 mV (eff.)
Galvanic isolation characteristics	See Appendix A.18, page 362
Characteristics of synchronization input SYN_IN: – logic zero level, max. – logic one level, min. – pull-up resistor	 0.5 V 2.4 V 20 kOhm relative to GND unlimited
Characteristics of synchronization output SYN_OUT: – Logic zero level: – Logic one level	 0…0.1 V (without load) 0.4 V (at 4 mA output current relative to 3.3 V) 3.2…3.4 V (without load) 2.8…3.0 V (upon 4 mA output current relative to GND)
Characteristics of output of external device power supply source: – Voltage – Output current – Output resistance, typical value	 Bipolar stabilized ±15 V 50 mA 22 Ohm at the output of each pole

A.10. LTR24 module

Parameter, characteristic	Value, description
Number of conversion channels	4
ADC conversion frequency:	
– maximum	117.188 Hz
– minimum	610.352 Hz
ADC bit depth	20 / 24 bits (programmable)
Frequency spectrum	set by the formula (12-1) , page 195

Parameter, characteristic	Value, description
Measurement range: – voltage in modifications LTR24, LTR24-1, LTR24-2 in the "Dif. input" mode	 "±10 V", "±2 V" (peaks)
– voltage in modification LTR24-2 in the "ICP input" mode	"~5 V", "~1 V" (mean-square value of variable component of signal if the signal variable component amplitude "±10 V", "±2 V" is not exceeded)
– voltage in modification LTR24-2 in the "ICP-test" mode	0…+25 V
– resistance[1] in modification LTR24-2 in the "DC+AC resistance" mode: • at current 10 mA and voltage range "±10 V" • at current 2.86 mA and voltage range "±10 V" • at current 10 mA and voltage range "±2 V" • at current 2.86 mA and voltage range "±2 V"	 0…1,000 Ohm 0…3,496 Ohm 0…200 Ohm 0…699 Ohm
– variable component of resistance in modification LTR24-2 in the "DC+AC resistance" mode • at current 10 mA and voltage range "±10 V" • at current 2.86 mA and voltage range "±10 V" • at current 10 mA and voltage range "±2 V" • at current 2.86 mA and voltage range "±2 V"	 ±R/2 at the sensor resistance R=0…1000 Ohm ±R/2 at the sensor resistance R=0…1000 Ohm ±R/2 at the sensor resistance 0…200 Ohm ±R/2 at the sensor resistance 0…699 Ohm
Voltage of differential input in-phase signal	±10 V (does not depend on the sub-range)
Signal operating range relative to AGND – at input X – at input Y – at ICP inputs	 ±12 V ±12 V 0 to 22 V.
Operating range of signal constant component compensation in the "AC" mode: – in "±10 V" sub-range (with single-phase signal source – signal sent to X, input Y grounded on AGND) – in "±2 V" sub-range (with single-phase signal source – signal sent to X, input Y grounded on AGND) – in "±10 V" and "±2 V" sub-ranges (for signal from ICP-sensor sent to ICP input)	 ±1.7 V ±10 V (if the variable component is within the range of ±1 V) ±2.5 V ±4.5 V (if the variable component is within the range of ±0.25 V) 0 to 22 V

[1] Measurement of resistance and estimation of errors is performed indirectly based on measured voltage values of known calibrated value of current for each channel and Ohm's law.

<table>
<tr><th>Parameter, characteristic</th><th colspan="3">Value, description</th></tr>
<tr><td>DC value in the current source circuit at a voltage from 0 to 22 V within operating temperature range, in the mode
“10 mA”
“2.86 mA”</td><td colspan="3">

“10 mA ± 2%
“2.86 mA ± 2%</td></tr>
<tr><td>Instability of the current source relative to the calibrated current value:
– under normal conditions
– within full temperature range</td><td colspan="3">
±0.05% of the calibrated value
±0.15% of the calibrated value</td></tr>
<tr><td>Internal resistance of ICP circuits at a voltage from 0 to 22 V in the operating mode:
– at direct current
– at alternating current in the passband frequency</td><td colspan="3">
Min. 2.7 MOhm
Min. 25 kOhm (impedance module)</td></tr>
<tr><td>ADC bit depth</td><td colspan="3">20/24 bits depending on the settings</td></tr>
<tr><td rowspan="15">Possible combinations of ADC conversion frequency, ADC output data format and number of channels.

(specific case of possible number of channels for LTR-U-1-4 crate is given in brackets)</td><td rowspan="4">ADC data acquisition frequency, kHz</td><td colspan="2">Supported combination of ADC data format and number of channels</td></tr>
<tr><td colspan="2">ADC data format</td></tr>
<tr><td>20 bits</td><td>24 bits</td></tr>
<tr><td colspan="2">Number of channels</td></tr>
<tr><td>117.188</td><td>1÷4 (1)</td><td>1÷2 (0)</td></tr>
<tr><td>78.125</td><td>1÷4 (1÷2)</td><td>1÷3 (1)</td></tr>
<tr><td>58.594</td><td>1÷4 (1÷3)</td><td>1÷4 (1)</td></tr>
<tr><td>39.063</td><td>1÷4</td><td>1÷4
(1÷2)</td></tr>
<tr><td>29.297</td><td>1÷4</td><td>1÷4
(1÷3)</td></tr>
<tr><td>19.531</td><td colspan="2">1÷4</td></tr>
<tr><td>14.648</td><td colspan="2">1÷4</td></tr>
<tr><td>9.76563</td><td colspan="2">1÷4</td></tr>
<tr><td>7.32422</td><td colspan="2">1÷4</td></tr>
<tr><td>4.88281</td><td colspan="2">1÷4</td></tr>
<tr><td>3.66211</td><td colspan="2">1÷4</td></tr>
<tr><td>2.44141</td><td colspan="2">1÷4</td></tr>
<tr><td>1.83105</td><td colspan="2">1÷4</td></tr>
<tr><td>1.22070</td><td colspan="2">1÷4</td></tr>
<tr><td>0.915527</td><td colspan="2">1÷4</td></tr>
</table>

Parameter, characteristic			Value, description
			0.610352 | 1÷4
The limits of permissible main relative error of DC voltage measurements in the "Dif. input" mode, per cent			$\pm\left[0{,}05+0{,}01\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$ X_K is the end value of the set measurement sub-range (X_K = 10 V or 2 V); X is LTR24 reading, V.
The limits of permissible main reduced error of DC voltage measurements – "ICP test"			±2 % (typical[1] value)
The limits of permissible main relative error of mean-square value of AC voltage measurements in the "Dif. input" mode, under conditions:			
ADC conversion frequency	**Signal frequency, "DC+AC"**	**Signal frequency, "AC"**	%
610.352; 915.527; 1220.7; 1831.05; 2441.41; 3662.11; 4882.81; 7324.22; 9765.63; 14648	From 1 Hz to $0.43F_{lim}$	From 25 Hz to $0.43F_{lim}$	$\pm\left[0{,}05+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}1}}{1{,}414\times X}\right\rvert-1\right)\right]$
19531; 29297; 39063	From 1 Hz to $0.25F_{lim}$	From 25 Hz to $0.25F_{lim}$	$\pm\left[0{,}1+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}1}}{1{,}414\times X}\right\rvert-1\right)\right]$
	More than $0.25F_{lim}$ to $0.43F_{lim}$	More than $0.25F_{lim}$ to $0.43F_{lim}$	$\pm\left[0{,}2+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}1}}{1{,}414\times X}\right\rvert-1\right)\right]$
58594; 78125; 117188	From 1 Hz to $0.25F_{lim}$	From 25 Hz to $0.25F_{lim}$	
	More than $0.25F_{lim}$ to $0.43F_{lim}$	More than $0.25F_{lim}$ to $0.43F_{lim}$	$\pm\left[2+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}1}}{1{,}414\times X}\right\rvert-1\right)\right]$
			X_{K1} is the end value of the set measurement sub-range (X_K = 10 V or 2 V); X is reading of LTR24, V.

[1] For "ICP test" mode, measurement accuracy is an evaluation value determined by accuracies of applied elements (not controlled intentionally during production)

The limits of permissible main relative error of mean-square value of AC voltage measurements in per cent in the "ICP input" mode, under conditions:		
ADC conversion frequency, F_{lim}, Hz	**Input signal frequency in the "ICP sensor" mode**	**%**
610.352; 915.527; 1220.7; 1831.05; 2441.41; 3662.11; 4882.81; 7324.22; 9765.63; 14648	From 100 Hz to 0.43F_{lim}	$\pm\left[0{,}1+0{,}02\times\left(\left\lvert\frac{X_{\hat{E}2}}{1{,}414\times X}\right\rvert-1\right)\right]$
19531; 29297; 39063	From 100 Hz to 0.25F_{lim}	$\pm\left[0{,}2+0{,}02\times\left(\left\lvert\frac{X_{\hat{E}2}}{1{,}414\times X}\right\rvert-1\right)\right]$
	More than 0.25F_{lim} to 0.43F_{lim}	$\pm\left[0{,}4+0{,}02\times\left(\left\lvert\frac{X_{\hat{E}2}}{1{,}414\times X}\right\rvert-1\right)\right]$
58594; 78125; 117188	From 100 Hz to 0.25F_{lim}	
	More than 0.25F_{lim} to 0.43F_{lim}	$\pm\left[4+0{,}02\times\left(\left\lvert\frac{X_{\hat{E}2}}{1{,}414\times X}\right\rvert-1\right)\right]$
		X_{K2} is the end value of the set measurement sub-range, X_{K2} = 5 V or 1 V; X is reading of LTR24-2, V
Common-mode rejection factor[1] 50 Hz in the differential mode, min.		77 dB
Common interference suppression factor[2] at 50 Hz in the differential mode, min.		75 dB
Input resistance of the differential input (for any line X1…X4, Y1…Y4 relative to AGND circuit) when the module is switched-on		Minimum 10 MOhm
Input current in lines X1…X4, Y1…Y4 at the voltage of ±10 V:		
– under normal conditions		±0.2 nA
– within operating temperature range		±3 nA
Maximum permissible voltage relative to AGND circuit:		
– at inputs X1…X4, Y1…Y4		±20 V
– at inputs ICP		-1…+27 V at a current of max. ±30 mA (in case of wrong connection of an external source of voltage-current)
AFC parameters:		
"Diff.-input":		
– Lower AFC limit in the "DC+AC" mode		Direct current (0 Hz)
– Lower AFC limit in the "AC" mode		(0.48 ± 0.6) Hz, by level –3 dB

[1] for interference applied to the input relative to AGND circuit at unbalance of resistances of external input circuits equal to 1 kOhm

[2] for interference applied to the input relative to LTR crate grounding terminal at unbalance of resistances of external input circuits equal to 1 kOhm

– Upper AFC limit	0.49 of the set conversion frequency by level –3 dB
"ICP-input":	
– Lower AFC limit	1.3 Hz, by level –3 dB (typical value)
– Upper AFC limit	0.49 of the set conversion frequency by level –3 dB

Residual zero shift[1] of the converter in the "AC" mode: – in ±10 V sub-range – in ±2 V sub-range	 5 mV 1 mV
Signal/noise ratio, typical value – *"Diff.-input":* – *"ICP-input":*	 102 dB
Signal/(noise+harmonics) ratio for sinusoidal signal (**SINAD**), typical value – *"Diff.-input":* – *"ICP-input":*	 97 dB 92 dB
Non-linear distortion factor (**THD**), typical value – *"Diff.-input":* – *"ICP-input":*	 100 dB 94 dB
Dynamic range free of pulse tails (**SFDR**), typical value – *"Diff.-input":* – *"ICP-input":*	 101 dB 95 dB
Inter-channel passage at 5 kHz frequency – *"Diff.-input":* – *"ICP-input":*	 Less than -90 dB Less than -90 dB
Own noise, typical value: *"Diff-input"* at shorted-out input : – at conversion frequency of 117.188 kHz • in "2 V" sub-range • in "10 V" sub-range – upon conversion frequency of 39.063 kHz • in "2 V" sub-range • in "10 V" sub-range – at conversion frequency of 9.766 kHz • in "2 V" sub-range • in "10 V" sub-range – *"ICP-input"* at signal source resistance of 100 Ohm: – at conversion frequency of 117.188 kHz • in "2 V" sub-range	 9 µV 42 µV 6 µV 26 µV 4.5 µV 23 µV 16 µV

[1] Zero shift in the AC mode is not calibrated intentionally.

• in "10 V" sub-range	45 µV
– at conversion frequency of 39.063 kHz	
• in "2 V" sub-range	12 µV
• in "10 V" sub-range	35 µV
– at conversion frequency of 9.766 kHz	
• in "2 V" sub-range	8 µV
• in "10 V" sub-range	23 µV
– *In case of indirect measurement* of 100 Ohm resistance in "2 V" sub-range and at the current of "2.86 mA ± 2%	
– at conversion frequency of 117.188 kHz	
• at the current of 2.86 mA ± 2%	10 µV
• at the current of 10 mA ± 2%	12 µV
– at conversion frequency of 39.063 kHz	
• at the current of 2.86 mA ± 2%	7 µV
• at the current of 10 mA ± 2%	9 µV
– at conversion frequency of 9.766 kHz	
• at the current of 2.86 mA ± 2%	6 µV
• at the current of 10 mA ± 2%	8 µV
Program converter overflow signs triggering threshold	96÷99% of half converter's range for signal of any sign
Galvanic isolation characteristics	See Appendix A.18, page 362
Characteristics of output of external device power supply source:	
– Voltage	+15 V, -15 V.
– Rated output current	30 mA 10 mA (for LTR24-2 in case of engaged ICP-inputs)
– Output resistance, typical value	22 Ohm
Power consumption from motherboard (in case of non-loaded outputs +15 V, -15 V):	
LTR24, LTR24-1	3.0 W
LTR24-2, ICP-inputs are not connected	3.5 W
LTR24-2, ICP-inputs are connected, current is 3 mA	3.5 W
LTR24-2, ICP-inputs are connected, current is 10 mA	4.6 W

A.11. LTR25 module (preliminary data)

Parameter, characteristic	Value, description
Number of channels	8 inputs for connection of ICP-sensors
ADC bit depth	20 / 24 bits (programmable)
Operating signal range relative to AGND at ICP inputs	0 to 22 V.
Voltage measurement range	"~5 V" (mean-square value of the variable component of signal, if the signal variable component amplitude does not exceed "±10 V")

<table>
<tr><th>Parameter, characteristic</th><th colspan="3">Value, description</th></tr>
<tr><td>Signal/(noise+harmonics) ratio for sinusoidal signal (SINAD), typical value</td><td colspan="3">92 dB</td></tr>
<tr><td>DC value in the current source circuit at a voltage from 0 to 22 V within operating temperature range, in the mode
“10 mA”
“2.86 mA”</td><td colspan="3">“10 mA ± 2%
“2.86 mA ± 2%</td></tr>
<tr><td>Current source stability relative to the calibrated current value:
– under normal conditions
– within full temperature range</td><td colspan="3">±0.05% of the calibrated value
±0.15% of the calibrated value (characteristic to be determined)</td></tr>
<tr><td>Internal resistance of ICP circuits at a voltage from 0 to 22 V in the operating mode:
– at direct current
– at alternating current in the passband frequency</td><td colspan="3">Min. 5 MOhm (to be determined)
Min. 30 kOhm (impedance module)</td></tr>
<tr><td>“ICP-input”:
– Lower AFC limit
– Upper AFC limit</td><td colspan="3">1.3 Hz, by level –3 dB (typical value)
About half samples spacing frequency (numerical characteristics to be determined)</td></tr>
<tr><td rowspan="9">Possible combinations of ADC conversion frequency, ADC output data format and number of channels.

(specific case of possible number of channels for LTR-U-1-4 crate is given in brackets)</td><td rowspan="3">ADC data acquisition frequency, kHz</td><td colspan="2">Supported combination of ADC data format and number of channels</td></tr>
<tr><td colspan="2">ADC data format</td></tr>
<tr><td>20 bits</td><td>24 bits</td></tr>
<tr><td></td><td colspan="2">Number of channels</td></tr>
<tr><td>78.125</td><td>1÷6 (1÷2)</td><td>1÷3 (1)</td></tr>
<tr><td>39.063</td><td>1÷8 (1÷5)</td><td>1÷6 (1÷2)</td></tr>
<tr><td>19.531</td><td>1÷8</td><td>1÷8 (1÷5)</td></tr>
<tr><td>9.76563</td><td colspan="2">1÷8</td></tr>
<tr><td>4.88281</td><td colspan="2">1÷8</td></tr>
<tr><td>2.44141</td><td colspan="2">1÷8</td></tr>
<tr><td>1.22070</td><td colspan="2">1÷8</td></tr>
<tr><td>0.610352</td><td colspan="2">1÷8</td></tr>
</table>

Parameter, characteristic		Value, description
The limits of permissible main reduced (to final value of sub-range) error of mean-square value of AC voltage measurement, under conditions:	**Signal frequency range**	
	From 25 Hz to 0.43F_{lim}	±0.1% (characteristic to be determined)

78.125	1÷6 (1÷2)	1÷3 (1)
39.066	1÷8 (1÷5)	1÷6 (1÷2)
19.531	1÷8	1÷8 (1÷5)

A.12. LTR34 module

! Performance limits and additional characteristics of signal lines are presented in paragraph 14.3.1, page 348.

Parameter	Value
Number of DAC physical channels in the module – LTR34-4 – LTR34-8	 4 8
Possible number of channels of parallel output to DAC in accordance with the mode set in software – LTR34-4 – LTR34-8	 1, 2, 4 1, 2, 4, 8
DAC data output modes:	– stream – active oscillator
Signal range at outputs: – 1:1 – 1:10	 ±10 V ±1 V
Maximum DAC frequency in the stream output mode: – in 1-channel mode – in 2-channel mode – in 4-channel mode – in 8-channel mode	 400.0 kHz 200.0 kHz 100.0 kHz 50.0 kHz
Maximum DAC frequency in the active oscillator mode: – in 1-channel mode – in 2-channel mode – in 4-channel mode – in 8-channel mode	 500.0 kHz 250.0 kHz 125.0 kHz 62.5 kHz
Frequency spectrum of samples synchronous output	Fs = F/N, where F is programmable *common data output frequency* (61 frequency values in total) from the range of 500 kHz, 400 kHz, 333 kHz, …, 31.7 kHz, 31.25 kHz, N is number of used channels N = 1 ,2, 4 or 8. The set frequency Fs is the same for all channels. Frequency spectrum is defined according to the formula (14-1)

Parameter	Value
Volume of the circular buffer in the active oscillator mode	from 2 to 2 million samples (within the specified limits it is defined by actual volume of data array pre-loaded to DAC)
Output DC resistance – outputs 1:1 – outputs 1:10	 (50±0.5%) Ohm (389±1%) Ohm
Maximum output current – outputs 1:1 – outputs 1:10	 minimum 25 mA 2.5 mA (limited by output resistance)
Long-term resistance of outputs to short circuit	yes
The limits of permissible main reduced error of DC voltage reproduction	±0.1%
The limits of permissible main reduced error of sinusoidal AC voltage reproduction for N-channel mode (N = {1, 2, 4, 8}), for output voltage frequency: – 400 Hz – Except for 400 Hz from 10 Hz to $\frac{5000}{N}$ Hz – More than $\frac{5000}{N}$ Hz to $\frac{12000}{N}$ Hz – More than $\frac{12000}{N}$ Hz to $\frac{16000}{N}$ Hz	 ±0.1% ±0.15% ±0.5% ±1%
Characteristics of synchronization input – input type – input current, max.	 a logic TTL input compatible with TTL/CMOS-output with power supply of 5V and derived output current of logic one not less than 8mA 8 mA at input voltage of 5 V
Galvanic isolation characteristics – synchronization input voltage relative to other contacts of user connector – other characteristics	 max. 200 V acceptable See Appendix A.18, page 362

A.13. LTR35 module (preliminary data)

Parameter, characteristic	Value, description
Number of channels of DAC conversion in the module / output digital lines: – LTR35-1-8 – LTR35-1-4: – LTR35-2-8: – LTR35-3-0: *Number of digital synchronization inputs*	 8 / 8 4 / 8 8 / 8 0 / 16 2
DAC bit depth	24
DAC data output modes:	– stream – asynchronous; – cyclic active oscillator of random cycle signal; – “arithmetic” sinusoidal generator.
Signal range at LTR35-1 outputs: – 1:1 – 1:5	 ±10 V ±2 V
Signal range at LTR35-2 outputs: – 1:1 – 1:10	 −2…+20 V −0.2…+2 V
Frequency band of output signal reproduction	From 0 to 96 kHz
Maximum DAC conversion frequency	192 kHz
The limits of permissible main reduced error of DC voltage reproduction	Characteristic to be determined
The limits of permissible main reduced error of sinusoidal AC voltage reproduction	Characteristic to be determined
Volume of the circular buffer in the active oscillator mode Volume of the FIFO buffer in the stream mode	4 M (2^{22}) of data samples 8 M (2^{23}) of data samples

Output DC resistance – outputs 1:1 – outputs 1:5	 (50±1%) Ohm (50±1%) Ohm
Maximum output current – outputs 1:1 – outputs 1:5	 Characteristic to be determined Characteristic to be determined
Digital outputs characteristics: – "Logic one" level – "Logic zero" level – Output resistance – Operating output current – Leakage current of outputs in Z-state – Leakage current of outputs in case of de-energized LTR35 – Maximum permissible range of output voltage in Z-state	 +3.3V (at a load current of 100 µA) 0…+0.2 V (at a load current of 100 µA) 100 Ohm ±8 mA ± 5 µA ± 10 µA −0.5…+7 V
Digital inputs characteristics: – "Logic zero" level – "Logic one" level – Typical value of hysteresis voltage	 −3.0…+0.55 V +1.3 V…+7 V 1.0 V
Galvanic isolation characteristics	See Appendix A.18, page 362

A.14. LTR114 module

Performance limits and additional characteristics of signal lines are presented in paragraph16.3.9, page 265.

Parameter, characteristic	Value, description
ADC parameters:	
ADC bit depth	24 bits
Maximum ADC conversion frequency	4 kHz
Number of channels for ADC data acquisition (except for the dedicated channel for temperature measurement): - in the voltage measurement mode - in the resistance measurement mode - in the combined measurement mode, the ratio of maximum possible number of channels for voltage/measurement can be equal to	 up to 16 up to 8 14/1, 12/2, 10/3, 8/4, 6/5, 4/6, 2/7
Measurement sub-ranges - in the voltage measurement mode - in the resistance measurement mode	 ±10 V, ±2 V, ±0.4 V 0÷4000 Ohm (at current of 0.1 mA), 0÷1200 Ohm (at current of 0.33 mA), 0÷400 Ohm (at current of 1 mA) [1]

[1] Lower values of resistance measurement sub-ranges will be specified in the next revisions of this document

<table>
<tr><td rowspan="5">The limits of permissible main relative error of DC voltage measurements in LTR114 (per cent) in the "Continuous calibration" mode, at a conversion frequency of</td><td colspan="3">Within the measurement sub-range</td></tr>
<tr><td>0.4 V</td><td>2 V</td><td>10 V</td></tr>
<tr><td>– 5 Hz</td><td>$\pm\left[0{,}01+0{,}005\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td><td colspan="2">$\pm\left[0{,}01+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td></tr>
<tr><td>– Over 5 to 1000 Hz</td><td>$\pm\left[0{,}015+0{,}005\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td><td colspan="2">$\pm\left[0{,}015+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td></tr>
<tr><td>– Over 1000 to 4000 Hz</td><td>$\pm\left[0{,}05+0{,}005\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td><td>$\pm\left[0{,}05+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td><td>$\pm\left[0{,}03+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td></tr>
<tr><td colspan="4">Symbols: X_K is the end value of the set measurement sub-range, V; X is reading of LTR114, V</td></tr>
<tr><td rowspan="5">The limits of permissible main relative error of DC voltage measurements (per cent) in the "Initial calibration" mode, at a conversion frequency of:</td><td colspan="3">Within the measurement sub-range</td></tr>
<tr><td>0.4 V</td><td>2 V</td><td>10 V</td></tr>
<tr><td>– 5 Hz</td><td colspan="3">$\pm\left[0{,}015+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td></tr>
<tr><td>– Over 5 to 1000 Hz</td><td colspan="3">$\pm\left[0{,}02+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td></tr>
<tr><td>– Over 1000 to 4000 Hz</td><td>$\pm\left[0{,}05+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td><td colspan="2">$\pm\left[0{,}03+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td></tr>
<tr><td colspan="4">Symbols: X_K is the end value of the set measurement sub-range, V; X is reading of LTR114, V</td></tr>
<tr><td rowspan="3">The limits of permissible main relative error AC voltage measurements (per cent), at a conversion frequency of:</td><td colspan="2">In the "Continuous auto-calibration" mode</td><td>In the "Initial auto-calibration" mode</td></tr>
<tr><td>– 5 Hz</td><td colspan="2">$\pm\left[0{,}025+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td><td>$\pm\left[0{,}025+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td></tr>
<tr><td>– Over 5 to 2000 Hz</td><td colspan="2">$\pm\left[0{,}03+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td><td>$\pm\left[0{,}05+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td></tr>
<tr><td>– 4000 Hz in the sub-ranges of 400; 1200 Ohm</td><td colspan="2">$\pm\left[0{,}03+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td><td rowspan="2">$\pm\left[0{,}1+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td></tr>
<tr><td>– 4000 Hz in the sub-range of 4000 Ohm</td><td colspan="2">$\pm\left[0{,}07+0{,}006\times\left(\left\lvert\frac{X_{\hat{E}}}{X}\right\rvert-1\right)\right]$</td></tr>
</table>

	X_K is the end value of the set measurement sub-range, Ohm; X is reading of LTR114, Ohm
ADC input - in the voltage measurement mode - in the resistance measurement mode	 differential 4-wire
Size of data acquisition frame	from 0 to 128
Amount of inter-frame delay	from 0 to 65535
Mean power dissipation on resistor in the resistance measurement mode, W (paragraph 16.2.2.8)	$P = I^2R\frac{n}{m+d}$, where I is flowing current (A), R is resistance of thermo-resistor (Ohm), n is number of polls of this channel within the frame (0÷m), m is frame size from 1 to 128, d is the size of inter-frame delay from 0 to 65535 ADC conversion periods
Modes:	
Auto-calibration modes	- with initial auto-calibration - with continuous auto-calibration
Resistance measurement modes	- with direct current - with alternating current
Input circuits integrity control mode	check for breakage/short circuit of input circuits, paragraph 16.4, page 268
Redundancy (duplication) mode	See paragraph 16.3.4 on page 262, paragraph 16.3.7 on page 264
ADC synchronization parameters:	
ADC conversion synchronization types:	- “internal” - “master” - “slave”
Number of synchronization lines	1 (bi-directional, combined with channel for temperature detector connection)
Type of synchronization signals - output (in the “master” mode) - input (in the “slave” mode)	 Compatible with TTL/CMOS (5V-logic). Compatible with TTL/CMOS (5V-logic).

Operating transition of synchronization signal - output (in the “master” mode) - input (in the “slave” mode)	 on edge (transition from "0" to "1") on edge (transition from "0" to "1")
Duration of synchronization pulse - output (in the “master” mode) - input (in the “slave” mode)	$0{,}273/F_{ADC}$, where F_{ADC} is ADC conversion frequency min. 1 µs
Maximum duration of input synchronization signal transition (in the "slave" mode)	unlimited
Output operating current of logic "0" and "1" of output synchronization signal (in the "master" mode)	±20 mA
Galvanic isolation characteristics: - voltage on DIO synchronization lines relative to other contacts of user connector - other characteristics	 max. 200 V acceptable See Appendix A.18, page 362

A.15. LTR210 module

Parameter, characteristic	Value, description
Number of channels: – ADC – Digital input/synchronization	 2 parallel independent channels 1
ADC frequency spectrum: – without data reduction – with data reduction	 From 1 to 10 MHz and is set by the ratio 10/n [MHz], where n=1,2,…,10. From 39 kHz to 10 MHz and is set by the ratio 10/(n*m) [MHz], where n=1,2,…,10; m=1,2,…256 – reduction factor
ADC bit depth	14 bits
Programmable (independently for both channels) ADC sub-ranges.	”±10 V”, “±5 V”, “±2 V”, “±1 V”, “±0.5 V”
ADC input modes (programmable independently for both channels)	– “0” (measurement of own zero) –“AC” (DC component cut-off mode) – “DC+AC” (normal mode without DC component cut-off)
Operating range of input signal:	
– in the “AC” mode	±13.5 V (peak-peak) for DC voltage (for AC voltage, is defined by the limits of the selected measurement sub-range)
– in the “DC+AC” mode	Defined by the limits of the selected measurement sub-range
Full passband: – in the “AC” mode – in the “DC+AC” mode	 0.8 Hz… 10 MHz 0 Hz…10 MHz
Main reduced to sub-range relative error of DC voltage measurement	±0.2% (for all sub-ranges).
Relative error of analog synchronization threshold setting (by DC voltage)	±0.2%
Maximum permissible voltage range at ADC input	±20 V
ADC input resistance	1.00 MOhm ±1% (compatibility with a standard oscillographic probe is ensured)

Parameter, characteristic	Value, description
Signal/noise ratio of ADC input for sinusoidal signal of 1 kHz (typical value): – In sub-ranges ”±10 V”, “±5 V” – In sub-ranges “±2 V”, “±1 V”, “±0.5 V”	 74 dB 77 dB
Inter-channel passage in ADC channels	Not found (within the monitoring range of 120 dB)
Settings of synchronization system events	– Analog (for event of passing a programmable voltage threshold (synchronization level)). – Digital (on edge/on drop of digital signal at the synchronization input) – Program single – Periodic, with a programmable period of up to 1 hour with period setting increment of 1 μs. – From other LTR210 module (for any event) or from an external source of TTL-signal through the synchronization connector.
Configurations of external synchronization line (possibility of multifunctional digital input/input-output of synchronization for different LTR210 connection diagrams).	– External synchronization of one LTR210 module from one TTL-signal source – External synchronization of several LTR210 modules from one TTL-signal source – One master LTR210 module synchronizes one or more slave LTR210 modules (50 Ohm plugs at both ends of the coaxial line connecting the modules into the circuit are required)
Possibilities of multi-functional digital synchronization input-output SYNC as a standard digital input	The existing logic state of input is written in the buffer memory together with ADC samples in any mode. Thus, the third data collection channel is implemented which operates like a standard digital input.
Input characteristics of multifunctional digital synchronization input-output SYNC:	
− Switching threshold	+1.5…+2.4 V
− Hysteresis voltage value	0.4…1.3 V
− Input resistance	50 kOhm (within the voltage range from 0 to 4.3 V)
− Maximum permissible input voltage: • Long-term • Short-term for 1 ms	 -6.0 …+11 V -12 V …+15 V
Output characteristics of multifunctional digital synchronization input-output SYNC:	
− Rated load resistance	25 Ohm (50 Ohm loads at both ends of the synchronization line).
− Active pulse output current.	150 mA (pulse duration is 1 μs)
− Output current when there is no synchronization pulse	less than 2 μA

Parameter, characteristic	Value, description
− Output voltage of “no-load run” − Output peak voltage on the rated load	(up to 11 V peak voltage of pulse 1 μs). +3.0…+4.5 V (50 Ohm at both ends of synchronization line).
Offset of synchronization time of different LTR210 modules in case of intermodule synchronization.	Maximum ±(1/Fs), where Fs is a period of ADC conversion.
Volume of buffer module memory	16 million ADC data samples
Modes of writing in buffer memory	– Writing of ADC channel 1 – Writing of ADC channel 2 – Writing of ADC channel 1 and 2 (for 2-channel mode) In any case, one of the channels can be used for synchronization event generation. In any case, the state of digital synchronization input is recorded.
Data acquisition modes:	– Start-stop for a synchronization event (oscillographic mode) with ADC conversion frequency of up to 10 MHz. – Continuous (with ADC conversion frequency, see below)
Maximum ADC conversion frequency in the continuous data acquisition mode: – in case of LTR210 installed in crate LTR-U-1-4 – in case of LTR210 installed in another crate	 200 kHz (the in single-channel mode), 100 kHz (in the bichannel mode) 500 kHz (in the single-channel mode), 250 kHz (in the bi-channel mode)
Duration of signal writing at the maximum ADC conversion frequency of 10 MHz: in the single-channel mode in the bi-channel mode	 1.6 s 0.8 s
Maximum total amount of data readings in the start-stop mode	Up to 16 million ADC data samples
Range of history data readings amount setting (prior to to the synchronization event) in the start-stop mode	From 0 to 16 million ADC data samples with 1 sample pitch
Main element of LTR210 architecture	FPGA Altera Cyclone III with software-updatable firmware.
Flash-memory volume	0.5 MB
ADC data calibration	Implemented by means of FPGA
Digital filtration (and other signal processing functionality) inside LTR210	FPGA is not implemented in the current firmware version but this is technically possible.

Parameter, characteristic	Value, description
Additional information in the data stream from LTR210	– Number of ADC channel – Sub-range of ADC channel – State of digital synchronization input – Feature of continuous data block beginning – Status word of continuous data block end with state flags – Periodic status word with state flags sent in case of no data reading ("life signal" from LTR210, important for cases of long waiting for a synchronization event)
Types of connectors	BNC
Galvanic isolation of ADC input	ADC inputs are galvanically isolated from the ground and LTR crate frame, but the "common wire" circuits of both ADC channels inputs are not isolated from each other. Galvanic isolation characteristics: In accordance with Appendix A.18, page 362
Galvanic isolation of multifunctional digital synchronization input/input-output	Absent. The common wire circuit of this input-output is connected to LTR crate frame.
Power consumption	4.2 W

A.16. LTR crate reference generator

Parameter	Value
Characteristics of single reference generator of LTR crates:	
– frequency	60.000 MHz
– frequency stability	±50 ppm under operating conditions, see Appendix A.19, page 362

A.17. Characteristics of circuits at synchronization connectors of LTR crates

LTR-U-1-4 crate

Parameter	Value	Note
Number of synchronization inputs	1	SYNC
Number of synchronization outputs	0	SYNC
Static parameters of synchronization input signal: – Logic zero level, max. – Logic one level, min.	 0.5 V 2.4 V	
Pull-up resistors at input	20 kOhm relative to GND	

Parameter	Value	Note
Dynamic parameters of synchronization input signal: – Maximum duration of signal transition – Minimum pulse duration	 Unlimited 100 ns	
Static parameters of synchronization input signal: – Level of logic zero without load – Level of logic one without load	20 kOhm relative to GND 0 – 0.2 V 3.2 – 3.3 V	

Characteristics of signals and supply circuit of external device at SYNC connector in crates LTR-EU-2-5, LTR-EU-8, LTR-EU-16, LTR-CU-1-4, LTR-CEU-1-4

Parameter, characteristic	Value, description	Note
Number of synchronization inputs	2	DIGIN1, DIGIN2
Number of synchronization outputs	2	DIGOUT1, DIGOUT2
Static parameters of synchronization input signals: – Logic zero level, max. – Logic one level (LTR-EU-2-5, LTR-EU-8, LTR-EU-16): – Logic one level (LTR-CU-1-4, LTR-CEU-1-4):	 0.5 V 2.4 V – 5.0 2.4 V – 3.3	 Compatibility with logic elements with power supply voltage of max. +5.0 V. Compatibility with logic elements with power supply voltage of max. +3.3 V.)
Pull-up resistors at synchronization inputs	No	
Dynamic parameters of synchronization input signal: – Maximum duration of signal transition – Minimum pulse duration	 Unlimited 100 ns	
Static parameters of synchronization output signal: – Logic zero level: – Logic one level	 0…0.1 V 0.4 V 3.2…3.4 V 2.8…3.0 V	 Without load At output current of 12 mA relative to 3.3 V Without load At output current of 12 mA relative to GND
External device power supply circuit “+3.3V” – power supply voltage – maximum long-term load current – short circuit protection	 +3.15...+3.45 V 160 mA Heat protection of voltage regulator (see the note).	LTR-EU-8/16 crates released before March 2010 have maximum long-term load current of 100 mA in +3.3V external device power supply circuit. Special upgrade of these crates is required to ensure current supply of 160 mA (required when connecting RS485-UART cable, see table 2-5).

Note: Triggering of heat protection of voltage regulator in LTR-EU-8/16 crates in external device power supply circuit +3.3V will preserve the serviceability of the rest crate units (with no loss in data acquisition process). Triggering of heat protection of voltage regulator in LTR-EU-2-5 crate will cause de-energizing of the crate controller, and after recovery, to reloading of Blackfin processor of the crate controller (with loss of connection via interfaces and unavoidable loss of collected data). In LTR-CU-1-4, LTR-CEU-1-4 crates, short circuit "+3.3V" is also undesirable

A.18. Galvanic isolation in LTR

In compliance with the specification ДЛИЖ.301422.0010 ТУ, galvanic isolation of signal circuits of LTR must correspond to the following requirements:

Isolation	Test voltage
Isolation between combined connector contacts of each LTR module from one side and LTR grounding terminal[1] from the other side	AC voltage of sinusoidal shape with a frequency of 50 Hz and mean-square value 820 V for 1 min
Isolation between connector contacts of each LTR module from one side and combined contacts of other measuring modules in LTR from the other side	AC voltage of sinusoidal shape with a frequency of 50 Hz and mean-square value 820 V for 1 min
Isolation between combined contacts of each measuring channel of LTR27 from one side and combined contacts of other measuring channels of LTR27 from the other side	AC voltage of sinusoidal shape with a frequency of 50 Hz and mean-square value 150 V for 1 min
Isolation between combined contacts of each digital input of LTR41 from one side and combined contacts of other digital inputs of LTR41 from the other side	AC voltage of sinusoidal shape with a frequency of 50 Hz and mean-square value 200 V for 1 min
Isolation between combined contacts of each digital output of LTR42 from one side and combined contacts of other digital outputs of LTR42 from the other side	AC voltage of sinusoidal shape with a frequency of 50 Hz and mean-square value 250 V for 1 min

A.19. Environmental conditions

LTR crate is meant for application in the conditions conforming to the requirements of GOST 22261 (group 3, with extended temperature range). The product must not be exposed to flush blows and impact of weather. Do not place the crate near heavy electromagnetic interference sources as well as in rooms rich of explosive and aggressive chemical compounds.

Parameter	Value
Normal conditions	
Ambient air temperature	(20±5) °C
Relative humidity	30…80%
Atmospheric pressure	630…795 mm Hg
Operating conditions	
Ambient air temperature	+5…+55 °C
Relative humidity	Up to 90% at +25 °C
Storage conditions	
Ambient air temperature	+5…+40 °C
Relative humidity	Up to 80% at +35 °C without moisture condensation

[1] For LTR-U-1-4 crate without grounding terminals, the isolation relative to cable part case of 37-contact connector of any LTR-module (DB-37F connector type) is meant.

Parameter	Value
Other	Absence of dust, acid fumes, alkaline fumes and gases causing corrosion in the air
Transportation terms and conditions	
Ambient air temperature	-25…+55 °C
Relative humidity	Max. 95% at 25 °C

A.20. Power supply of LTR crates

Modification/hardware version of LTR crate	Operating voltage range	Maximum power consumption[1]
LTR-U-16-1, LTR-EU-8-1 LTR-U-8-1, LTR-EU-16-1	(220±22) V from 50 Hz mains, (220±22) V from 50 Hz mains	150 V*A 80 V*A
LTR-U-16-2,	1) (220±22) V from 50 Hz mains; 2) $+12^{+3}_{-1}$ V from DC voltage source	1) 150 V*A 2) 150 W
LTR-U-8-2	1) (220±22) V from 50 Hz mains; 2) $+12^{+3}_{-1}$ V from DC voltage source	1) 80 V*A 2) 80 W
LTR-U-16-3	1) (220±22) V from 50 Hz mains; 2) (+27±3) V from DC voltage source	1) 150 V*A 2) 150 W
LTR-U-8-3	1) (220±22) V from 50 Hz mains; 2) (+27±3) V from DCvoltage source	1) 80 V*A 2) 80 W
LTR-U-1-4	(+11…+24) V (from external power source) (+5±0.5) V from USB	6.5 W (from external power source) and 1.0 W (from USB)
LTR-EU-2-5	(+11…+30) V	19 W
LTR-CU-1-4, LTR-CEU-1-4	(+11…+24) V	10 W

Note: All LTR crates except for LTR-U-1-4 do not use +5 V circuit of USB interface for power supply.to internal units

A.21. Design parameters

Parameter	Value
LTR module parameters:	
– overall dimensions	129 x 144 x 24 mm
– type of connector for user connections	DRB-37M

[1] is achieved in a configuration with the maximum number of LTR212(M) modules with set output reference voltage of 5V and connected external load (8 bridges, 100 Ohm each).

Parameter	Value
Overall dimensions[1]:	
–1-slot LTR crate	135x41x189 mm
–2-slot LTR crate	135x61x189 mm
–8-slot LTR crate	236 x 133 x 378 mm
–16-slot LTR crate	481 x 136 x 406 mm
Reliability:	
– mean time between failures	minimum 40000 hours
– service life	10 years

Other design parameters can be found in table 3-1, page 37.

Overall crates drawings can be found and downloaded on website http://en.lcard.ru/products/ltr when going to the page of corresponding product.

A.22. General requirements

LTR conforms to the requirements of GOST 22261-94, GOST 14014-91, GOST 30605-98 as regards technical characteristics, GOST P 51350-99 as regards safety requirements, GOST P 51522-2011 as regards electromagnetic compatibility.

A.23. Electromagnetic compatibility

LTR meets the requirements for resistance to electromagnetic interference given in Table:

LTR crate	Resistance to electromagnetic interference
LTR-U-16, LTR-EU-16, LTR-U-8, LTR-EU-8	GOST R 51522.1-2011 for the equipment meant for handling in industrial areas
LTR-U-1, LTR-EU-2, LTR-CEU-1, LTR-CU-1 1	GOST R 51522.1-2011 for the equipment meant for handling in controlled electromagnetic environments

Emission of electromagnetic interference of LTR corresponds to the requirements of GOST R 51318.11-2006 for the equipment of group 1, class B.

[1] no allowance being made for projecting parts of connectors, handle for 8-slot crate

Appendix B. Abnormal situations

Do not delete these three paragraphs! Numeration in the section is linked to them!

This Appendix attempts to classify possible abnormal situations in LTR which can occur in real practice and provides troubleshooting recommendations to the user.

Table B. LTR abnormal situations.

External appearance of abnormal situation	Possible reasons	Troubleshooting measures
Computer operating system records unexpected disappearance of connection via USB interface during the operation. Indicator on the front crate panel becomes yellow or blinks for a short or a long time	1). Connection with USB cable is lost or USB cable is defective 2). Common grounding circuit of the computer mainframe and LTR crate is missing through the contact of the grounding of stubs of these devices	Recover the contact, replace the cable See the rules for LTR crate connection to the computer, paragraph3.6.4, page57
Failure of data stream from LTR module which was recorded by the user program (or UTS program) based on the analysis of index information present in each data packet.	1). Bad contact of electrostatic grounding circuit of the module. 2). There is pulse noise with great rate of growth from the external source at the inputs of LTR module relative to crate frame	Tighten bolts on the front panel of module, paragraph 3.6.2, page 51. Consider the recommendations (paragraph3.6.2.2, page52). In-phase interference-suppressing filter should be applied in case of severe interference conditions (L.[3]).
Suspicions on the failure of LTR equipment appeared while operating with LTR with your software.	Your software may work incorrectly, or LTR equipment is really inoperable.	Check LTR functions under the suspicion using LTR -server and UTS programs supplied by L-Card. In case the failure is confirmed, contact L-Card.

The procedure of recovery after a failure of LTR-crate is described in Section 3.9.2, page 65.

A.24. How to get an advice from L-CARD specialist?

A telephone call to L-CARD and explaining the problem "in layperson’s terms"is, as a rule, a pure waste of time (both yours and another person's) because the specialist needs initial data describing your situation. There is a great amount of these **initial data** (you can not remember all), so it is extremely necessary to send the data to L-CARD in writing (e-mail, website conference, fax, regular mail or personal delivery to L-CARD, see the addresses on the reverse side of the title page of this book). The following initial data describing your situation are required:

- What is your name and how to contact you.
- What crate is used and what is the configuration.
- Serial number of crate and modules (this is software-accessible information).
- What computer (which chipset) is used and what type of operating system is used.
- What software and what device driver are used (indicate the version and other information which would help us to understand you).

- What software user settings of the product are used (for example, for LTR11 module: ADC frequency, input range, operating mode (16-channel or 32-channel), which channels are polled and other user settings).
- Which configuration of jumpers is used on the board (if any).
- External connections diagram (textual description of connections or a diagram sketch), numbers of connectors contacts and approximate length of wires must be specified.
- What signal sources are used and what internal resistances they have.
- Estimation of levels of the signals applied to the product contacts, which type of signal is used (point out specific parameters of signal, if known, pulse or sinusoidal, stray or periodical, frequency bandwidth).
- Under which conditions the product is being handled (laboratory, production).
- Describe the configuration of grounding circuits of the computer, if the sources of signals are grounded and how.
- Finally, describe the observed negative impact providing this description with **at least any metric values or assessments!**

If you do some work and provide these complete initial data, our specialist will be able to send you the most accurate and correct answer within the shortest possible time!

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