A family of universal modules of the ADC, DAC

Measuring voltage converters

E-502-P-EU-D-I
E-502-P-EU-D
E-502-X-EU-X
E-502-X-U-D
E-502-X-U-X

User manual

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L-CARD

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Revision history of this document

Date	Document revision	Contents of the change
09.2014	1.0.0	Preliminary data
05.2015	1.0.1	The operating temperature range has been changed (fig. 1-1), upgraded Chapter 2, Chapter 4. Added section 4.8, Chapter 7, technical data corrected – Chapter 5.
05.2016	1.0.2	Order option **E-502-X-EU-X** has been added to the section 1.1.
10.2016	1.0.3	Fixed bugs in the drawings 6.3
01.2017	1.0.4	Information on the industrial design version is included. Amended fig. 1-1.
01.2017	1.0.5	The error about the presence of pull-up resistors on DI inputs is corrected (s.5.3,6.3)
01.2017	1.0.6	The operating temperature range in the table of section 5.9 has been brought into correspondence, amended the section 5.8, the tables in subparagraphs 1.1.1 are amended, 2.1
02.2017	1.0.7	Paragraph added 3.3.4.1
06.2017	1.0.8	Comments are added to sec. 2.3.3, section is added. 2.8
06.2017	1.0.9	A warning is added to item. 3.3.5.2
10.2017	1.1.0	Added industrial design versions. The characteristics according to the results of preparation of the family of *L-CARD voltage measuring converters* for certification as Means of Measurement are brought into correspondence. Added to item 3.3.8. Paragraph added 4.7

When reading this document electronically, to facilitate navigation, use the electronic tree of the table of contents (for example, Acrobat Reader), as well as hyperlinks within the document.

Contents

Chapter 1. General description.

L-Card presents a data collection system **E-502** on the basis of USB and Ethernet interfaces. **E-502 –** is a system developed by LLC "L-Card". It is made on the basis of high quality production of the company, it provides its own technical support and maintenance.

E-502 has the continuity of architecture with L-502: only the interface with the PC with the same functionality as the L-502 is subjected to processing, except for the small functional differences that will be discussed in this manual (s. 3.5, p. 29). The E-502 and L-502 software has also has continuity (common library functions of the upper software level of the PC, identical to the software at the Blackfin level).

The most important characteristics of E-502:

- ADC: 16 bits, conversion frequency up to 2 MHz, with switching to 16 differential channels or 32 channels with common ground. Subranges: ±10 V", "±5 V", "±2 V", "±1 V", ±0.5 V, ±0.2 V.
- Modification E-502-…-…-D has DAC support: 16 bits, 2 channels, output ± 5 V, asynchronous or synchronous mode with a conversion frequency of up to 1 MHz for each channel.
- Digital input: up to 17 digital inputs of general purpose, asynchronous or synchronous data output mode with a frequency of up to 2 million words per second.
- Digital output: up to 16 digital outputs of general purpose, with separate control of the output resolution of the high and low byte, asynchronous or synchronous data output mode with a frequency of up to 1 million words per second.
- Processor (modification E-502-P-…) Blackfin 530 MHz, SDRAM 32 MB, the JTAG connector allows to activate ready "advanced" signal processing and control functions inside the **E-502** or independently to be engaged in low-level programming of these functions.
- Galvanic isolation provides isolation of digital and analogous signal inputs/outputs to all computer circuits.
- The system can consist of one or more **E-502** modules, synchronized from each other, from an internal or external synchronization source with an ADC conversion frequency of up to 1.5 MHz.
- Design version "I" (E-502-…-…-…- I) has an industrial temperature range and a lacquer seal.

The **E-502** notation system is given in fig. 1-1.

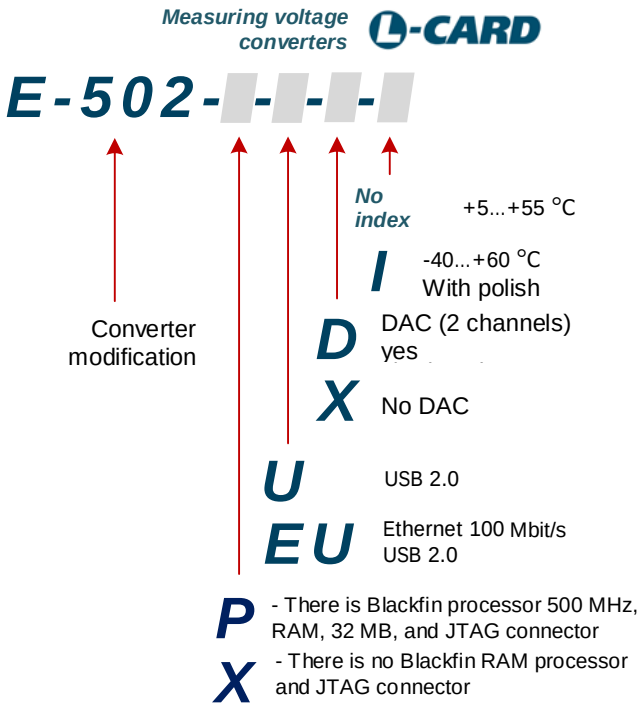


Fig. 1-1. The notation system of the E-502 module

1.1. Order information

The E-502 versions and design versions available for ordering:

E-502-P-EU-D-I,

E-502-P-EU-D,

E-502-X-EU-X,

E-502-X-U-D,

E-502-X-U-X.

When choosing the modification of the E-502 module for the order, it should be noted that when you contact the L-Card sales department, the **previously purchased E-502 module can not be modified to another modification or design version**.

Information on other modifications and design versions you can find in the L-Card sales department (en@lcard.ru).

1.1.1. Distribution kit

Except for the E-502 module, the distribution kit includes the following accessories, depending on the version:

Accessory	Quantity			Note
	E-502-P-EU-D-I, E-502-P-EU-D, E-502-X-EU-X	**E-502-X-U-D**	**E-502-X-U-X**	
DB-37F connector	1 pc.	1 pc.	1 pc.	Cable receptacle
DB-37M connector	1 pc.	1 pc.	1 pc.	Cable plug
Cover DP-37C	2 pcs.	2 pcs.	2 pcs.	For DB-37 connectors
DJK-10A straight connector	1 pc.	1 pc.	1 pc.	To connect low-voltage power from a non-standard power source.
Cable Ethernet Pathcord 5e, L=1.5 m	1 pc.	–	–	
USB cable, type A-B, L=1.8 m	1 pc.	1 pc.	1 pc.	
Power adapter network adapter ~ 220V/ = 12V, 0.5A, unstabilized	1 pc.	1 pc.	1 pc.	Linear transformer power supply for mains supply ~220 V, 50 Hz
Jumper	2 pcs.	2 pcs.	2 pcs.	For all E-502 jumper modifications, the enable configuration of the digital outputs is included. The remaining jumpers are pre-installed inside the E-502 by "default", s. 2.1, p. 11

1.2. Appearance and main structural elements

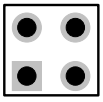
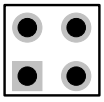
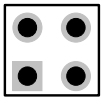
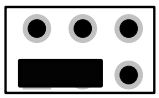
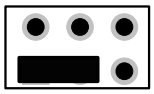
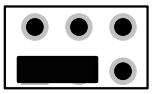
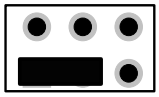
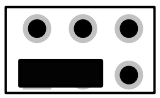
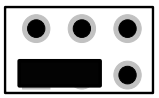
Fig.1-2. Front view (front panel)

Fig.1-3. Back view (back panel)

Chapter 2. Installation and configuration.

2.1. E-502 configuration "by default".

E-502 comes with presets "by default" corresponding to the table below.

Configuration	**E-502-P-EU-D** **E-502-P-EU-D-I**	**E-502-X-U-D**	**E-502-X-U-X** **E-502-X-EU-X**
Setting the resolution of the high and low byte of DO digital outputs on the *Analog* connector	Programmed control (no jumper on fig. 2-1 on the left) 	Programmed control (no jumper on fig. 2-1 on the left) 	Programmed control (no jumper on fig. 2-1 on the left) 
Output setting DAC1 / +15V / AGND / NC on *Analog* connector	DAC1  (See fig. 2-1)	DAC1  (See fig. 2-1)	NC  (See fig. 2-1)
Output setting DAC2 / -15V / GNDD / NC on *Analog* connector	DAC2  (See fig. 2-1)	DAC2  (See fig. 2-1)	NC  (See fig. 2-1)

"L-Card" installs this configuration using jumpers on the board (fig. 2-1) – inside the pack. See configuration explanation in subsection 2.2.1, 2.2.2.

Note: How to programmatically resolve the Ethernet interface, explained in p. 2.8.

2.2. Internal construction elements and E-502 configuration.

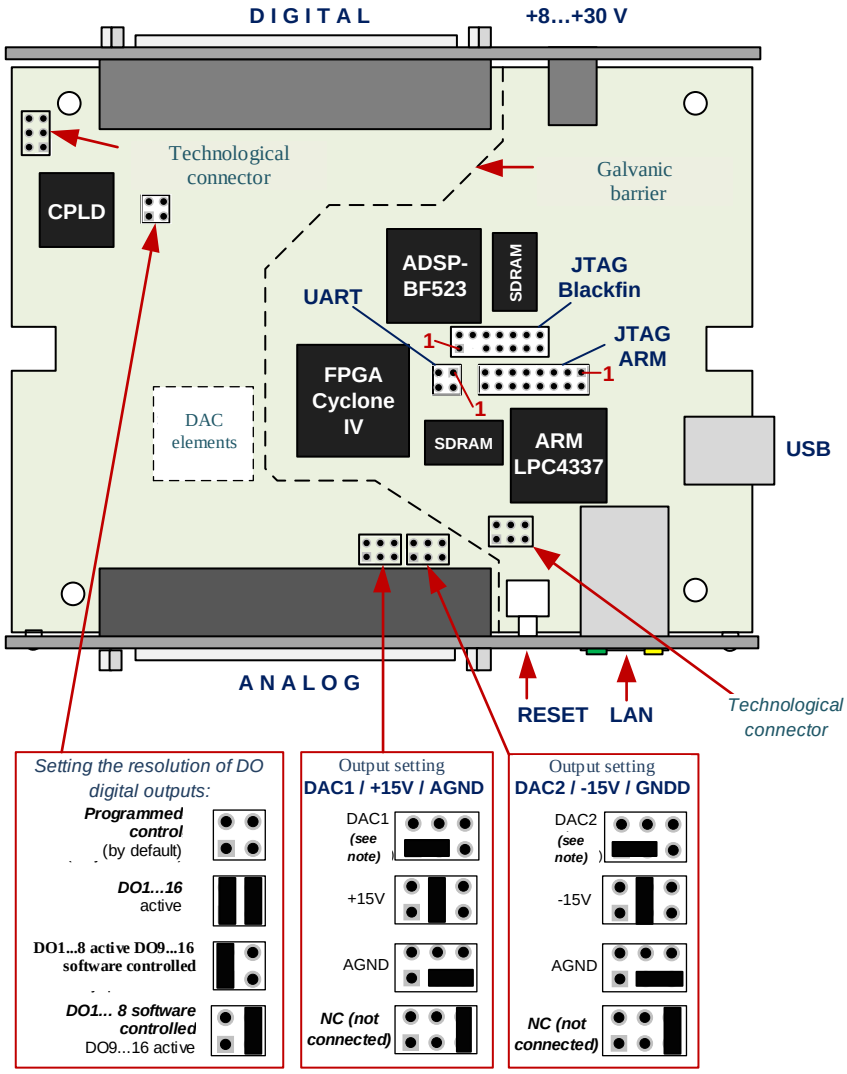


Fig. 2-1. Internal configuration

Note to fig. 2-1: in modules **E-502-X-U-X, E-502-X-EU-X** (without DAC), state of DAC1 or DAC2 is equivalent to the unconnected state of this output.

Attention! Technological connectors are not designed for user connections.

To access the elements of the internal structure, carefully remove the rubber feet from the bottom of the chassis, unscrew the 4 screws and disassemble the housing covers. Reassemble in the reverse order.

2.2.1. Configuration of the DAC outputs of the connector Analog (DAC1/+15V/AGND/NC and DAC2/-15V/DGND/NC)

If your modification E-502 (fig. 1-1) has DAC, then "by default" the DAC within E-502 should be connected to contacts 18 and 19 of the connector *Analog* (fig. 4-3, p. 32).

If necessary, you can independently change the configuration of these outputs by rearranging the jumpers, according to fig. 2-1.

Analog connector is described in section 4.4.1, p. 31.

2.2.2. Configuration of the resolution of the active state of the digital outputs DO1 ... DO16 on the Digital connector.

Activation of the digital outputs on the *Digital* connector (fig. 4-4, p. 34) is done in a programmatic way "by default", and, as practice shows, users are satisfied in the overwhelming majority of cases.

But, if necessary, digital outputs can be activated at power-up (without the possibility of programmed transfer to the *third state*) – in this case, you need to install one or two additional jumpers according to fig. 2-1. This setting is made when the initial high-impedance state of the digital outputs is not permissible for the connected load.

2.3. Functions of the status LEDs on the front panel.

2.3.1. LED1.

Usually LED1 on the front panel indicates a status of the module data collection:

LED1 state	Description
Red light	E-502 is connected and in the synchronous I/O standby mode.
Green light	E-502 is in the synchronous I/O mode.
No lights	Power is off.

In case of using more than one E-502 module, the user faces the task of identifying the module with which the program is currently running. To solve this problem in a visual manner, you can use the software function of controlling the red glow of LED1. Of course, the task of automatic module identification can be solved with software, reading the module's available serial number.

Note: behavior of LED1 on E-502 is identical to the behavior of LED on the L-502 panel.

2.3.2. LED2.

The LED2 on the front panel indicates the state of USB interface

LED2 state	**Description**
Constant red light	There is a USB connection at the Full-Speed (up to 12 Mbit/s)
Non-periodic short red light	Data transfer via USB at the Full-Speed (up to 12 Mbit/s)
Constant green light	There is a USB connection at the High-Speed (up to 480 Mbit/s)
Variable green light	Data transfer via USB at the High-Speed (up to 480 Mbit/s)
Yellow orange light	No USB connection (no cable connected, no drivers installed or the PC operational system has not found a USB-device E-502)
Periodically changing red-green glow	E-502 is in the service "bootloader" mode, or after holding RESET button, or in the software update process.
No lights	Power is off
Slow periodic red light after power is on	SDRAM test error. If the E-502 got into this state after power-up, this could be either a sign of E-502 failure or a sign of the heavy external electromagnetic environment in which the E-502 is located, which led to a malfunction. Contact the "L-Card" technical support if the E-502 gets into this state after turning on the power.

2.3.3. LEDS Link and Activity (on LAN connector) in modifications E-502-P-EU.

Link LED status	**Description**
Yellow glow	Connected to Ethernet
No glow	No Ethernet connection

Note: in the current manufactured products, the opposite logic of the LINK LED illumination is possible (this feature is not a malfunction of the E-502). But, in any case, if E-502 is programmed to operate with USB, **Link** and **Activity** LEDs will not glow.

Activity LED status	**Description**
Green glow	Data transmission via Ethernet
No glow	No data transmission via Ethernet

How to programmatically resolve the Ethernet interface, explained in p.2.8.

2.4. RESET functions

The secret reset button is used to reset the ARM controller, after which the E-502 will normally restart the ARM-controller. For a normal restart, briefly press the RESET button.

The "loader" service mode will be activated after holding the RESET button for at least 10 seconds. The periodically changing red-green glow of LED2 indicates that the E-502 is in the bootloader mode.

2.5. Serial number. E-502 version number. Module identification in a multi-module configuration.

The unique eight-digit product serial number (on the label on the bottom of the case) serves to identify the module instance within its life circle. E-502 serial number is program-available.

2.6. E-502 application as a part of user programs

LLC "L-Card" supports integration of its modules in the user systems. But when E-502 is included in any system, the system developer must mention in the documentation for his system the E-502 module of the "L-Card" production, as the component part (the completing unit).

2.7. Software installation

To install the necessary drivers and libraries for Windows OS, you must download and run the installer "L-Card L502 / E502 SDK" http://www.lcard.ru/download/lpcie_setup.exe.

For information on installing the driver and libraries under Linux OS, see http://en.lcard.ru/download/x502api.pdf.

2.8. Ethernet interface configuration

To work with E-502 module via Ethernet, it is required to make settings and resolution of this interface in the program "L-Card Measurement Studio" (https://bitbucket.org/lcard/lqmeasstudio/), connecting the module via USB. If Ethernet interface is not permitted, the E-502 module will not respond to the connection of Ethernet cable (both LEDs **Link** and **Activity** on the LAN connector will be turned off).

Chapter 3. The mechanism and principle of operation of E-502.

3.1. Conventions

3.1.1. Convention on numbering

In all products of the L-Card, the numbering of all physical objects (for example, channel numbers) in the description of the principle of action and design is always made from one!

This agreement is completely unrelated to the encoding method in programming, where the numbers of these physical objects can be encoded from scratch or otherwise, in the context of the corresponding library function or programming language.

3.1.2. The assumption on the concept of "frequency"

In the documentation for E-502, the frequency of discrete signals (e.g., synchronization signals) is expressed in Hertz, and not in periods per second, as it is common for frequency for a non-sinusoidal process.

3.2. Introduction (general information)

All modifications of E-502 (fig. 1-1, section 1.1) are made on the basis of the same multilayer PCB. Modification is achieved by different variants of the factory assembly. Changing E-502 modifications after factory assembly is not provided for.

The presence of the ADSP-BF523 signal processor with SDRAM (modification E-502-P-▒-▒) is considered justified for those users who want to get the maximum of on-board signal processing capabilities on-board, as well as for advanced users to have their own low-level programming of the processor, possibly with the use of the JTAG-emulator (s.4.4.3, p. 39).

All E-502 modifications have a galvanic isolation of the signal circuits (for L-502 a galvanic isolation is an option).

DAC with 2 channels (modification E-502-▒-▒-D) allows to display output analog voltage levels or voltage time functions.

ADC 16 bits with a conversion frequency of up to 2 MHz with 16/32-channel circuit switching (up to 16 differential channels, up to 32 with a common ground) with voltage subbands of ±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V, ±0.2 V has an analog ADC path, identical to L-502, with a maximum conversion frequency of 2 MHz.

Note the limitations up to± 1 V of the operating range of the input signal on the Y and GND32 inputs (for details, see 4.6).

Instrumental DAC 16 bits 2 channels ±5 V provides the opportunity of synchronous (streaming up to 1 MHz for a channel), asynchronous mode on the selected DAC channel, including mixed synchronous asynchronous mode on different channels, as well as a cyclic synchronous self-oscillator from the E-502 internal buffer (2 pages of 1.5 Mcounts.)

Digital output, 16 lines. Similarly to a DAC, it is possible to have a synchronous output of up to 1 MHz, as well as an asynchronous output, as well as a synchronous output from an internal buffer. With synchronous output, the frequency is matched to the frequency of the DAC output. The output enable allocated for the low and high byte increases the flexibility of using digital lines, for example,

configuration is possible: 8-bit 2-directional data bus + up to 8 data bits per input + up to 8 data bits per output. This allows the implementation of controlling bus diagrams for complex digital devices (sec. 4.4.2.2, p.38).

!	With synchronous output to the DAC to digital output, operation only in the same synchronous mode is supported: in the mode of streaming output, or a self-oscillator from the internal buffer. At the same time, you can work asynchronously with any output channels.

Note the limitations of the asynchronous output for external synchronization (n.3.3.4.1).

Digital input, up to 17 lines, synchronous mode of up to 2 MHz or asynchronous one. In synchronous mode, the stream from digital lines is synchronous with the ADC stream, but separate and independent of the settings of the ADC data collection frame (the frequency of data collection by digital lines is set separately and does not depend on the ADC frame settings).

It should be noted that in the E-502, the three highest digits in the group of digital inputs (DI14, DI15, DI16) have alternative synchronization functions (table 4-2).

The ADC, DAC, digital input and output streams are synchronized with respect to the same $\mathbf{f_{ref}}$ reference frequency, which can be assigned programmatically: 1.5 MHz or 2 MHz.

Hardware-wise, in E-502, the physical frequency of the ADC and the synchronous digital input is always equal to $\mathbf{f_{ref}}$, and the physical refresh rate of each DAC channel and digital output is $\mathbf{f_{ref}}/2$. Getting all the fractional frequences of the data input $\mathbf{f_{ref}}/n$ and $\mathbf{f_{ref}}/2m$ output fractional frequencies (where m and n are natural numbers) occurs at the hardware processing level in the FPGA and/or in the Blackfin processor.

E-502 has a mechanism of the intermodule synchronization (s.3.3.5, p. 20) to form a single synchronous I/O system.

E-502 has a 32-bit data word format, in the format of which, besides the actual data for input or output, there is also a physical channel number. This hardware binding of the physical channel number ensures that the channel number is mistaken even if the top-level program for some reason lost an arbitrary amount of data.

For advanced users: HOST DMA access mode to the internal memory of the signal processor ADSP-BF523 allows you to apply an independent access channel to the Blackfin internal memory. This creates a huge convenience - "transparency" with low-level Blackfin programming - to see what happens in Blackfin memory on an independent channel. To some extent, HOST DMA can replace JTAG (the convenience of the technology of independent access channel in the signal processor memory has been evaluated by users even in products E-440/ E14-440 by L-CARD!).

Operation modes with E-502 via USB or Ethernet are alternative. E-502 uses 32 bit data words for a transmission via interfaces (in each word the data is counted with the index part).

When using USB, the E-502 has a bandwidth limitation of 5 Mcounts/ s High-Speed, which must be taken into account while applying the E-502.

When operating via Ethernet, the E-502 has a 2.5 Mcounts/s bandwidth limit on the input.

The interface function (USB, Ethernet) in E-502 is performed by a separate 2 cores ARM controller LPC4333/4337, which has a separate JTAG connector on the board and an independent additional UART0 port.

3.3. Operation principle

In section 3.2the general information about E-502 was summarized, in this section further details are presented. This section in many respects repeats a similar section of the manual L-502 due to the similarity of these projects.

3.3.1. Reference frequency

f_{ref} – a signal reference frequency, from which the conversion processes are synchronized to the ADC, DAC, digital input and digital output. The E-502 uses a common reference frequency that synchronizes the start-up of the ADC, DAC, digital input and digital output to an accuracy of an integer division of this frequency. In E-502, the reference frequency source can be internal (2.0 or 1.5 MHz) or external (with a frequency of max. 2.0 MHz). In particular, the reference frequency from the neighboring E-502 module can be used to form a synchronous multi-module system.

3.3.2. ADC channel.

The analog data input channel is a channel with dynamic switching up to 32 input physical analog channels of the E-502 module to the input of a single internal ADC module. The process of switching channels itself is hardware, according to a pre-configured control table. The input process itself is conditionally divided into periodically alternating frame periods and interframe delay with pre-configured durations of these periods (interframe delay, in particular, can be set to zero). Duration of frame, interframe delay, ADC output sample timing - all these times can be configured, but they are always a multiple of $\mathbf{t_{ref}= 1/ f_{ref}}$ - the period of the synchronization reference frequency.

$\mathbf{t_{sw}} = \mathbf{n_{sw}} / \mathbf{f_{ref}}$ – the ADC channel commutation period within the frame, equal to the sampling period of the ADC readouts, where $\mathbf{n_{sw}}$ can be specified by an integer from 1 to 2097152

The preset number of samples in the frame and the size of the control table $\mathbf{n_к}$ can be set from 1 to 256. In each cell of the control table, the physical number of the ADC polling channel is prescribed. Within the frame, the control table will be read completely: from the 1st to the $\mathbf{n_{th}}$ cell and the read sequence of physical channels will be used in the hardware control mechanism of the channel switch.

The cell number of the control table is called the logical channel number. Accordingly, logical channels can be up to 256, and physical - up to 32. For example, it gives the opportunity to obtain a different frequency of polling different physical channels within the frame.

Frame time: $\mathbf{t_k} = \mathbf{n_к} * \mathbf{t_{sw}} = \mathbf{n_к}* \mathbf{n_{sw}} / \mathbf{f_{ref}}$

If necessary, between intermittently following frames, a non-zero interframe delay $\mathbf{t_d}$ with a duration $\mathbf{n_d}$ of synchronization frequency periods can be inserted:

$\mathbf{t_d} = \mathbf{n_d}* \mathbf{t_{ref}} = \mathbf{n_d} / \mathbf{f_{ref}}$, where $\mathbf{n_d}$ can be set with an integer from 0 to 2097151

The frame period is equal to the sum of the frame length and the interframe delay:

$\mathbf{t_{ch}} = \mathbf{t_k} + \mathbf{t_d} = \mathbf{n_к}* \mathbf{n_{sw}} / \mathbf{f_{ref}} + \mathbf{n_d}/ \mathbf{f_{ref}}$

In other words, the frame period $\mathbf{t_{ch}}$ is equal to the period of data collection from the same logical channel of the control table.

During interframe delay, the sample of control words does not advance, and the analog channel switch is always set in accordance with the first cell of the control table.

Frequency of collection from one logical channel of the control table

$f_{ch} = 1/ \mathbf{t_{ch}}= \mathbf{f_{ref}} /(\mathbf{n_к}* \mathbf{n_{sw}}+ \mathbf{n_d})$,

where $\mathbf{f_{ref}}$ can be 2.0 or 1.5 MHz for an internal synchronization or $\leq$2.0 MHz for an external, $\mathbf{n_к} = \{1,2,\ldots, 256\}$, $\mathbf{n_{sw}} = \{1,2,\ldots,2097152\}$, $\mathbf{n_d} = \{0,1,\ldots,2097151\}$.

The above-mentioned frame structure of the ADC data is shown in fig. 3-1. Here, for example, a 3-channel ADC mode operation ($\mathbf{n_к} = 3$) is taken with a non-zero interframe delay $\mathbf{t_d}$.

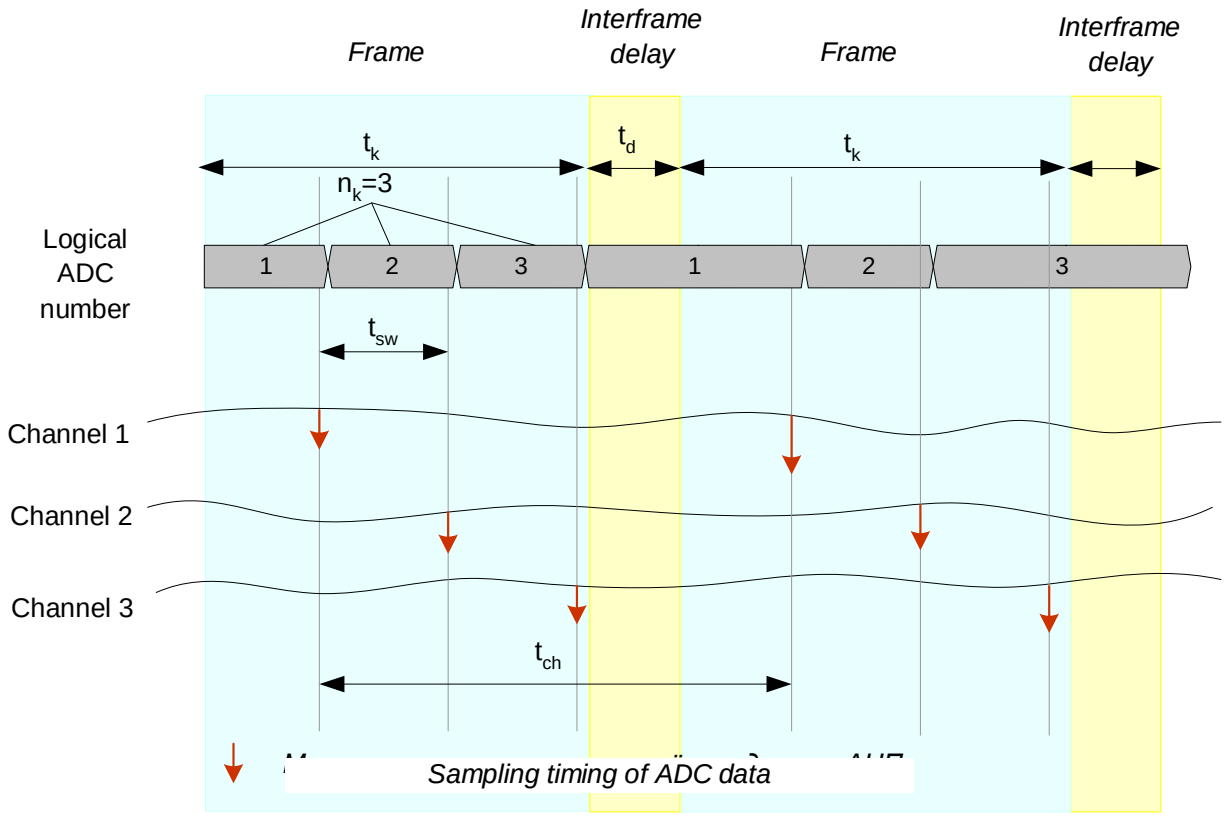


Fig. 3-1. Illustration of the personnel principle for acquiring ADC data

3.3.3. Digital input channel.

Synchronous digital input occurs with a period of $\mathbf{t_{ref}} * \mathbf{n_{din}}$,

where $\mathbf{n_{din}}$ ={1,2,…,2097152} is a configurable frequency division factor for synchronous digital input.

3.3.4. Digital output and DAC channels

Synchronous digital output, as well as updating both channels of the DAC, occurs with a period of 2* $\mathbf{t_{ref}}$. If the data buffer for the output and the DAC is empty, then the last value is held at the outputs.

With any DAC channel and digital output, you can work asynchronously, with the other channels assigned as synchronous, the same synchronous mode is supported: either a streaming or an self-oscillator from an internal buffer.

3.3.4.1. Restrictions on the current implementation of asynchronous output during external synchronization.

Asynchronous output to digital lines and to DAC in the operating mode will always work when configured for internal synchronization. But asynchronous output to digital lines and to the DAC will not function in the standby mode for external synchronization of the start of data acquisition or waiting for more than 1 μs of the external clock of the ADC conversion.

3.3.5. E-502 synchronization general principle.

The fig. 3-2 shows a simplified block diagram explaining the general device of the synchronization system in E-502. E-502 synchronization system consists of two parts: primary and secondary synchronization circuits.

3.3.5.1. Primary synchronization.

The primary synchronization circuit *(I)* according to the settings selects the corresponding external or internal source of the reference frequency, as well as the external or internal source of the start signal. Using the selected signals, circuit ***I*** generates an internal reference signal $\mathbf{f_{ref}}$ as a sequence of synchronization pulses with a period $\mathbf{t_{ref}}$. Moreover, the beginning of this sequence is strictly bound by this scheme to the external or internal *start event*, and all I/O equipment is synchronized (and simultaneously starts) from this sequence: nodes of the ADC (including the logic of the control table), DAC and digital I/O. These nodes contain the corresponding frequency dividers $\mathbf{f_{ref}}$.

We list all possible options for user settings related to the *selection of sources of reference frequency signals*:

- Internal generator 2.0/ 1.5 MHz of this E-502 module (setting by default)
- The reference frequency from the DI_SYN1 input (on the front or on the drop)
- The reference frequency from the DI_SYN2 input (on the front or on the drop)
- The reference frequency from the CONV_IN input from the neighboring E-502, which acts as the master.

We list all possible options for user settings for selecting *sources of the start event of the E-502 I/O system*:

- Program start from PC (default setting)
- On the signal from the input DI_SYN1 (on the front or on the drop)
- On the signal from the input DI_SYN2 (on the front or on the drop)
- By the signal from the input START_IN from the neighboring E-502, which acts as the master.

Each E-502 module always translates via its outputs CONV_OUT and START_OUT, respectively, its internal reference and start signals for one E-502 slave module.

E-502 module can be, at the same time, the master for one or two adjacent modules and the slave for the other adjacent E-502. Thus, synchronization of several E-502, connected by a chain, as well as branching from one master to three slaves, is supported. The possible topology of the synchronization circuits is discussed in detail in sec.4.4.2.1, p.37.

The primary synchronization circuit provides synchronization of the frequency and phase of the ADC, DAC and cycle cycles of the digital input and output system. It is understood that in a multi-module synchronization system, the user will be able to intelligently set the control tables of different modules, as well as the division of the reference frequency for the required input-output processes.

Note that for the slave E-502 there is a frequency limitation at the input CONV_IN – no more than 1.5 MHz. Thus, two or more slave E-502 modules can be synchronized only at a reference frequency of 1.5 MHz from the master.

Stopping the primary synchronization scheme is done only programmatically and asynchronously.

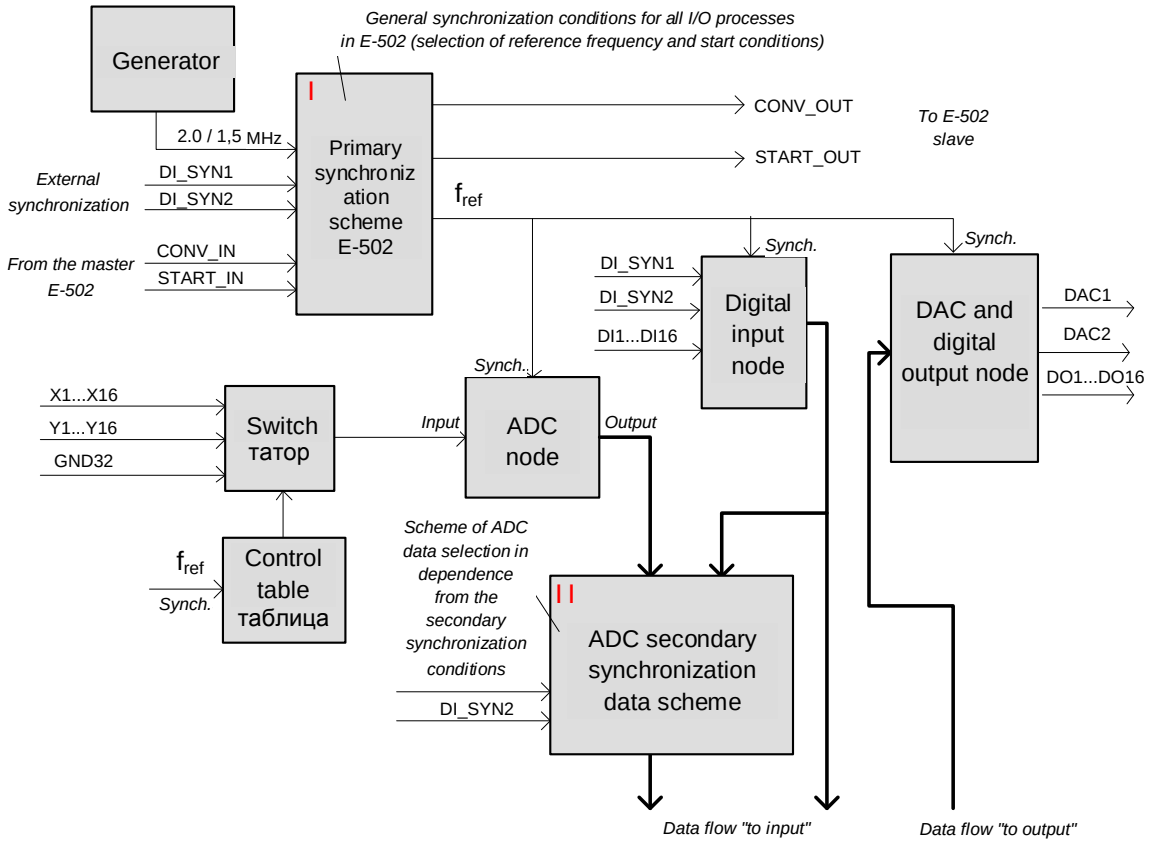


Fig. 3-2. Synchronization system structure in E-502

3.3.5.2. Secondary synchronization.

The functionality of the secondary synchronization is embedded in the project, but is not currently implemented. You can find out about the availability of this functionality in the sales department of L-Card.

The secondary synchronization circuit *(II)* is the ADC data selection circuit depending on the secondary synchronization conditions, operating exclusively against the background of the previously started clock signal from the output of the primary synchronization circuit (***I***), i.e. against the background of the started data stream of the ADC.

The following ADC data resolution synchronization modes are supported:

- No synchronization (transparency mode)
- Synchronization from an analog signal in the selected ADC channel
- Digital synchronization with the selected signal from the inputs DI1 ... DI16, or DI_SYN1, or DI_SYN2

The following modes of sensitivity to the fluctuations of the synchronization signal are supported:

- Enable of ADC data *on the edge (drop)* of an analog or digital signal
- Enable of ADC data at *a level* "above the threshold" or "below the threshold" (for analog synchronization) or *at the logic level* "1" (for digital synchronization)

The following ADC data inhibit modes are supported:

- Software prohibition (stop) with the possibility of re-authorization (if the previously set enable condition is repeated) without restarting the primary synchronization scheme

- Automatic prohibition (stop) after entering the specified number of frames (from 1 to 2^{32}-1 frames) with the possibility of re-authorization (if the previously set resolution condition is repeated) without restarting the primary synchronization scheme

3.3.6. Adjustment of the ratio between the time of setting the signal and the resolution for each ADC channel.

Above was the principle of the frame-by-line input of ADC data, which was applied in all L-CARD ADCs with the input channel switch, up to synchronization frequency, frame size and interframe delay. But in L-502 and E-502 this principle is developed for the better adaptation to the output physical properties of the signal source. Further we will discuss it more precisely.

If E-502 is used at the highest possible data acquisition frequency from each channel, then set $\mathbf{n_{sw}} = 1$, which means that the sampling period of one measurement channel is $\mathbf{t_{sw}} = \mathbf{t_{ref}}$, during which only one ADC sample is converted. For example, for $\mathbf{f_{ref}}$=2 MHz time$\mathbf{t_{sw}} = \mathbf{t_{ref}}$ = 0,5 μs is a fairly short switching period of the channel switch, which imposes restrictions on the output impedance of the signal source (and the wires from it): the impedance should be sufficiently small (not more than 50 Ohm) and not have a large reactive component, so that the duration of the transient process caused by circuit switching does not exceed 0.5 μs. In other words, the signal sourse should be no more than 50 Ohm and have a short or coordinated cable. For those who used the L-783, these requirements and these application conditions roughly correspond to the conditions of application of the L-783 in the multichannel mode at the maximum ADC conversion frequency of the 3 MHz, but with the difference that the ADC resolution of the E-502 is 16 bits rather than 12, and the electronic switch in the E-502 is much more "quiet" (i.e., injects significantly less parasitic charge into the signal circuit at the time of commutation, and therefore causes a significantly smaller shock excitation for a possible transient process in the signal circuit).

But if it is required to use the E-502 at a data acquisition rate for each channel less than the maximum, and it is possible to reduce the switching frequency, then in E-502 with internal synchronization there is no reduction in the frequency of ADC startup, and $\mathbf{n_{sw}} > 1$ is set, for example, as it is shown in the example on fig. 3-1. But, in the sense of $\mathbf{n_{sw}}$ – this is the number of cycles of ADC conversion for one switching period. In the E-502 it is set by default that for $\mathbf{n_{sw}} > 1$, all ADC readouts are flipped, except for the last one, during the switching period. It creates the maximum settling time after commutation (due to "idle" ADC conversion cycles), therefore the least stringent requirements are imposed to the impedance of the signal source. On fig. 3-3, with $\mathbf{n_{sw}}$ =3, such conditions are set "by default" for the logical channel 1: the first two counts are always discarded, and the third one is used. But the real tasks of using multichannel ADCs do not assume that the impedances of the signal sources are the same, and for channels with connected low-impedance sources it would be good not to discard at least some of the ADC samples, but to use them for averaging the data, thereby increasing the enable when measuring this channel. Such option is provided for in E-502 due to the fact that in every cell of the control table, besides the physical channel number, there is also the averaging factor $\mathbf{n_{av}}$, by default, $\mathbf{n_{av}}$= 1. Averaging factor $\mathbf{n_{av}}$ ={1,2,…,128} means: "how many counts of the ADC from the end of the switching cycle of this channel will be used to averaging the data". Accordingly, $\mathbf{n_{su}} = \mathbf{n_{sw}} - \mathbf{n_{av}}$ means "how many ADC counts from the beginning of the switching cycle of the given channel will be discarded", or "how many periods $\mathbf{t_{ref}}$ will be used to set the signal at the ADC input after switching".

For example, on fig. 3-3 for navigational channel 2, $\mathbf{n_{av}}$ = 2 is installed in the control table, which means that for $\mathbf{n_{sw}}$=3 the result of the last two conversion periods in one switching phase will be used for averaging, and one first period is added to the time of signal establishment after switching. For logical channel 3, all three samples of the ADC are used for averaging, and therefore the minimum time is assigned here to establish a signal after switching.

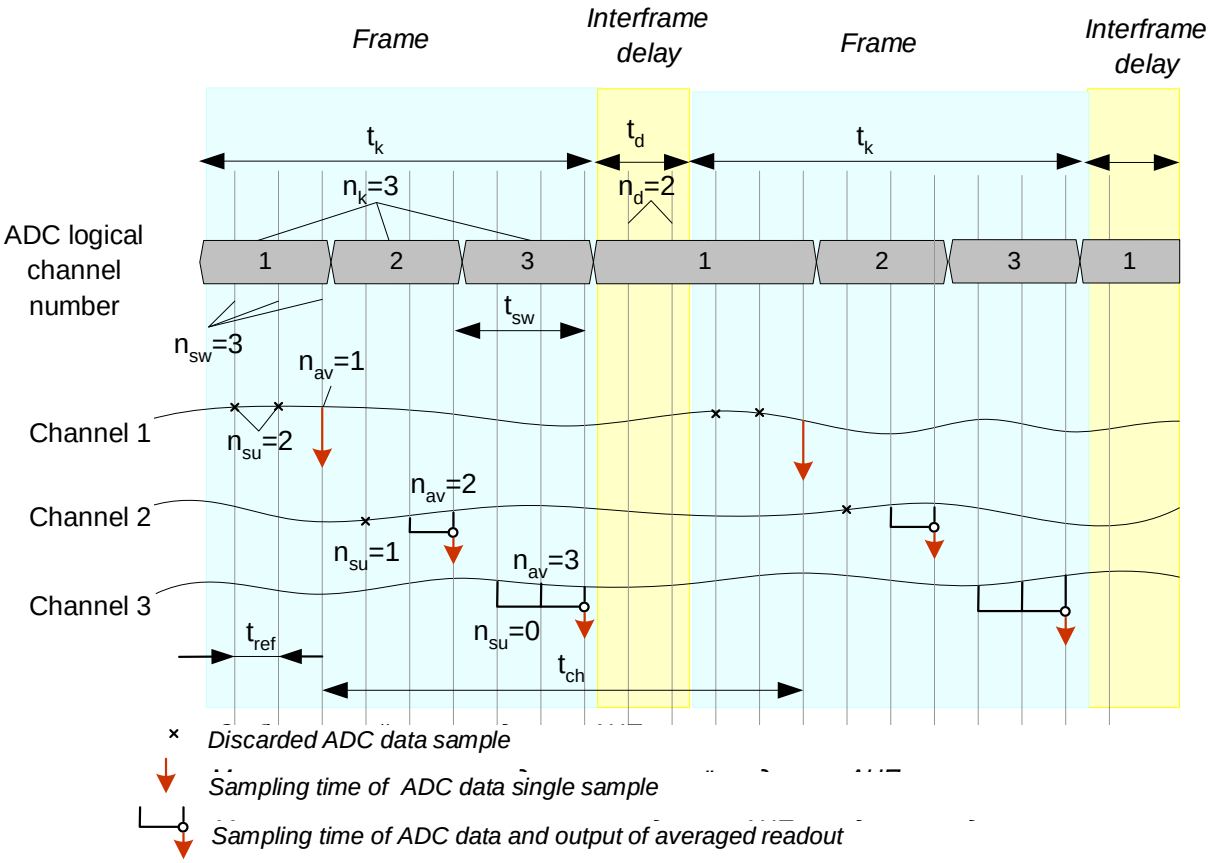


Fig. 3-3. The principle of obtaining ADC data (in detail)

From fig. 3-3 it also follows that the set non-zero interframe delay actually increases the settling time for the first logical channel. This can be used, for example, by associating the first logical channel with the physical channel to which the signal source is connected by the largest impedance.

It can be argued that **by setting optimal n_{su} / n_{av} settings for each channel, we are trying to optimize the *timing of the signal conditioning* associated with the inter-channel passage and the *resolution of the ADC*.**

It is important to note that in the E-502, the ADC averaging algorithm described here (by the simple average method) is considered as an inseparable part of the analog-to-digital converter itself, although physically the averaging procedure is performed by means of FPGA using 24-bit integer arithmetic.

Such an averaging operation increases the real resolution of the ADC by suppressing the random components of the signal of different nature, improves the signal/noise by suppressing the high-frequency components of the spectrum above the Nyquist frequency of 0.5*f_{ch} for a given physical channel associated with one (or more) logical channel. Note in passing that digital filtering by the Blackfin processor (or high-level software) has a fundamentally different active filtering area, because it is below the Nyquist frequency.

Once again, we emphasize that "by default" in the E-502 settings n_{av}=1 is set, and "averaging" does not occur by default.

3.3.7. Relative switching delays in ADC channels.

This information will be important only for that class of multi-channel data acquisition tasks where the magnitude of the relative signal delay between the ADC channels is important for measuring relative phase delays. For this class of problems, the theoretical calculated latency values in the ADC channels are taken into account in the delay equalization algorithm based on one or another method of signal interpolation.

For ADC mode without averaging ($\mathbf{n_{av}}$=1), the relative switching delay between adjacent ADC channels within one frame (in the order of polling the control table) is equal to $\mathbf{t_{sw}}$, and between the last channel of the previous frame and the first channel of the next one is $\mathbf{t_{sw}} + \mathbf{t_d}$.

If the averaging mode is used ($\mathbf{n_{av}}$>1), where $\mathbf{n_{av}}$ are selected equal for all ADC channels, the absolute delay for each channel will decrease by the same amount $0.5*\mathbf{n_{av}}*\mathbf{t_{ref}}$. Therefore, the relative delay will remain equal to $\mathbf{t_{sw}}$ between neighboring channels of one frame and equal $\mathbf{t_{sw}} + \mathbf{t_d}$ between the nearest channels of neighboring frames separated by interframe delay.

If the averaging mode is used ($\mathbf{n_{av}}$>1), where $\mathbf{n_{av}}$ are assigned in the control table different for i- and j-th logical ADC channel, the absolute signal delay on the i- channel will decrease by $0.5\mathbf{n_{av}}(i)*\mathbf{t_{ref}}$, and the relative delay j channel towards the previous i- (within one frame) becomes $\mathbf{t_{sw}} + 0{,}5* \mathbf{t_{ref}} (\mathbf{n_{av}}(i) - \mathbf{n_{av}}(j))$, or becomes equal to $\mathbf{t_{sw}} + \mathbf{t_d} + 0{,}5* \mathbf{t_{ref}} (\mathbf{n_{av}}(i) - \mathbf{n_{av}}(j))$ between the nearest i-th and next j-th channels of neighboring frames separated by interframe delay (if more precisely, for the last channel in the frame always i = $\mathbf{n_k}$, and for first, always j = 1).

3.3.8. Relative delays of the ADC, DAC and I/O channels.

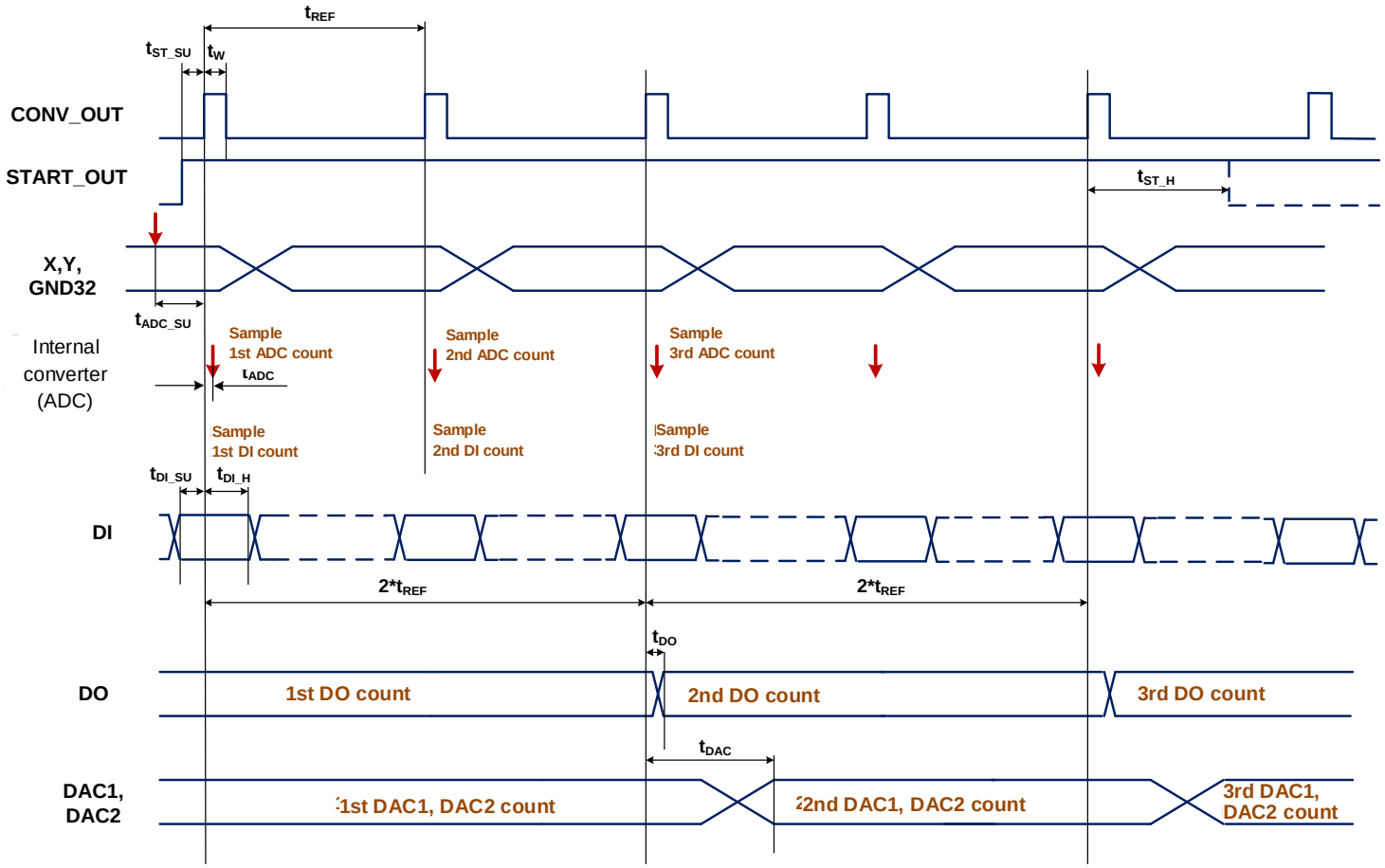


Fig.3-4. Synchronous I/O diagram

In the above-mentioned synchronous I/O diagram, the output signal CONV_OUT is used as a reference clock signal, with respect to which all I/O delays are described. Temporal parameters of the diagram are described in the table below. The delays in the ADC channel are given for the operating mode without averaging the data and without allocating additional cycles of the ADC for setting the signal

Description	**Desig-nation**	**Timing sample**		
		Minimum	**Typical**	**Maximum**
Reference frequency period	t_{REF}		500 ns (2 MHz) 667 ns (1.5 MHz)	
Duration of the signal pulse CONV_OUT	t_W		50 ns	
Group delay time of analog channel of ADC channel in E-502	t_{ADC_SU}		15-70 ns	
The delay time from the front CONV_OUT to the sampling time of the ADC chip	t_{ADC}		0 ns	
The time to set the state "1" to START_OUT before the front CONV_OUT (start of data collection)	t_{ST_SU}	45 ns		

Description	Desig-nation	Timing sample		
		Minimum	Typical	Maximum
Time of holding state "1" to START_OUT after the front CONV_OUT (termination of data collection)	t_{ST_H}	150 ns		
The time to set the data at the DI input	t_{DI_SU}		5 ns	
Data hold time at the DI input	t_{DI_H}		-1 ns	
DO delay time relative to the front CONV_OUT	t_{DO}		6 ns	
The group delay time of the signal at the output of the DAC relative to the front CONV_OUT (delay of the DAC chip plus the delay of the analog filter- buffer at the output of the DAC)	t_{DAC}		2 µs	

3.4. Operation principle and function circuit

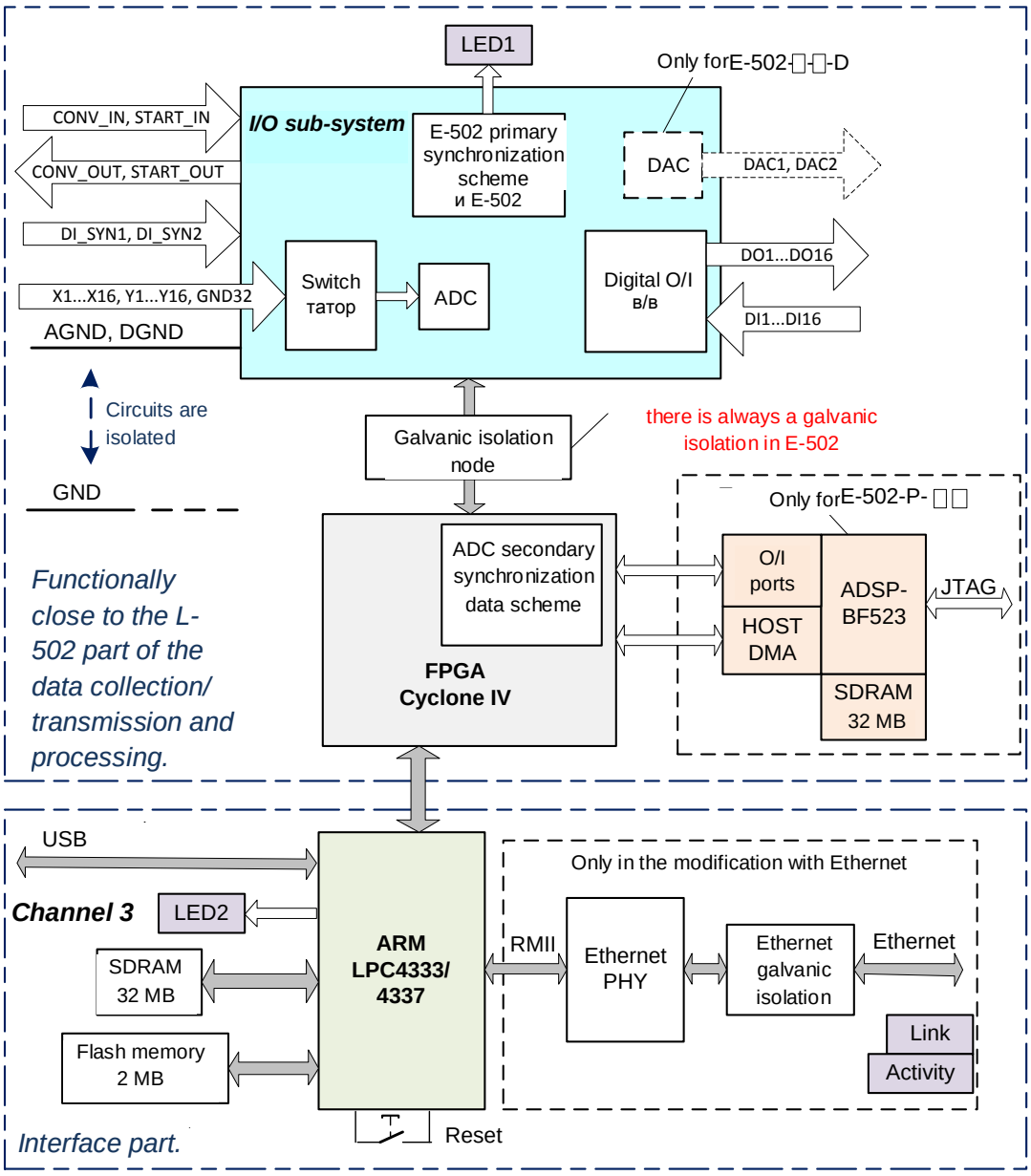


Fig. 3-5. Block diagram

E-502 operational scheme is nominally divided in two parts:

1. **The part related to the collection/output of ADC/DAC data** is digital I/O. This part repeats the architecture of L-502. DAC and signal processor ADSP-BF523 presents depends on the E-502 modification. The FPGA is focused on the logic of data collection control, the ADC calibration logic, the *secondary synchronization logic* (3.3.5), and the interface with the LPC4333 (LPC4337) ARM controller and the ADSP-BF523 signal processor.
2. **E-502 interface part on the basis on LPC4333 (LPC4337) ARM controller, with USB and Ethernet support.** Ethernet option depends on the E-502 modification.

All E-502 modifications have a LPC4333 (LPC4337) ARM controller and a galvanic isolation.

Flash-memory with a capacity of 2 MB is designed for storing FPGA firmware, calibration factors, factory serial number. Half the amount of Flash memory is provided for user tasks.

The E-502 I/O subsystem (in part 1.) contains nodes for the channel switch, ADC, DAC, digital I/O, as well as the *primary synchronization circuit* (3.3.5).

A galvanic isolation node isolated all circuits of the I/O subsystem from circuits electrically connected with any other circuits.

Signal processor ADSP-BF523 with SDRAM 32 MB is designed for additional data processing and management within user tasks. If the processor is enabled, the entire data stream and the I/O subsystem are transferred through the processor's I/O ports. For example, it is possible to create a control loop through a signal processor using all the capabilities of E-502 data collection and delivery. Independent processor and data transfer Interface is performed through the HOST DMA processor port to the ARM-controller. The processor has a JTAG connector on the board.

ARM controller LPC4333 (LPC4337) has its independent SDRAM 32 MB and hidden Reset button, located on the E-502 front panel. The test of this SDRAM is always done after the power is turned on (the error is indicated by LED2, s. 2.3.2, p. 14).

Processors LPC4333, LPC4337 are identical, in terms of their resources involved, and the option of bundling does not affect the consumer properties of the product[1]. ("L-Card" The manufacturer reserves the right to optionally complete the E-502 module either with the LPC4333 or LPC4337 processor without any distinctive product marking and without corresponding differences in product passports.

A short press of the Reset button makes a normal reset of the ARM controller.

A long press (more than 10 s) of the Reset button (s. 2.4, p. 14) shifts the E-502 to a special "loader" mode via USB. A special mode is needed to update the E-502 firmware and change the Ethernet IP address.

After power supply is applied to the E-502, the firmware will be downloaded to the FPGA from the Flash memory (fig. 3-5), and the E-502 internal power supply system will be fully turned on, after which the E-502 will be ready for normal operation.

E-502 switches to work with USB or Ethernet after turning on the power automatically on the interface from which the first access to the E-502 will take place. Parallel operation from both interfaces is not supported.

[1] "L-Card" reserves the right to optionally equip the E-502 module with either the LPC4333 or LPC4337 processor without any distinctive product marking and without corresponding differences in product passports

3.5. All functional differences of E-502 and L-502.

Functional difference	L-502	E-502
Structure	PCI Express card (installed inside the PC)	External module in relation to the PC.
Interface with the PC	PCI Express 1.0	USB 2.0 Ethernet (100BASE-TX)
Intermodule synchronization interface	Uses a different connector. CONV_IN, START_IN inputs have constant pull-up resistors to "zero".	Has a single Digital connector with digital I/O signals. The function of the inputs DI15, DI16 is combined with the function of the inter-module synchronization inputs CONV_IN, START_IN, respectively. DI15/CONV_IN, DI16/START_IN inputs have different programmable pull-up resistors to "zero" (s.4.4.2, p. 34).
The second [2] input of external synchronization DI_SYN2	Is present separately on the internal connector L-502. Programmable pull-up resistor of DI_SYN2 input	Is combined with D14 input. Programmable pull-up resistor of DI14/ DI_SYN2 input
Programmable pull-up resistor of DI digital inputs	Is present (separate for the high and low byte)	No
Galvanic isolation	Not all E-502 modifications have it	All E-502 modifications have it
Cyclic self-oscillator mode for output to the DAC and digital output.	Is supported by PC software driver.	Is supported by the interface ARM controller LPC4333(4337) within E-502, a data buffer 2 pages of 1.5 Mcounts.

Comparing to L-502, in E-502 DAC meteorological characteristics have been improved (s. 5.2) while reproducing direct and alternate current voltage.

[2] The first external clock input DI_SYN1 is available on the external connector in the L-502 and on the Analog connector in the E-502)

Chapter 4. Connection of signals.

This section contains information on E-502 connectors, their contacts' purpose and main characteristics of E-502 inputs and outputs, related to the current connection.

4.1. DGND, AGND circuits

AGND is a *common wire circuit* of isolated analog circuits: ADC inputs and DAC outputs.

DGND is a *common cable* circuit of isolated digital circuits: digital inputs and outputs.

Inside the E-502, **the AGND and DGND circuits have a common connection point** (figuratively: G1), but these circuits are isolated from GND, USBm Ethernet and E-502 power input (fig. 4-1)

4.2. GND, 0 V, GND_USB, CHASSIS circuits

GND is a *common wire circuit* of digital nodes of E-502 module in the non-isolated part.

0 V *is a circuit of the zero potential of the low-voltage* E-502 *power input.*

GND_USB is a common wire circuit of USB interface.

CHASSIS is a circuit for chassis connection (only if E-502 is used without cover – for embedded application) and signal cables display

Inside E-502, **GND, 0 V, GND_USB, CHASSIS circuits have a common connection point** (figuratively: G2). These circuits are connected to the common wire of the ARM controller and the non-isolated USB interface (fig. 4-1).

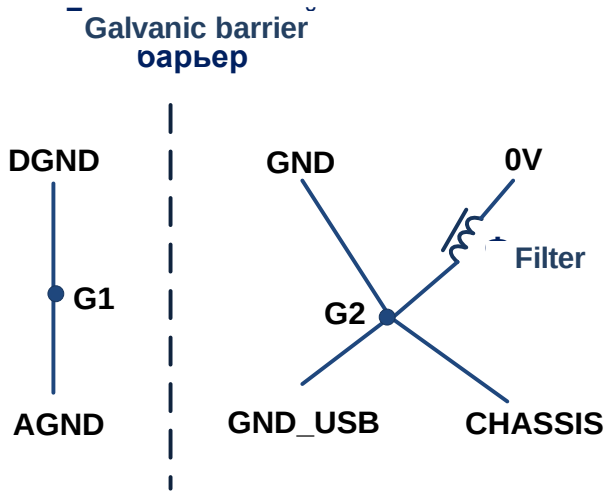


Fig. 4-1: Internal connection of the "common wires" circuits in E-502.

4.3. Location of DGND, AGND, GND, 0 V, GND_USB, CHASSIS circuits on the board

In sub items 4.1 and 4.2the purpose of these circuits is explained, and the figure below shows schematically their belonging to different functional parts of the E-502.

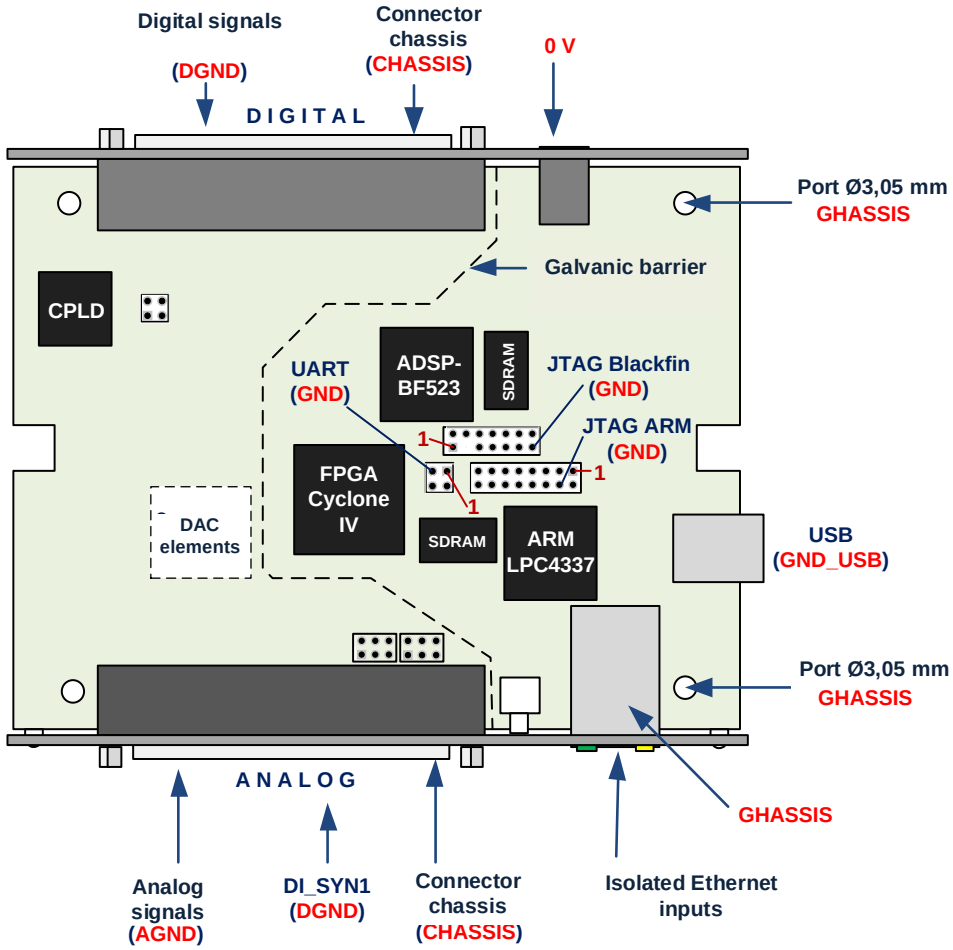


Fig. 4-2: The location of the "common wires" circuits on the E-502 board

In particular, GND is a common wire for internal interfaces UART, JTAG Blackfin, JTAG ARM.

If you use a separate E-502 board without a chassis[3] in the embedded chassis circuit applications (CHASSIS), it is recommended to connect it to the solid metal surface of the chassis (case construction). Two right ports of ∅3.05 mm on fig. 4-2 have a metal coating connected to a CHASSIS circuit, and two left ports of ∅3.05 mm are isolated from the other circuits. These 4 mounting ports are used to secure the E-502 board.

4.4. E-502 connectors description

4.4.1. Connector *Analog*.

Connector Analog is a 37-pin 2-row type DRB-37M plug on the front panel of the E-502. The conductive connector contact piece (shield) is electrically connected to the GND signal ground circuit. On the shield of the cable part of the connector, the shield of the signal cable can be directly sealed. The connector *Analog* shield does not have a contact with AGND, DGND and other circuits of the *Analog* connector.

[3] Here we do not consider the usage accuracy of the certified Measuring Device without a standard chassis.

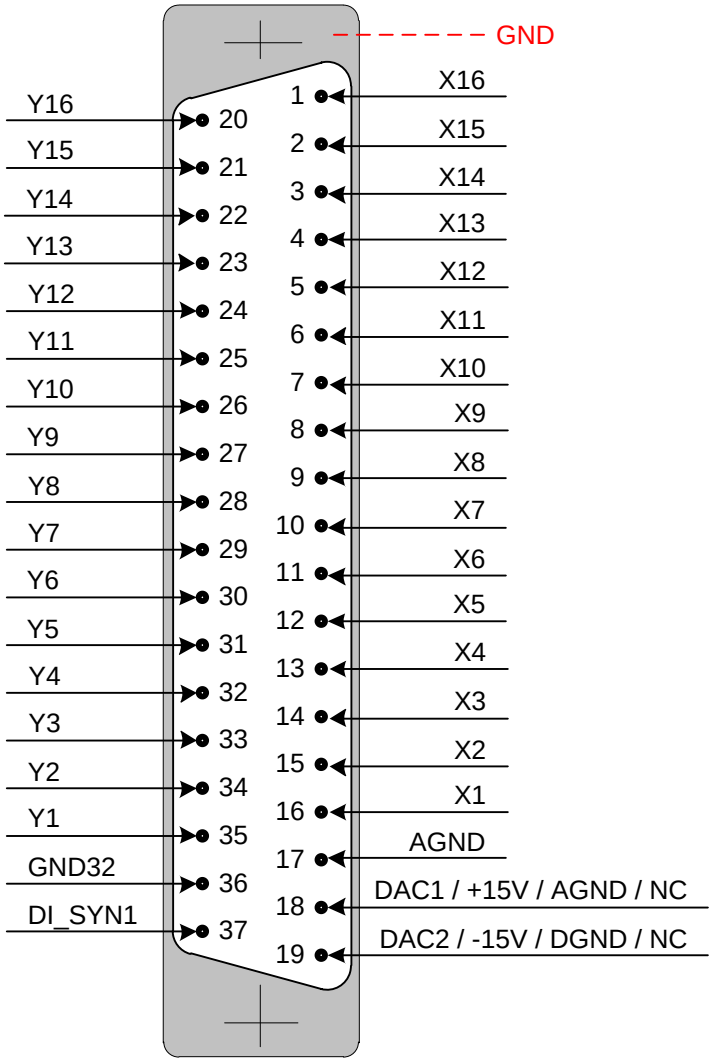


Fig. 4-3: Connector Analog

Table 4-1: Connector Analog

Signal name	Common point[4]	Direction	Description
X<1…16>	AGND	Input	• Non-inverting channel voltage input 1 ... 16 for differential and "common ground" mode: • Operation voltage range: **±10 V (**see the details in section 4.6 p. 41). • Unused inputs X <1 ... 16> are recommended to be connected to AGND or the corresponding physical channel not to be interrogated programmatically.
Y<1…16>	AGND	Input	• Inverting channel voltage input 1 ... 16 for differential mode. • Input channels 17 ... 32 for the mode "with common ground". • Operation voltage range: **±10 V (**see the details in section 4.6 p. 41). • Unused inputs X <1 ... 16> are recommended to be connected to AGND or the corresponding physical channel not to be interrogated programmatically.

[4] The common wire circuit for the specified signal input or output

Signal name	Common point[4]	Direction	Description
DAC1 / +15 V / AGND / NC (see section 2.2.1)	AGND	Output	For modifications, E-502-▒-▒-D can be configured with a jumper as the output of the 1st channel of the DAC (voltage output in the range -5 ... + 5 V). For any modifications, the E-502 can be configured with a jumper as + 15V output of an external device, or as an additional AGND contact, or as an unconnected contact of the connector (NC). (see section 2.2.1)
DAC2 / -15 V / DGND / NC (see section 2.2.1)	AGND	Output	For modifications, E-502-▒-▒-D can be configured with a jumper as the output of the 2nd channel of the DAC (voltage output in the range -5 ...+ 5 V). For any modifications, the E-502 can be configured with a jumper as - 15V output of an external device, or as an additional AGND contact, or as an unconnected contact of the connector (NC). (see section 2.2.1)
AGND	—	—	Analog ground
GND32	AGND	Input	• In the *"with common ground"* mode: common inverting channel input 1 ... 32. • For all modes must be connected to AGND (in differential mode - to increase noise immunity). In the *"with common ground"* mode, the connection to AGND is recommended to do on the signal source side. • Operation voltage range ±1 V **(**see the details in section 4.6 p.41).
DI_SYN1	DGND	Input	Synchronization input 1, which can also act as an additional input to the digital input. Compatible with the output logic level of TTL/CMOS- cells with a supply voltage of +2.5 V to +5 V. The input has an extended range of maximum permissible voltages (± 10 V relative to GND). The minimum rate of rise of the signal drop at the input DI_SYN1 is not specified, since there is a Schmitt trigger on this input. There is a software option to turn the 1k pull-up resistor to a high logic level at this input. The DI_SYN1 input does not bypass the external TTL source, even when the power is off.

Notes to table 4-1:

- The maximum permissible voltages and currents at the contacts of the connectors are indicated in section 4.5, on p.40.

4.4.2. Connector Digital.

Connector Digital is a 37-pin 2-row plug of DRB-37F type on the E-502 front panel. The conductive connector contact piece (shield) is electrically connected to the GND signal ground circuit. On the shield of the cable part of the connector, the shield of the signal cable can be directly sealed. The *Digital* connector shield has no contact with the DGND circuits and the remaining circuits of the *Digital* connector.

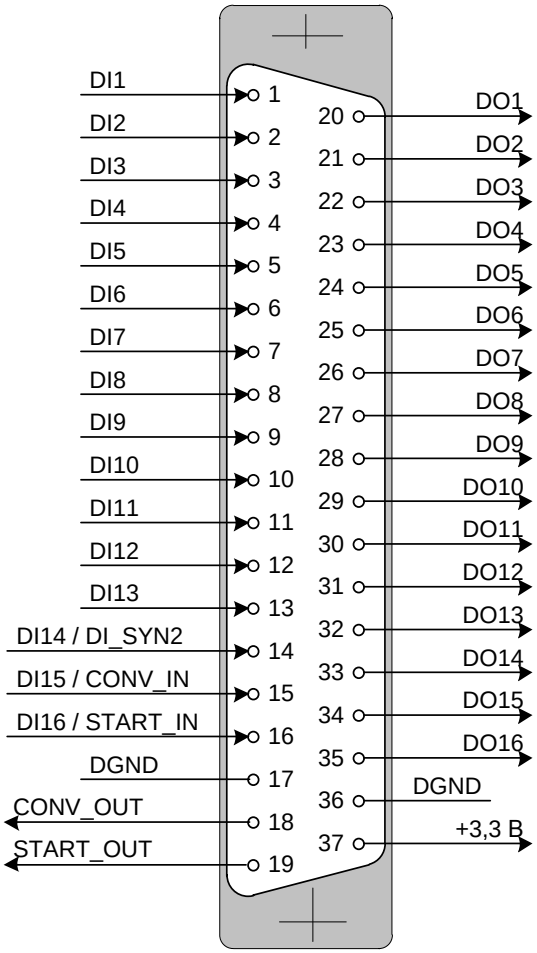


Fig. 4-4: Connector Digital

Table 4-2: Connector Digital

Signal name	Common point	Direc-tion	State after connection	Description
DI<13…1>	DGND	Input	Input	16-bit digital input, where DI1 is the low bit, DI16 is the high bit of the 16-bit word. The inputs DI14, DI15, DI16 are described below, they have alternative programmable functions for the synchronization inputs. The DI input does not bypass the external TTL source, even when the E-502 power is off.
DI14/ DI_SYN2	DGND	Input	Input	Digital input DI14 or synchronization input DI_SYN2 (software selection). The input is compatible with the output logic level of the TTL/CMOS- cells with a supply voltage of +2.5 V to +5 V. There is a Schmitt trigger at this input. There is a software option to turn the 1k pull-up resistor to a high logic level at this input. The DI/DI_SYN2 input does not bypass the external TTL source even when the E-502 power is off.
DI15 / CONV_IN	DGND	Input	Input	Digital input DI15 or synchronization input CONV_IN (software selection). Input of the synchronization pulse of the ADC-DAC conversion (from the neighboring module E-502). It is programmable to turn on a pull-up resistor of 360 ohms to a low logic level at this input. The DI15/CONV_IN input does not bypass the external TTL source, even with the E-502 power off. The input is compatible with the output logic level of the TTL/CMOS- cells with a supply voltage of +2.5 V to +5 V. There is a Schmitt trigger at this input.
DI16 / START_IN	DGND	Input	Input	Digital input DI16 or synchronization input START_IN (software selection). Input of start signal of ADC-DAC and input-output (from neighboring module E-502). Active logical signal level is high. It is programmable to turn on a pull-up resistor of 360 ohms to a low logic level at this input. The DI16/START_IN input does not bypass the external TTL source, even when the E-502 power is off. The input is compatible with the output logic level of the TTL/CMOS- cells with a supply voltage of +2.5 V to +5 V. There is a Schmitt trigger at this input.
DO<16…1>	DGND	Output	Z-state	16-bit digital output, where DO16 – high bit, DO1 – low bit of the 16-bit word. Lines DO1 ... DO8 refer to the low byte, and lines DO9 ... DO16 - to the high one. Program control Z- state is independent for the high and low bytes. It is possible to force the active state of the outputs of each byte when the power is turned on by installing jumper, section 2.2.2.
CONV _OUT	DGND	Output	Output	The output of the ADC-DAC conversion pulse and the I/O (to the neighboring E-502)
START _OUT	DGND	Output	Output	The output of the ADC-DAC start signal and the I/O (to the adjacent E-502 module). Active logical signal level is high.
DGND	—	—	—	A *"common wire"* circuit for digital inputs and outputs.

Signal name	Common point	Direc-tion	State after connection	Description
+3.3 V	DGND	Output	Output +3.3 V	Output +3.3 V supply external digital nodes. Short circuit of the +3.3 V circuit is undesirable, but permissible (causes heat protection of the internal stabilizer).

For the maximum permissible voltages and currents at the contacts of the connectors, see the section 4.5, on p. 40.

4.4.2.1. Connections with intermodule synchronization.

Examples of connections with intermodule synchronization are shown on fig. 4-5 – fig. 4-7. Connections should be made with shortest twisted pairs for a number of E-502 modules located next to each other.

The software of such a system should ensure the start of data collection of the master module after the slave starts and pre-programmed these modules to the appropriate synchronization modes.

It is needed to programmatically turn on the pull-up resistors on the inputs START_IN and CONV_IN to a low logic level on the last slave module in the circuit. It is recommended that no more than 2 adjacent slaves are connected to the same chain with the master. Each slave in the circuit, for example, E-502 #2, as it is shown on fig. 4-7, can, if necessary, become the master for the other synchronization circuit.

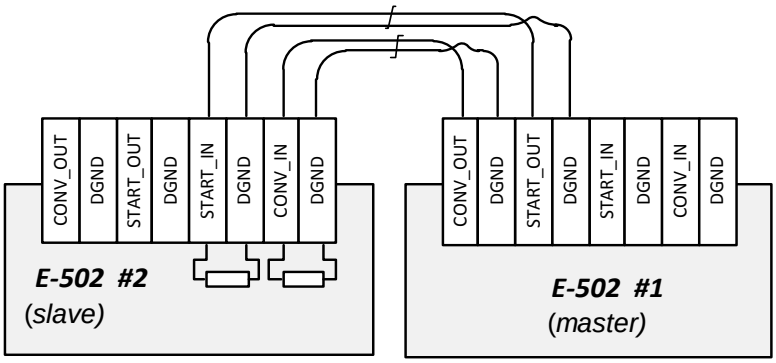


Fig. 4-5: Synchronization scheme master - slave

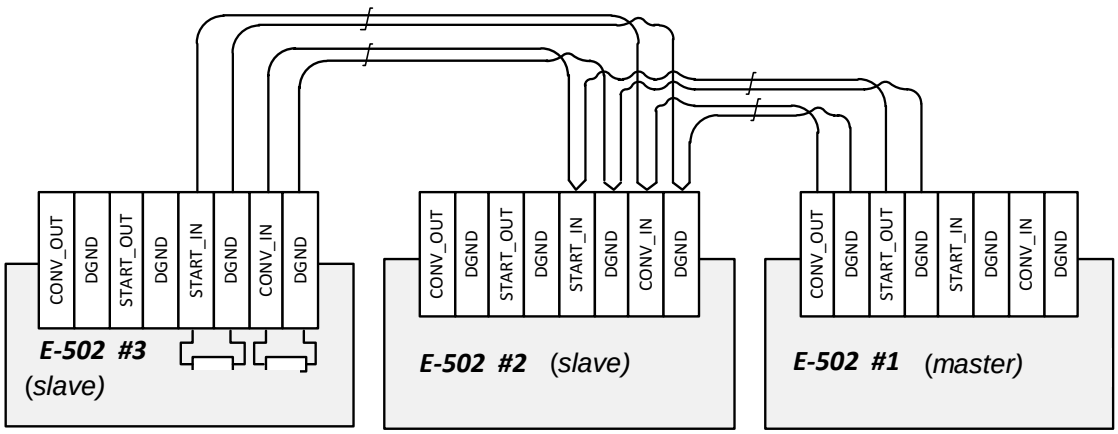


Fig. 4-6: Synchronization scheme master - two slaves

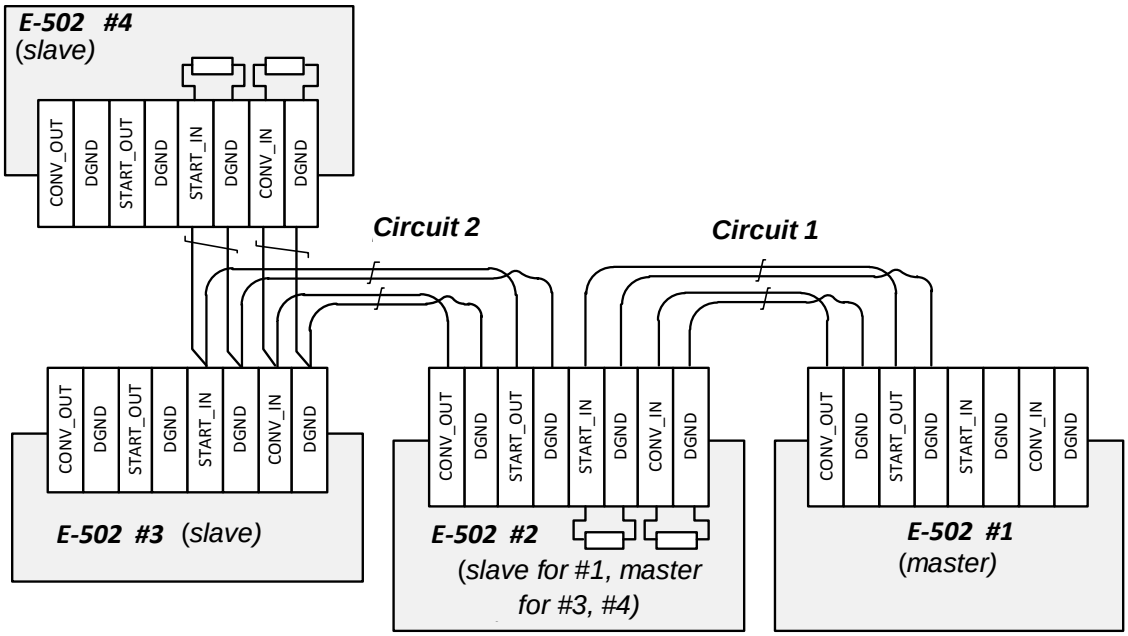


Fig. 4-7: Example of a two-circuit synchronization scheme

4.4.2.2. What gives an independent resolution to the outputs of the high and low byte?

One of the important practical examples is a system of 3 buses with a width of 8 bits each, as shown in the figure below. The first bus is the input one, the second is the output bus, the third is bi-directional.

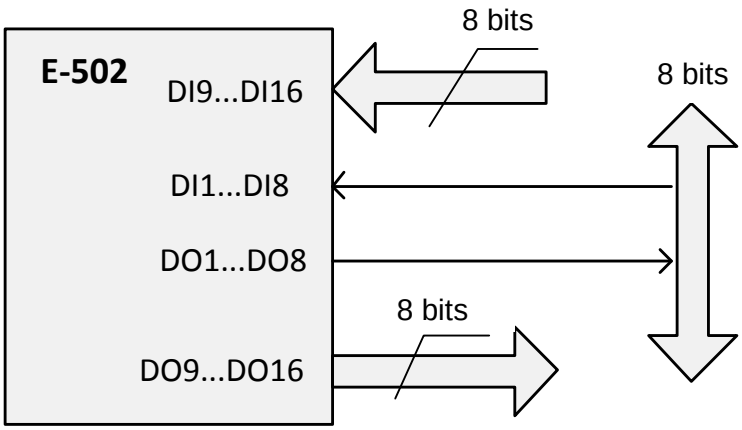


Fig. 4-8: Example of a grouped connection of digital lines: three buses of 8 bits each.

The example shows an almost important case of implementing interfaces with various devices that have an 8-bit bidirectional data bus, input and output control lines. It should be noted that DI14, DI15, DI16 inputs have alternative synchronization functions (table 4-2).

4.4.3. JTAG connectors of Blackfin processor.

To debug your own Blackfin software on the E-502 board, you should use one of the JTAG- emulators from Analog Devices: ADZS-USB-ICE, ADZS-HPUSB-ICE or ADZS-ICE-100B with the USB-interface. They differ significantly with USB transfer rate and price. You can get information on these devices on the manufacturer's website www.analog.com .

The board has a JTAG connector, fig. 4-9, compatible with the above JTAG- emulators.

The operation of attaching and detaching the JTAG-emulator connector should be done in the de-energized state of both devices.

Do not connect the JTAG connector to other devices which are not specified in this chapter.

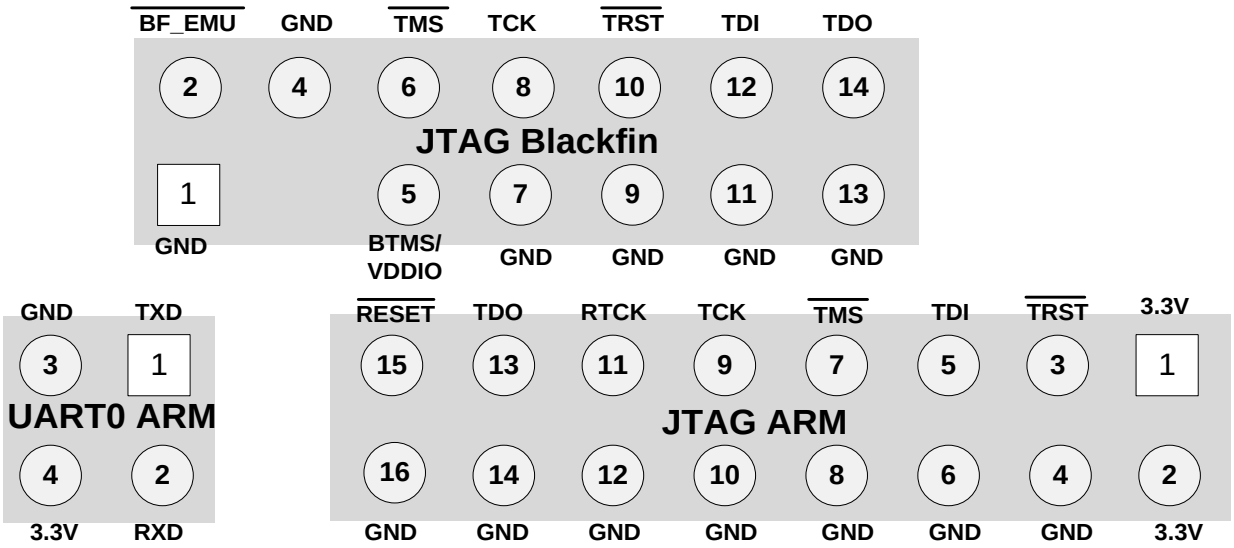


Fig. 4-9. Detailing of signals on JTAG Blackfin JTAG ARM and UART0 connectors

4.4.4. Connectors JTAG and UART0 of the ARM controller LPC-4333 (LPC-4337).

To debug your own Blackfin software on the board, you probably will not need to modify the ARM-controller software that performs the interface function E-502. However, for advanced users such a modification is possible, for example, in order to use the UART0 ARM port for any interface functions.

It is also shown on fig. 4-9 the standard JTAG pinout for ARM, as well as the pinout for the UART0 ARM interface (the location of the connectors on fig. 4-9 corresponds to their actual relative position in the E-502).

The TXD and RXD signals of the UART0 interface have an internal pull-up to 3.3V by resistors of 10 kΩ.

The operation of connection and disconnection the JTAG-emulator and UART0 connectors should be done in the de-energized state of the connected devices.

4.5. The maximum allowable conditions at the inputs and outputs of signal lines.

Under the maximum permissible conditions are meant such currents and voltages that do not lead to failure or irreversible degradation of the characteristics of the E-502. At the same time, the maximum permissible conditions may not provide the performance characteristics of the product.

! Long-term operation of equipment at maximum permissible levels is not allowed

Table 4-3 Maximum permissible E-502 input/output conditions

Circuit/ Signal	**Maximum permissible modes description**
Inputs X1÷X16, Y1÷Y16, GND32	±15 V relative to AGND
Outputs DAC1, DAC2	± 20 mA when the total load power is not exceeded, see section .
Outputs +15 V, -15 V	No more than 30 mA in load circuits when the total load power is not exceeded, see section . SC is not permitted.
Inputs DI_SYN1	± 10 V relative to the DGND circuit with an internal input resistance of, at least, 1 kΩ.
Digital inputs DI1÷ DI13, DI_SYN2	From -0.4 to +6.5 V relative to the DGND circuit
Digital inputs of dual purpose DI14 / DI_SYN2, DI15 / CONV_IN, DI16 / START_IN	From -0.4 to +3.6 V relative to DGND circuit
DO digital outputs	From -0.4 to +3.6 V relative to the DGND circuit, the current is not more than ± 20 mA. When the power is on, the total load power should not exceed the calculated value, according to section ..
TX, RX signals on the internal UART0 connector	From -0.2 to + (Vcc + 0.2) V relative to the GND circuit, where Vcc is the E-502 internal voltage of 3.3V. The load current is not more than ± 8 mA.

Table 4-4 Maximum permissible through currents by common wires circuits:

Maximum permissible through-current by the circuits of one E-502 module: AGND-DGND[5]	100 mA
Maximum permissible through-currents by circuits GND, 0 V, GND_USB, CHASSIS (on any contour into which covers these circuits)	100 mA
The maximum permissible voltage rise rate between galvanically isolated circuits in E-502	10 kV / μs

The maximum permissible circuit modes of JTAG connectors are not considered, since the scope of application of JTAG is limited to the standard types of JTAG emulators and the specified connection procedure, according to i. 4.4.3, p. 39.

[5] The notion of circuits GND, AGND, DGND is introduced in section 4.1

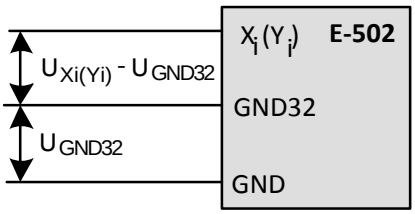
4.6. ADC input operation voltage range

Note that in the differential mode on the sub-bands ±10, ±5 V, the E-502 has unbalanced input and output ranges for the inputs X and Y with respect to the AGND analog ground circuit, and in the "common ground" mode, the E-502 on the same subbands has asymmetrical input signal ranges of the inputs X (Y) and GND32 with regard to the AGND circuit.

Mode "with common ground"

Measured voltage from ±0.2 V to ±10 V, depending from the set subband

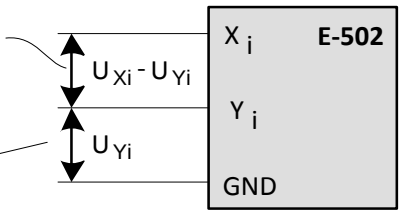
Constant or alternating offset voltage GND32 in the range of ± 1 V.



Differential mode ±10 V or ±5 V

Measured voltage ±10 V or ±5 V, depending on the set subband

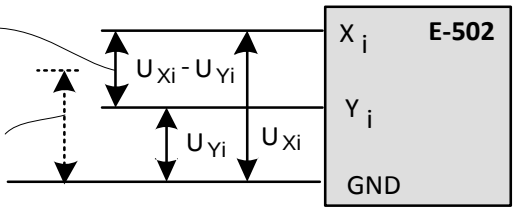
Constant or alternating offset voltage U y; in the range of ± 1 V relative to GND.



Differential mode ±2, ±1, ±0,5 or ±0,2 V

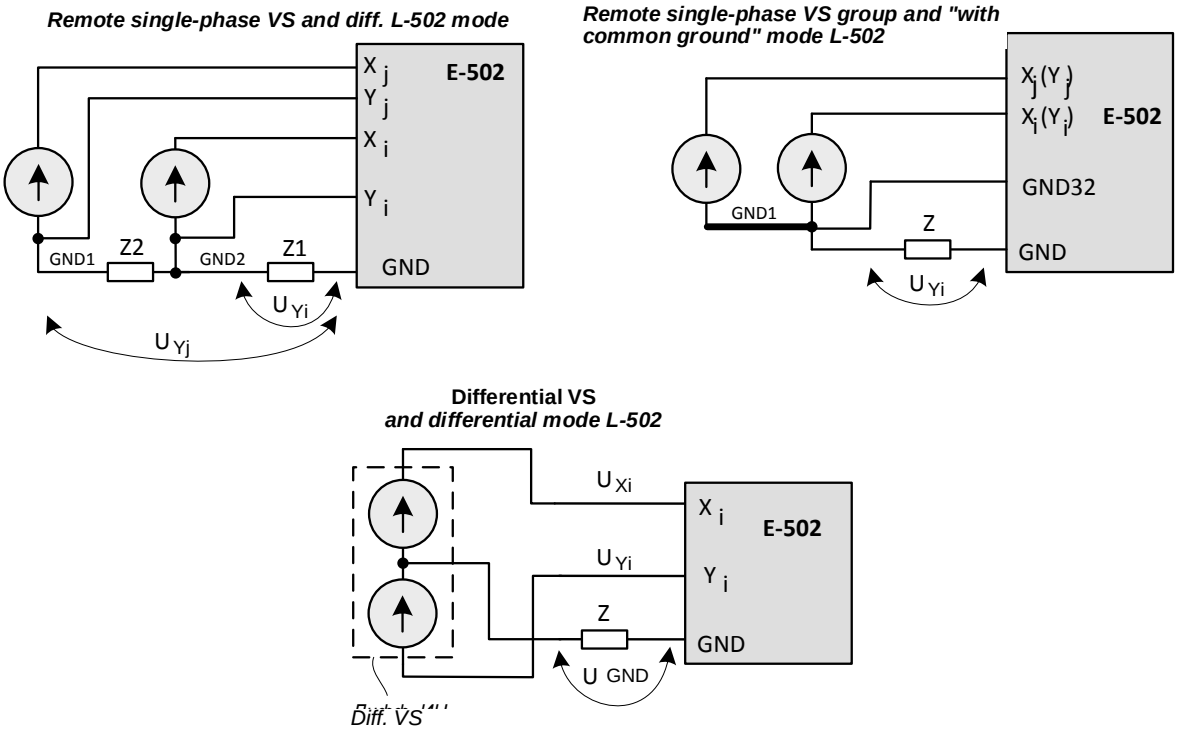
Measured voltage ±2, ±1, ± 0.5 or ± 0.2 V depending on the set subband

Constant or alternating common-mode voltage (Uxi + Uyi)/2 in the range ±1V.



The figure below shows examples of connecting voltage sources (VS) to the ADC inputs.

Z, Z1, Z2 - the intrinsic resistances of the wires (through which the through currents can flow with the connection of different devices) or other external electrical causes inducing the parasitic offset voltage U_{Yi}, U_{Yj}.U_{GND} are indicated. In the first two circuits, the voltage U_{Yi}, U_{Yj} should not exceed ± 1 V in order to ensure the operating mode, and in the latter scheme the common mode voltage (U_{Xi} +U_{Yi})/2 must be within ± 1 V.



Examples of connecting the ADC input are collected in the item 6.1 on page 54.

4.7. Preconditions for correct connection and correct settings of the input of the ADC E-502.

Simplified examples of connection of the ADC input are given in section 6.1, however,

! ... if you do not take into account the electrical properties of the signal sources, wires (cables) when using E-502 ADC connections, use the default E-502 program settings, then, most likely, you will get a bad result. Why? What do you need to consider? – If you answer below these questions, links to the Internet resources of the site en.lcard.ru will be used.

4.7.1. The physical causes of possible problems

Physical cause #1. The wide bandwidth of ADC transmission in E-502 (about 10 MHz) can be not only a big advantage of ADC E-502 (in the ability of the ADC to qualitatively digitize high-speed dynamic processes), but it can be a big problem if:

- the signal source has an unlimitedly wide frequency band (much wider than the width of the frequencies of the useful signal)
- unscreened connection is applied (or the signal source itself has a significant area of the unscreened surface), in a situation where electromagnetic fields in the frequency band up to 10 MHz are always present in the real situation, and also in the situation of the user's failure to apply a differential connection (and adjustment to the differential mode), and therefore use the valuable property of a differential input – effectively suppressing common-mode interference.

Physical cause #2. The high frequency of the 2 MHz channel switch (when tuned to multi-channel mode) with E-502 default settings may not only be a big advantage of the ADC E-502 (in the high-speed ADC input interrogation), but it can also be a problem because of the measuring circuit , it takes a short signal setting time (less than 500 ns after the switch's own charge is injected into the measurement circuit). This cause is fundamental for all ADC with input commutator, manifested as a switching disturbance.

4.7.2. Conditions for correct E-502 connection and settings.

1. If you need to use no more than 16 ADC channels, always select the differential connection mode and E-502 settings.
2. With a differential connection, the X and Y circuits of each channel always lead in pairs (twisted pair, shielded pair).
3. E-502 signal circuit should be shielded. On the screen connection, see 4.4.1.
4. For differential connection, when using a pair cable, to maximize the common-mode rejection of the E-502, the output impedances on the side of the remote source along the X and Y circuits must be balanced (connection example - p.6.1.9).
5. The AGND E-502 circuit should be connected to the common wire circuit of the signal source (if there are several signal sources – to the common junction point of the signal source common wires).
6. If you need to configure the E-502 for multichannel operation, you first need to optimize the signal-to-noise ratio of the ADC in a single-channel operation mode with a maximum data rate of 2 MHz, in which in the signal spectrum you will see all the frequencies of the interfering interference (possibly with "mirror frequencies" if interference is above 1 MHz), which means that you have a tool in your hands to find the

sources and causes of these interferences (before switching to multi-channel mode and averaging mode, when it is more difficult to understand the sources of interference).

7. **When using ("by default") in the multi-channel operation mode of the maximum switching frequency (2 MHz), the output impedance** of the E-502 ***signal circuit*** **must be from 0 to 50 Ω (in the frequency band up to 10 MHz), and this voltage source must be connected to connector E-502 by wires of zero length.** This is achieved either by directly connecting the output of the signal source itself (50 Ω) or by connecting its load resistor (up to 50 Ω) directly to the cable part of the E-502 signal connector (cases of connecting a 50 Ω coherent line or a current shunt to 50 Ω of the external current measurement circuit).
8. **When using a multichannel mode of non-zero length of wires *to the voltage source and (or) with an output resistance of the signal circuit of more than 50 ohms, the program setting of the signal conditioning time* n_{su} > 1 (s.3.3.6) *should be applied.***
9. **In multi-channel mode, the optimal settling time n_{su} (s. 3.3.6) should be selected depending on the output impedance of the signal source, the length and the coherence of the cable.**It is suggested to choose the optimal n_{su} for this channel by the criterion of obtaining a small inter-channel signal transmission from the previous polling channel.
10. **To improve the signal-to-noise ratio and increase the resolution in the measurement path, it is recommended to use the maximum possible averaging factor n_{av}> 1 (s. 3.3.6)** for the required channel polling frequency and the necessary *signal conditioning time* n_{su} .
11. Do not exceed the operating voltage ranges at the inputs X, Y, GND32 (s. 4.6)
12. Use the E-502 "with common ground" operation mode only in case of closely located low-resistance signal sources. Optimizing the n_{su} **and** n_{av} settings for the "common ground" mode is required. Do not make "common ground" connections through the cable, if there are no low-resistance pull-up resistors on the E-502 side.
13. When connecting the E-502 "with common ground", the GND32 circuit must be in the same group of cable wires (in particular, within the same shield) as the other X and Y circuits operating on the "common ground" scheme.
14. When using 16 to 31 channels, it is advisable to combine E-502 "differential" and "common ground" connections and settings to obtain more channels operating in differential mode. In this case, the wires X and Y (differential circuit) and the wires X, Y, GND32 ("common ground" circuits) should form different groups in the cable in a common AGND circuit situation for these groups.
15. Do not allow through-currents on the shields and common wires of analog and digital signal circuits. Consider the internal circuit for connecting the common wires of the signal circuits to E-502 (p. 4.1, p. 4.2).

4.8. Calculation of total load power of E-502 output circuits

If you intend to use E-502 output circuits to connect any external loads, then the total load power should not exceed the power specified in the specification (paragraph 5.7 on page 52). The load power should be estimated according to the procedure described below.

Total load power P, taken from the supply system E-502, is:

$$P = \sum P_{DO} + \sum P_{DAC} + P_{+15} + P_{-15} + P_{3,3}$$

where P_{DO} is the total load power taken from digital DO outputs in the "1" state (only for loads connected to the GND circuit);

P_{DAC}— power load removed from the DAC outputs;

P_{+15}— power load, taken from the output of +15 V;

P_{-15}— power load, taken from the output of -15 V;

$P_{+3,3}$— power load, taken from the output of +3.3 V;

In turn, the power summandsP_{DO} of the corresponding i-th outputs must be calculated either through the known load currentI_{DO}^{i} by the formula$P_{DO}^{i} = 3{,}3 * I_{DO}^{i}$, or through the known load resistance R_{DO}^{i} at the i-th output $P_{DO}^{i} = \frac{10{,}9}{R_{DO}^{i}}$

The power summandsP_{DAC} of the corresponding j-th outputs must be calculated either through the known load currentI_{DAC}^{j} by the formula$P_{DO}^{j} = 5{,}0 * I_{DAC}^{j}$, or through the known load resistance R_{DAC}^{j} at the j-th output $P_{DAC}^{j} = \frac{25}{R_{DO}^{j}}$

The power P_{+15} and P_{-15} should also be calculated either through known load currents $I_{+15} + I_{-15}$by formulas $P_{+15} = 5{,}0 * I_{+15}$,$P_{-15} = 5{,}0 * I_{-15}$or through a known load resistance R_{+15}, according to R_{-15} formulas $P_{+15} = \frac{25}{R_{+15}}$, $P_{-15} = \frac{25}{R_{-15}}$

All terms in the power formulas are positive, dimension: power — Watt, current — Ampere, resistance — Ohm

Chapter 5. Specifications.

The following specifications show the main parameters of the E-502 for its intended operating mode.

!	*For the maximum permissible voltages and currents at the contacts of the connectors, see section 4.5, on p. 40.*

5.1. ADC

Parameter	Value
Number of channels	16 differential or 32 with "common ground" (single - phase)
DC Voltage Measurement Range Voltage measurement subranges (the input signal is applied between Xi and Yi for 16-channel mode, between Xi (Yi) and GND32 for 32-channel mode)	±10 V ±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V, ±0.2 V when *observing the operating conditions of the measurement (see below)*
Operating conditions of measurement at the ADC inputs (s. 4.6, p. 41)**:** - Voltages at the input Yi with regard to AGND for the differential measurement mode on the subbands "± 10 V", "± 5 V" - The average value of the voltage at the inputs X and Y for the differential mode on the measurement subranges "± 2 V", "± 1 V", "± 0.5 V", "± 0.2 V" - Voltages at the GND32 input relative to AGND for the "common ground" mode and all measurement subbands	$\lvert U_X \rvert \leq \pm 1$ V $\lvert (U_X + U_Y)/2 \rvert \leq \pm 1$ V $\lvert U_{GND32} \rvert \leq \pm 1$ V
Analog-to-digital converter bit depth	16 bits
ADC data width after arithmetic processing (data correction, data averaging)	24 bits
Limits of the permissible reduced basic error of DC voltage measurements, %, in subbands: – 10; 5 and 2 V – 1 V – 0.5 V – 0.2 V	 ±0.05 ±0.07 ±0.1 ±0.2
Own input current (via X, Y or GND32 circuits) in single-channel mode, no more than	0.4 µA
Charge injection into the input circuit of the ADC (X, Y or GND32) for one switching	2 pC
Possibility of data correction (use of calibration coefficients)	Yes
Common-mode rejection ratio 50 Hz with 1 V amplitude in differential mode on sub-band: ±10 V ±5 V ±2 V	 77 dB 83 dB 90 dB

±1 V ±0.5 V ±0.2 V	92 dB 92 dB 92 dB
Resistance to overloads by input measuring signal of DC voltage	±15 V
Limits of the permissible relative fundamental error of the ADC conversion frequency	±0.005 %
AC voltage measurement range	From 0.2 mV to 7 V
Limits of the permissible relative basic error of measuring the AC voltage	According to section 5.1.1

5.1.1. Limits of the permissible relative basic error of measuring the AC voltage

Frequency range of input signal, kHz	Limits of the permissible relative basic error of measuring the AC voltage, %
from 0.01 to 50 incl.	$\pm[0{,}15 + 0{,}02 \times (\frac{X_{AC}}{X} - 1)]$
more than 50 to 100 incl.	$\pm[0{,}3 + 0{,}02 \times (\frac{X_{AC}}{X} - 1)]$
more than 100 to 300 incl.	$\pm[1 + 0{,}03 \times (\frac{X_{AC}}{X} - 1)]$
more than 300 to 999	$\pm[5 + 0{,}05 \times (\frac{X_{AC}}{X} - 1)]$

Notes

1 The error in measuring the AC voltage is normalized in the differential connection scheme E-502 at the ADC conversion frequency of 2000 kHz, for signals whose peak values do not exceed the value of the set measurement subband.

2 X_{AC} is the AC voltage measurement limit, $X_{AC} = \frac{X_K}{\sqrt{2}}$ where X_K is the value of the set voltage subband.

3 X_K is the final value of the set voltage subband.

4 X is the value of the measured voltage.

5.1.2. ADC own input noise.

Data entry rate, Kword/s from one ADC channel	**Averaging factor**	**ADC subrange, V**					
		±10	±5	±2	±1	±0.5	±0.2
		Typical value of the noise level, applied to the ADC input, µV					
2000	1	420	175	87	40	26	23
400	5	185	78	40	18	12	11
50	20	93	38	20	10	7	6
10	128	40	25	12	7	5	4

5.1.3. ADC inter-channel passing.

Signal source resistance (in the channel where the interchannel passage is measured)	**Channel polling time,** µs (with averaging factor equal to 1**) or channel setup time, µs**					
	0.5	1.0	2.0	4.0	8.0	16.0
	Interchannel traversal, dB (the signal from the previous channel in the order of interrogation)					
0-50 Ohm	**-65**	**-78**	**-82**	**-82**	**-82**	**-82**
1 kOhm	-35	-63	-73	-82	-82	-82
10 kOhm	-5	-11	-22	-43	-74	-82

5.2. DAC.

Parameter	Value
Number of channels	2
Output frequency in synchronous mode	1 Msample/s per each channel
Output frequency in asynchronous mode	The actual speed depends on many factors of the software and hardware environment.
DAC bit depth, bit	16
Output modes	Asynchronous. Synchronous streaming, synchronous self-oscillator
Output signal range	±5 V
Operating range of output currents	±10 mA
Limits of the allowed reduced basic error of reproducing DC voltage	±0,1 %
Maximum allowable output current[6]	±20 mA
AC voltage playback range	From 1 mV to 3.5 V
AC voltage playback error	According to section 5.2.1

5.2.1. AC voltage playback error

Output voltage frequency, KHz	**Limits of the permissible relative basic error of AC playback voltage, %**
From 0.01 to 5 incl.	$\pm[0{,}15 + 0{,}02 \times (\frac{X_{AC}}{X} - 1)]$
More than 5 to 15 incl.	$\pm[0{,}5 + 0{,}05 \times (\frac{X_{AC}}{X} - 1)]$

[6] If the total load power is not exceeded, see s. _____ output circuits

More than 15 to 50 incl.	$\pm[3{,}0 + 0{,}1 \times (\frac{X_{AC}}{X} - 1)]$
More than 50 to 100 incl.	$\pm[15{,}0 + 0{,}3 \times (\frac{X_{AC}}{X} - 1)]$
Notes 1 X_{AC} – the final value of the range of AC voltage playback, X_{AC} = 3.5 V. 2 X is the value of the voltage to be reproduced.	

5.3. Digital inputs.

Parameter, characteristics	Value, description
Total number of digital inputs (DI1-DI16, DI_SYN1, DI_SYN2) Of these, the number of digital inputs with synchronization function (DI_SYN1, DI_SYN2)	18 2
Data entry modes	Asynchronous Synchronous streaming, synchronous self-oscillator.
Program control of pull-up resistors activation: - for inputs DI1-DI16 - for inputs DI_SYN1, DI_SYN2	 **No pull-up resistors** (unlike L-502) Regardless of each input
Maximum speed in synchronous mode	2 Mwords/s
Maximum speed in asynchronous mode.	The actual speed depends on many factors of the software and hardware environment.
Recommended operating voltage range	0 …+5.5 V
Operating voltage range	-0.2...+0.6 V ("logical zero") +2.4...+5.0 V ("logical item").
High-impedance state with power off	Yes
Maximum input current with power off	10 µA
Own input current in operating mode with software-activated pull-up resistors	10 µA
Recommended edge duration: - at the input DI1-DI16 - DI_SYN1, DI_SYN2	 0…50 ns Not limited
The input hysteresis voltage DI_SYN1, DI_SYN2, typical value	400 mV

5.4. Digital outputs.

Parameter	Value
Number of digital outputs of general purpose	16
Control of the third state of outputs	Byte
Data entry modes	Synchronous, asynchronous
Maximum speed in synchronous mode	1 KWords/s
Maximum speed in asynchronous mode	the actual speed depends on many factors of the software and hardware environment.
Maximum permissible current[7] in the load circuit	20 mA
Recommended current in the load circuit	max. 8 mA
Voltage range at digital outputs	0...+0.4 V ("logical zero") max. 2.4 V ("logical unit"). Output logic elements with a supply voltage of 3.3 V
Output resistance, typical value	110 Ohm
Maximum leakage current in operating mode in high-impedance state	±1 µA
High-impedance state with power off	No

5.5. Synchronization in E-502.

Parameter	Value
The reference frequency of the process of synchronization of data collection and output of ADC, DAC, digital input and output: • For a single module • For a multiple module synchronization	 1.5/2.0 MHz 1,5 MHz
Limits of the permissible relative fundamental error of the reference frequency	±0.005

[7] If the total load power is not exceeded, see s. _____ output circuits

5.6. Characteristics of standard interfaces.

Parameter, characteristics	Value, description
Interface with a computer	
Standards for interfaces with PC	USB 2.0 100BASE-TX
Bit depth of program data word	32 bits
Data transmission speed • via USB on input and output • via Ethernet on input • via Ethernet on output	 5 Mwords/s 2.5 Mwords/s To be confirmed
Interfaces of ADSP-BF523 (E-502-P) signal processor	
Interface with a computer	HOST DMA 16 bits
Main interface of input-output for ADC, DAC, digital I/O	SPORT0, >120 Mbit/s, duplex
Main control interface	SPI
A number of auxiliary I/O ports for connection with FPGA	
SDRAM interface	32 MB; 16 bit; 132.5 MHz
Debugging interface	JTAG
Compatibility with JTAG emulators Analog Devices	ADZS-ICE-100B, ADZS-USB-ICE, ADZS-HPUSB-ICE.

5.7. Power supply system and galvanic isolation.

Parameter, characteristics	Value, description
Operating voltage range of the E-502 low-voltage supply input	+8…+30 V
Power consumption: • From the external E-502 power source • From the USB input	 to 6 W No more than 0.025 W
Test voltage of galvanic isolation: • Between AGND, DGND circuits, connected together, and GND • Between GND circuits and Ethernet lines, connected together	 400 V 50 Hz during 1 min. 1500 V 50 Hz during 1 min.
Maximum permissible voltage rise rat between galvanically isolated circuits	10 kV / μs
The total load power taken from all outputs E-502 (according to the method of estimating the load power is given in p. 4.8 on page 44) For E-502-P-EU-D For E-502-X-U-D For E-502-X-U-X	The method for estimating the load power is given in p. 4.8, p. 44 0.4 W 0.4 W 0.8 W
External analog power supply outputs	+15 V, -15V. The maximum load current is up to 30 mA, provided that the total load power is not exceeded. SC is prohibited. Outputs are switched on by jumpers, (see p.2.2.1), this possibility is dependent on whether the corresponding outputs of the DAC are used
External digital circuits supply output	+3.3 V. The operating current of the load is up to 50 mA permanently, up to 100 mA for a short time.

5.8. Construction specification.

Parameter	Value
Dimensions	140 x 112 x 39 mm (without cable connectors)
Weight, max.	350 g (with a case, without cable connectors)

5.9. Environmental conditions.

5.9.1. Normal conditions

Parameter	Value
Normal operating conditions: – environment temperature, ℃ – relative humidity, % – air-pressure, kPa	 20±5 from 30 to 80 from 84 to 106

5.9.2. Operating conditions

Parameter	Value
For stability under climatic influences, the converters, in addition to the versions with the letter index I, correspond to GOST 22261, group 3 with an extended range of operating temperatures: – environment temperature, ℃ – relative humidity at an ambient temperature of 25 °C, % – air-pressure, kPa	 from +5 to +55 up to 90 from 70 to 106.7
For stability under climatic influences, converters of designs with the letter index I correspond to GOST 22261, group 4 with an extended range of operating temperatures: – environment temperature, ℃ – relative humidity at ambient temperature of 30 °C, % – air-pressure, kPa	 from -40 to +60 up to 90 from 60 to 106.7

Chapter 6. Connexion samples.

! These connection examples should be considered inextricably with the recommendations for connection and settings of the E-502 (p. 4.7).

The short form of information provided in this chapter does not cover all the features of the connection for your particular case. If necessary, please contact: en@lcard.ru or in the conference on the site en.lcard.ru.

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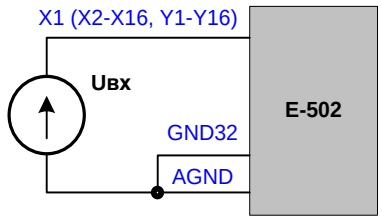
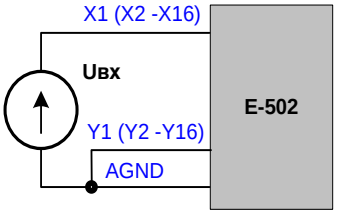
6.1. ADC entry point connection

6.1.1. Connecting to the ADC entry point of single-phase voltage source

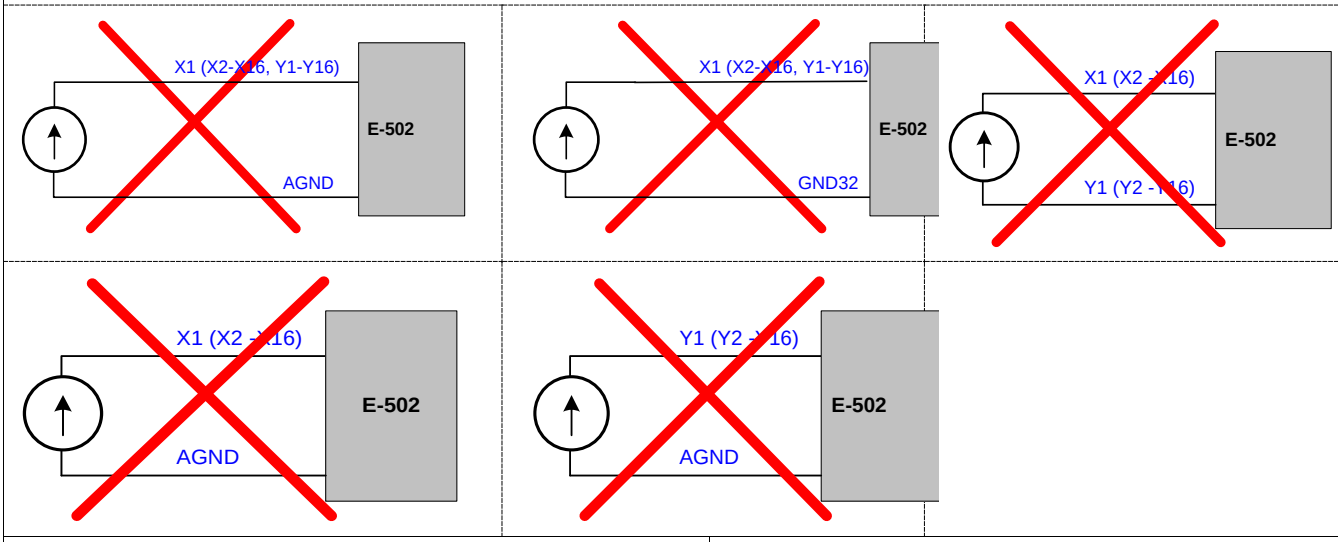
6.1.1.1. Up to 32 channels. Mode "with common ground"



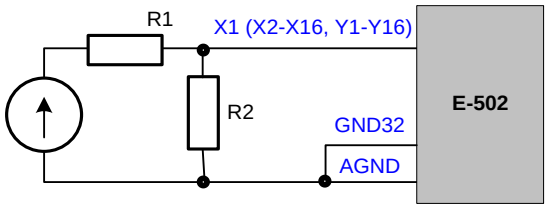
6.1.1.2. Up to 16 channels. "Differential" mode



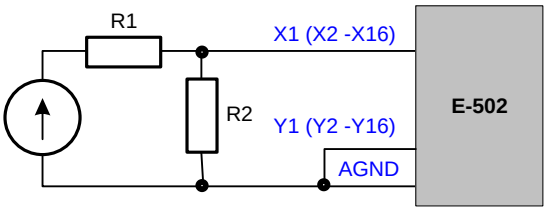
Forbidden to connect in this way!:



6.1.1.3. Voltage divisor. Mode "with common ground"

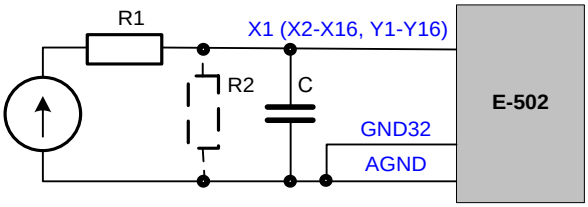


6.1.1.4. Voltage divisor. "Differential" mode

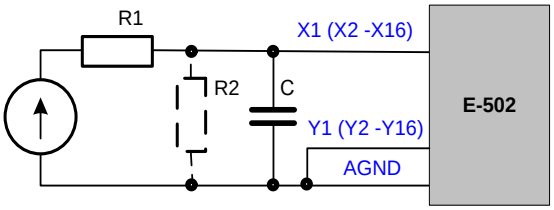


The voltage transfer ratio is R2/(R1+R2).
It is necessary that R1 or R2 should not be more than 50 ohms if the switching frequency is maximal.
R2 should be located close to E-502 input.

6.1.1.5. Integrating circuit. Mode "with common ground"

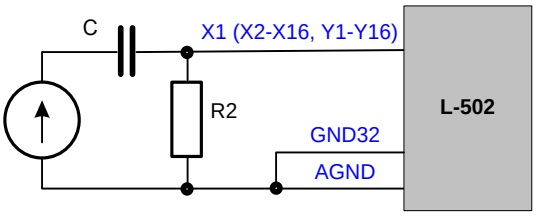


6.1.1.6. Integrating circuit. "Differential" mode

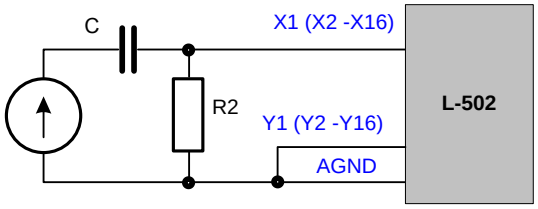


The transmission coefficient of the voltage in the frequency band is R2/(R1+R2).
If multichannel mode, it is necessary that $1/F_{ADC} >> R1*R2*(C+10^{-10})/(R1+R2)$, or if R2 is not present, then $1/F_{ADC} >> R1*(C+10^{-10})/R1$, where F_{ADC} is the ADC conversion frequency.
It is necessary that R2 should not be more than 50 ohms if the switching frequency is maximal.
R2, C should be located close to E-502 input.

6.1.1.7. Closed entry. Mode "with common earth"



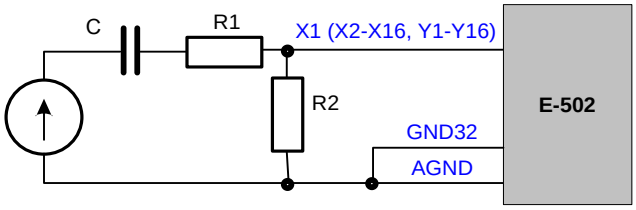
6.1.1.8. Closed entry. Mode "differential"



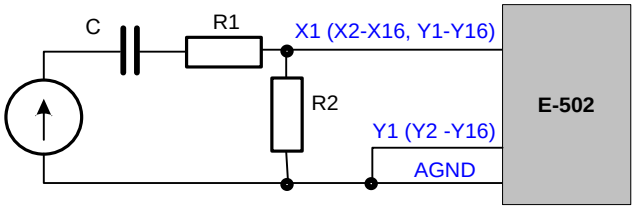
The connection is recommended for single-channel mode.

R should be located close to E-502 input.

6.1.1.9. Closed entry with divider. Mode "with common ground"



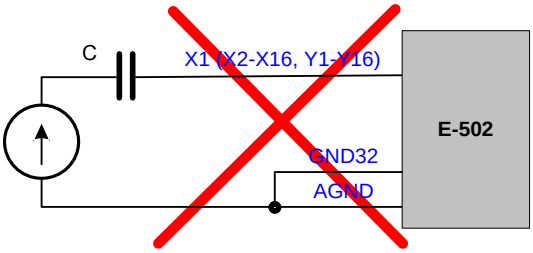
6.1.1.10. Closed entry with divider. "Differential" mode

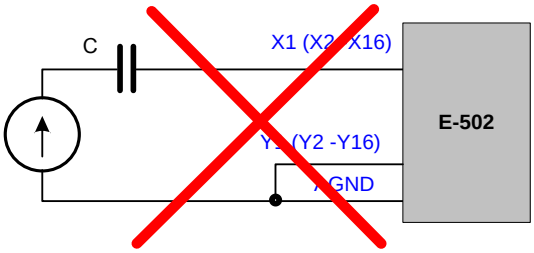


In multi-channel mode, the connection is correct only for R2 << R1 and R2 ≤ 50 Ω.

R2 should be located close to E-502 input.

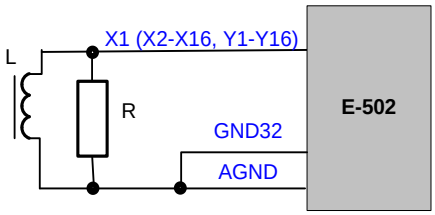
The transmission coefficient of the voltage in the passband is R2/(R1+R2).



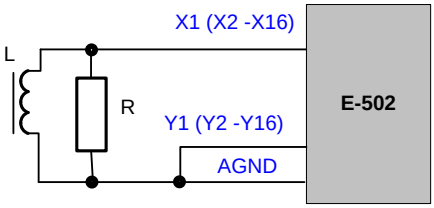


Can not be connected like this!

6.1.1.11. Inductive pickup. Mode "with common ground"



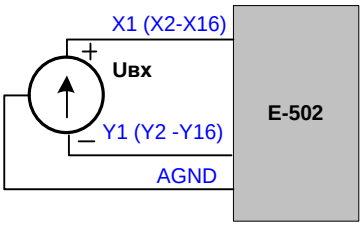
6.1.1.12. Inductive pickup. "Differential" mode



Resistor R performs the function of a damper to suppress the oscillation process in the L-C circuit, where C is the equivalent total capacitance applied in parallel to L. The ADC entry capacitance is estimated to be 25 pF. R resistor should be located close to E-502 input.

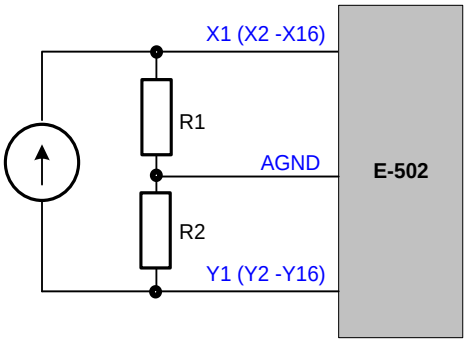
6.1.2. Connection to ADC input with up to 16 differential voltage sources

6.1.2.1. General case



Only for E-502 voltage subbands: ± 2 V, ± 1 V, ± 0.5 V, ± 0.2 V.

6.1.2.2. Differential connection of an isolated voltage source

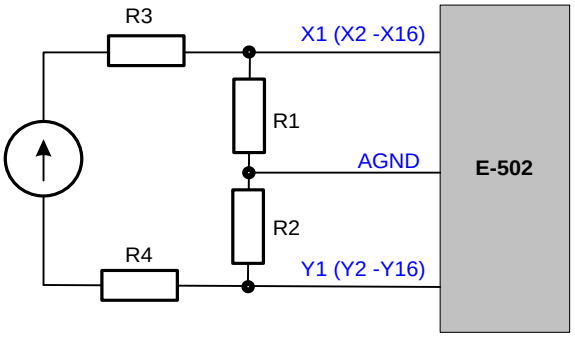


The following condition should be met:
(R1 = R2) ≤ 50 Ω, if the switching frequency is maximal.

R1, R2 should be located close to E-502 input

Only for voltage subbands:
± 2 V, ± 1 V, ± 0.5 V, ± 0.2 V.

6.1.2.3. Differential connection of an isolated voltage source with divider



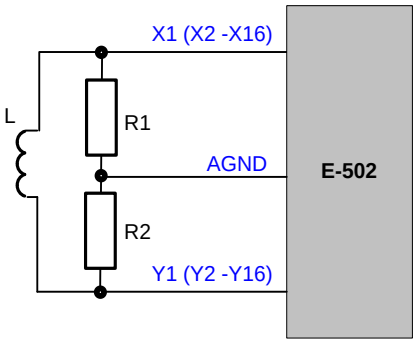
It is necessary: R1 ≤ 50 Ω, if the switching frequency is maximal, R1 = R2, R3 = R4..

Locate R1, R2 close to E-502 input.

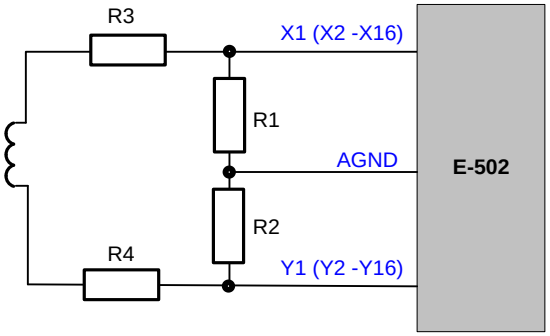
The voltage transfer ratio is (R1+R2)/(R1+R2+R3+R4)

Only for voltage subbands:
±2 V, ±1 V, ±0.5 V, ±0.2 V

Special case: differential connection of the inductive sensor:

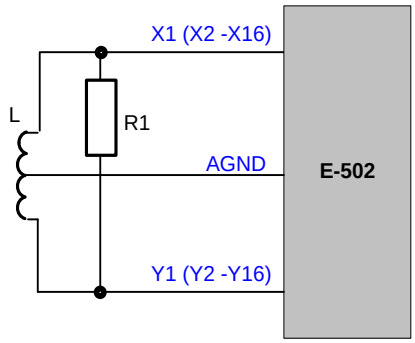


Only for voltage subbands:
±2 V, ±1 V, ±0.5 V, ±0.2 V



Only for voltage subbands:
±2 V, ±1 V, ±0.5 V, ±0.2 V

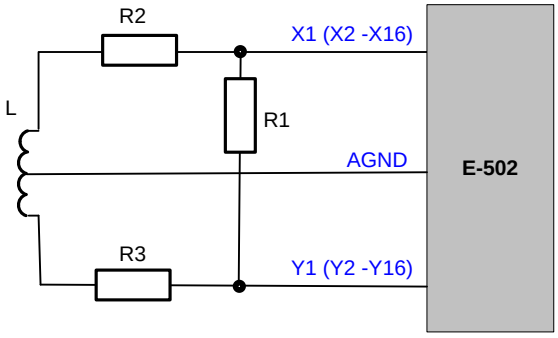
6.1.2.4. Differential winding connection with midpoint



Locate R1 close to E-502 input.

Only for E-502 voltage subbands: ±2 V, ±1 V, ±0.5 V, ±0.2 V

6.1.2.5. Differential winding connection with midpoint through the divider

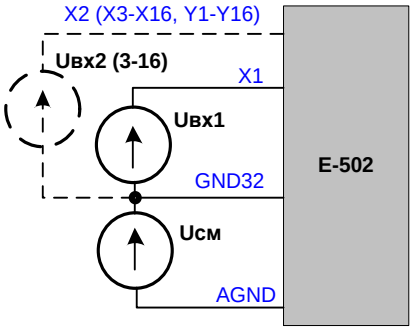


Locate R1 close to E-502 input.

Only for E-502 voltage subbands: ±2 V, ±1 V, ±0.5 V, ±0.2 V

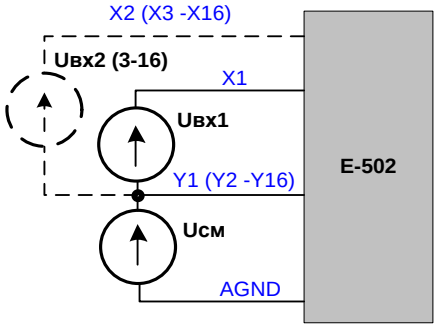
6.1.3. Connection to the ADC input for the case where the common wire of the signal sources has a offset potential **Ucm of max. ± 1 V** relative to the AGND circuit.

6.1.3.1. Connection up to 32 channels. Mode "with common ground"



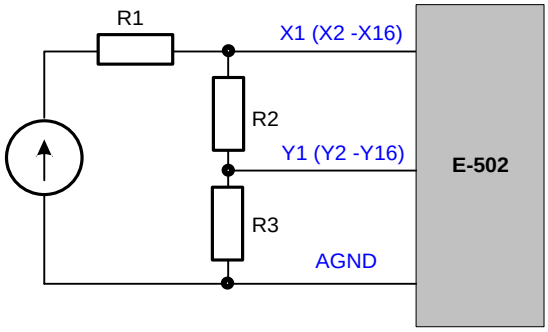
See limitations in section 4.6, p. 412!

6.1.3.2. Connection up to 16 channels. "Differential" mode



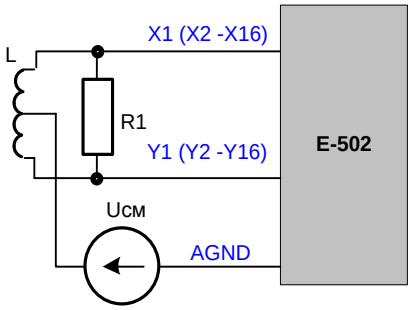
See limitations in section 4.6, p. 412!

6.1.4. Measurement of the voltage drop on the circuit section in the differential mode (up to 16- channels)



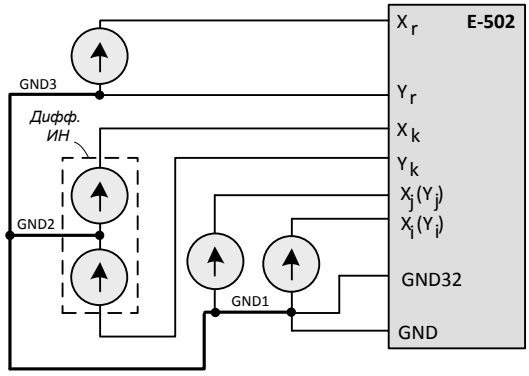
This connection allows you to measure the voltage drop *across resistor R2*. **For a single-channel mode**, R1, R2, R3 can also be impedances of a capacitive or inductive nature, but with the condition that the circuits X and Y used are not broken by the direct current of the circuit. **In multichannel mode**, the equivalent impedance referred to the ADC input must be active. It is necessary that R2 should not be more than 50 ohms if the switching frequency is maximal. See limitations in section 4.6, p.412!

6.1.5. Differential connection of the transformer (throttle) winding with midpoint and offset potential with respect to AGND



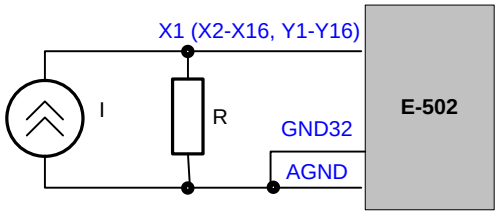
Limitations:
|Ucm| ≤ 1 V
Only for E-502 voltage subbands:
±2 V, ±1 V, ±0.5 V, ±0.2 V

6.1.6. Example of mixed connection of voltage sources "with common ground" and differential.

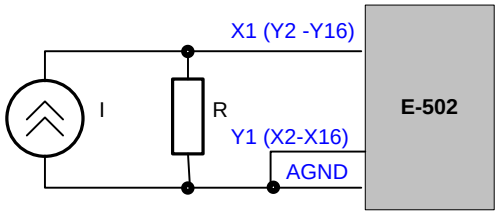


6.1.7. Connecting a power supply to the ADC input

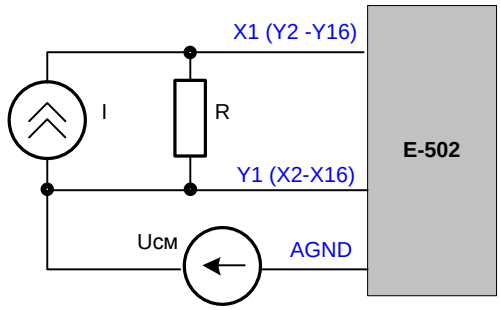
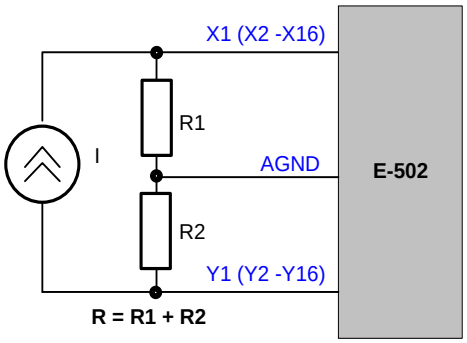
6.1.7.1. Mode "with common ground"



6.1.7.2. Differential mode



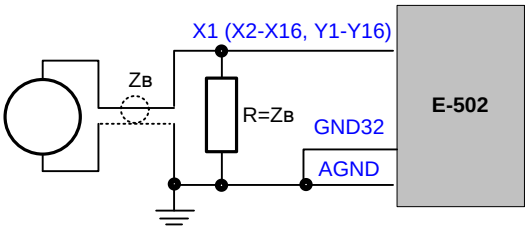
Fixed ADC ± U subband must correspond to $U=I_{MAX}*R$, and the current source must have a voltage margin of at least U. Resistor R should always be located close to the ADC input. In any case, the resistor R must be less than 50 Ω in the multi-channel mode at the maximum switching frequency.

6.1.7.3. Differential mode, offset potential due to current source in regard to AGND	*6.1.7.4. Differential mode, isolated current source*
	 *Only for E-502 voltage subbands:* ±2 V, ±1 V, ±0.5 V, ±0.2 V
Fixed ADC ± U measurement subband must correspond to $U=I_{MAX}*R$, while the current source must have a voltage margin of, at least, U. Resistor R should always be located close to the ADC input. Resistors R, R1, R2 must be less than 50 Ω in multichannel mode at the maximum switching frequency. **|Ucm| ≤ 1 B**	

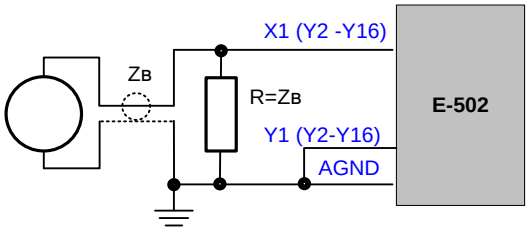
6.1.8. The coordinated connection of remote sources of current or voltage through a long line with a wave impedance Zw

(If the signal source has an output impedance, unequal to Zw, then these cases correspond to one-way matching of the long line on the side of the signal receiver)

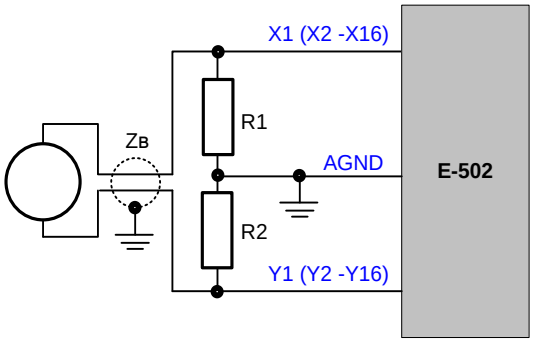
6.1.8.1. Mode "with common ground"



6.1.8.2. Differential mode



6.1.8.3. Differential connection of an isolated current source or voltage



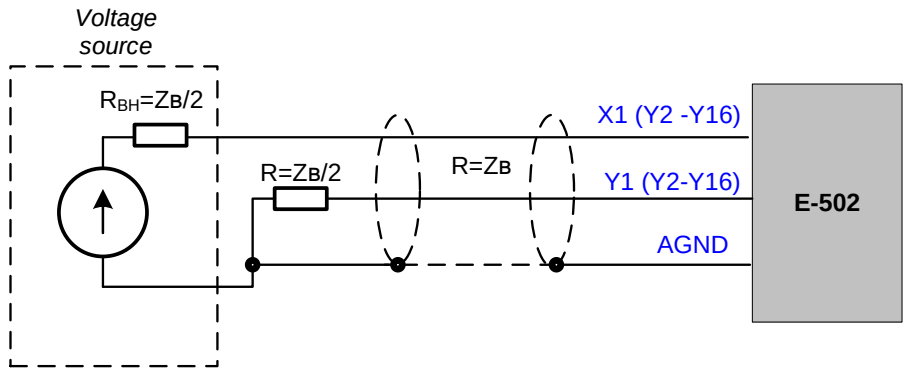
R1=R2

R1+R2 = Zw

The circuit is valid only for the following E-502 voltage sub-ranges:

±2 V, ±1 V, ±0.5 V, ±0.2 V

6.1.9. The coordinated connection of a remote voltage source through a pair of long line with a wave resistance Zw with matching on the signal source side

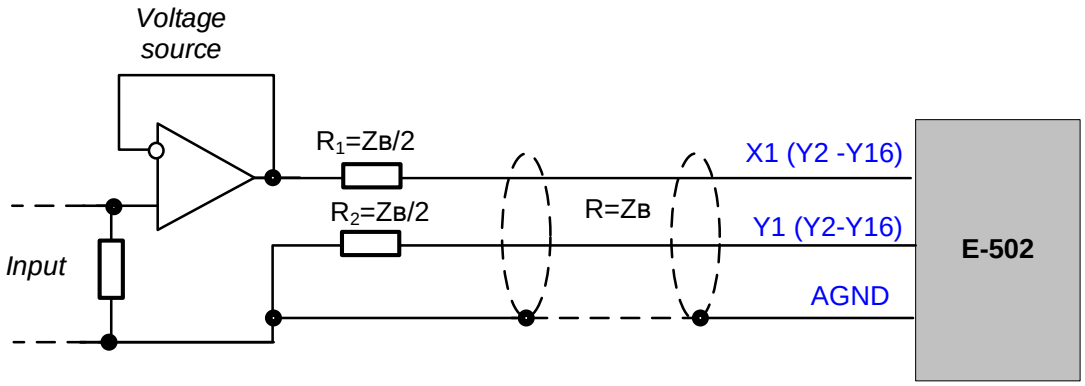


R_{BH} – internal (output) impedance of the signal source.

R – balancing resistor on the signal source side.

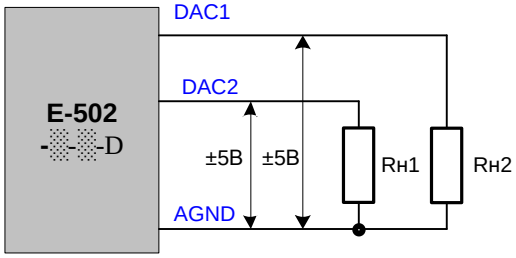
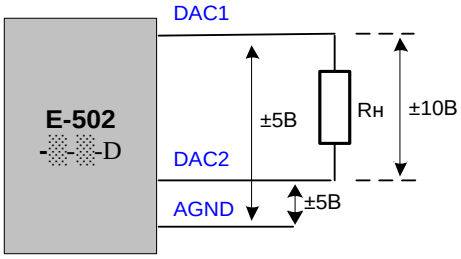
The cable must be paired (shielded twisted pairs) with wave resistance of wire pairs Zw.

Below is a practical case where a broadband operational amplifier acts as a remote voltage source (providing a low-impedance voltage output in the frequency band up to 10 MHz).



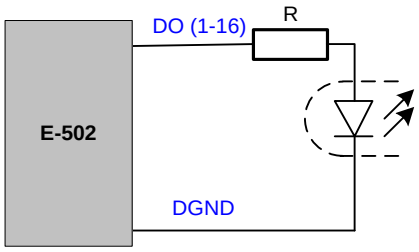
6.2. Connecting the DAC outputs.

To carryout the DAC function in E-502-▒-▒-D, the outputs DAC1 and DAC2 should be preconfigured with jumper, see p.2.2.1 p. 13

6.2.1. Mode "with common ground" 2-channel output ±5 V	6.2.2. Single-channel differential output ±10 V
	 The differential output ±10 V is realized as a difference voltage between the outputs DAC1 and DAC2

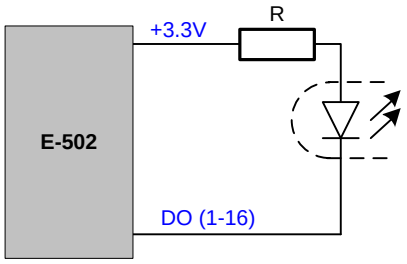
6.3. Connecting the digital inputs and outputs.

6.3.1. Connecting the LED or the optron input. Option 1



The LED is lit when the DO output is at the "logical unit".

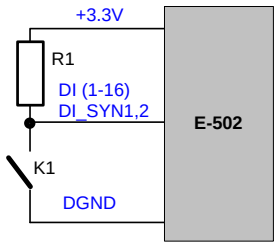
6.3.2. Connecting the LED or the optron input. Option 2



The LED is lit when the DO output is at the "logical zero".

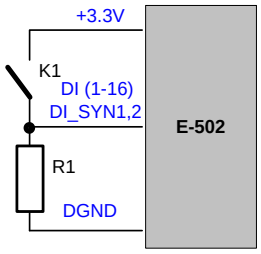
6.3.3. Connecting a contact to a digital input

Option 1



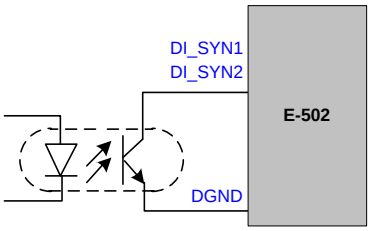
A logical unit corresponds to an open contact. The recommended resistor R1 nominal is from 3 to 5 kOhm.

Option 2



The open contact corresponds to a logical zero. The recommended resistor R1 nominal is from 3 to 5 kOhm.

6.3.4. Connect the optron output to the synchronization input



The digital inputs DI_SYN1,2, which can be used as synchronization inputs, are adapted to directly connect the optron output. The internal pull-up resistor of the DI_SYN1,2 input must be software-enabled.

Chapter 7. Design data

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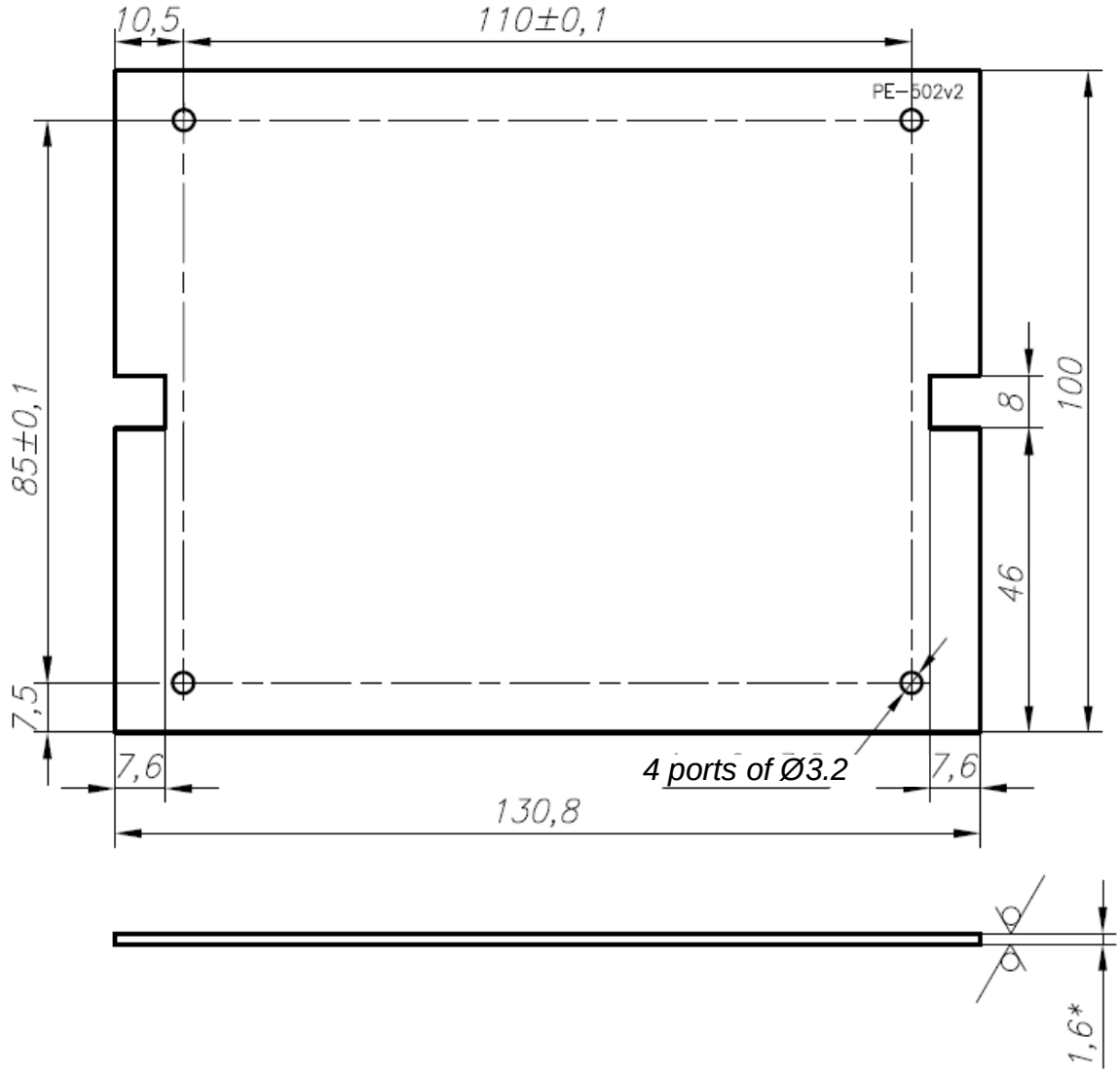
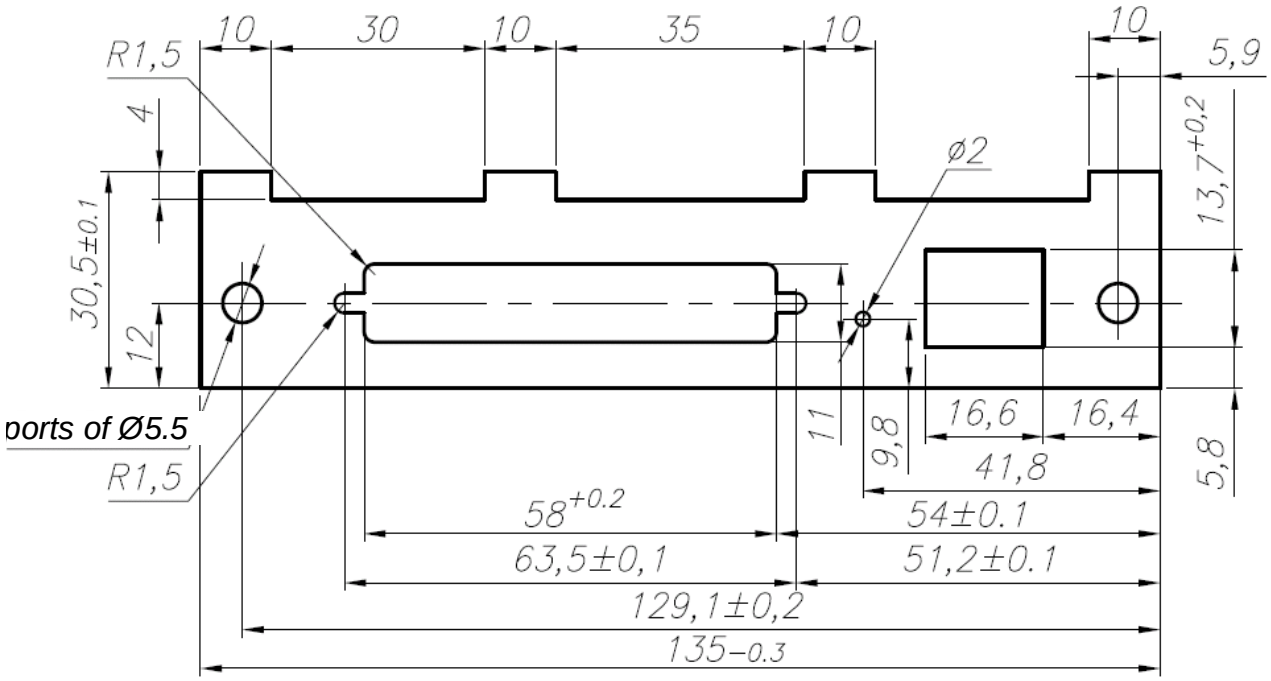
7.1. Circuit plate draft.

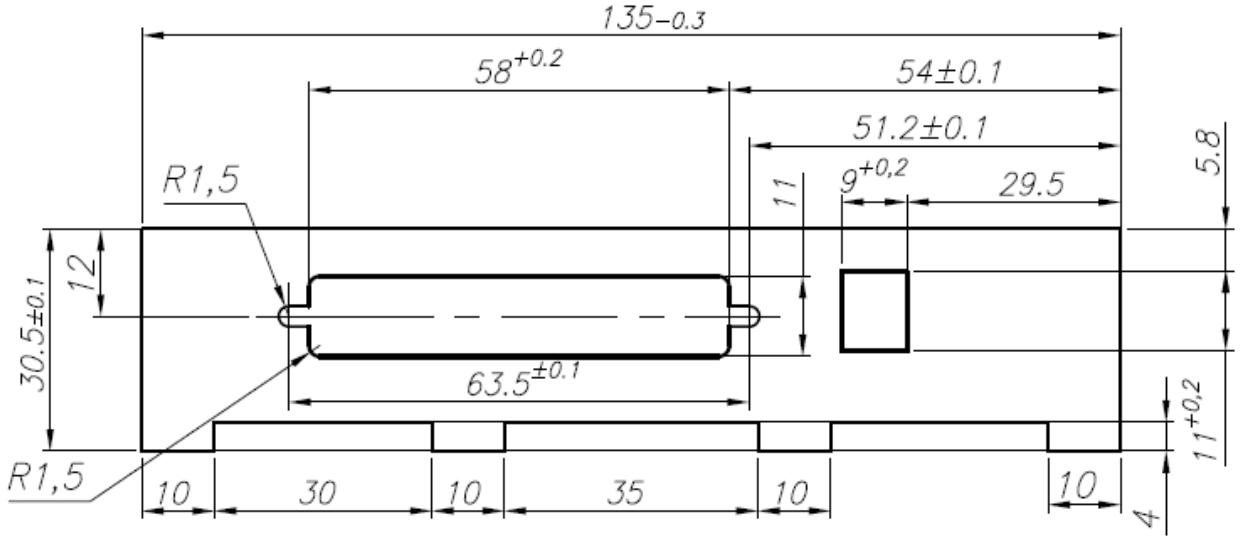


Note: diameter of 4 ports taking into account metallization: 3.05 mm

7.2. Front panel draft.



7.3. Back panel draft.



List of tables.

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